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Register Memory Map Quick Reference

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About This Book

The primary objective of this reference manual is to define the functionality of the MCF5208 processor for use by software and hardware developers. In addition, this manual supports the MCF5207. This book is written from the perspective of the MCF5208, and unless otherwise noted, the information applies also to the MCF5207. The MCF5207 has the same functionality as the MCF5208 and any differences in data regarding bus timing, signal behavior, and AC, DC, and thermal characteristics are in the hardware specifications. Please refer to [Table 1-1](#) to see a summary of the differences.

The information in this book is subject to change without notice, as described in the disclaimers on the title page. As with any technical documentation, it is the reader's responsibility to be sure he is using the most recent version of the documentation.

To locate any published errata or updates for this document, refer to the world-wide web at <http://www.freescale.com/coldfire>.

Audience

This manual is intended for system software and hardware developers and applications programmers who want to develop products with the MCF5208. It is assumed that the reader understands operating systems, microprocessor system design, basic principles of software and hardware, and basic details of the ColdFire[®] architecture.

Organization

Following is a summary and brief description of the major sections of this manual:

- [Chapter 1, “Overview,”](#) includes general descriptions of the modules and features incorporated in the device, focusing in particular on new features.
- [Chapter 2, “Signal Descriptions,”](#) describes the device signals. It includes a listing of signals that characterizes each signal as an input or output, defines its state at reset, and identifies whether a pull-up resistor should be used.
- [Chapter 3, “ColdFire Core,”](#) provides an overview of the microprocessor core. The chapter describes the organization of the Version 2 (V2) ColdFire processor core and an overview of the programming model as they are implemented on the device.
- [Chapter 4, “Enhanced Multiply-Accumulate Unit \(EMAC\),”](#) describes the multiply/accumulate unit, which executes integer multiply, multiply-accumulate, and

miscellaneous register instructions. The EMAC is integrated into the operand execution pipeline (OEP).

- [Chapter 5, “Cache,”](#) describes the cache implementation, including organization, configuration, and coherency. It describes cache operations and how the cache interacts with other memory structures.
- [Chapter 6, “Static RAM \(SRAM\),”](#) describes the on-chip static RAM (SRAM) implementation. It covers general operations, configuration, and initialization. It also provides information and examples of how to minimize power consumption when using the SRAM.
- [Chapter 7, “Clock Module,”](#) describes the device’s different clocking methods. It also describes clock module operation in low power modes.
- [Chapter 8, “Power Management,”](#) describes the low power operation of the device and peripheral behavior in low power modes.
- [Chapter 9, “Chip Configuration Module \(CCM\),”](#) details the various operating configurations of the device. This chapter provides a description of signals used by the CCM and a programming model.
- [Chapter 10, “Reset Controller Module,”](#) describes the operation of the reset controller module, detailing the different types of reset that can occur.
- [Chapter 11, “System Control Module \(SCM\),”](#) describes the functionality of the SCM, which provides the programming model for peripheral access control, the software core watchdog timer (CWT), and the generic access error information.
- [Chapter 12, “Crossbar Switch \(XBS\),”](#) details the interaction between bus masters and bus slaves within the device, including arbitration schemes.
- [Chapter 13, “General Purpose I/O Module,”](#) describes the operation and programming model of the general purpose I/O (GPIO) ports on the device.
- [Chapter 14, “Interrupt Controller Module,”](#) describes operation of the interrupt controller portion of the SCM. Includes descriptions of the registers in the interrupt controller memory map and the interrupt priority scheme.
- [Chapter 15, “Edge Port Module \(EPORT\),”](#) describes EPORT module functionality, including operation in low power mode.
- [Chapter 16, “Enhanced Direct Memory Access \(eDMA\),”](#) describes the direct memory access (DMA) controller module. It provides an overview of the module and describes in detail its signals and registers. The latter sections of this chapter describe operations, features, and supported data transfer modes in detail.
- [Chapter 17, “FlexBus,”](#) describes data-transfer operations, chip-select operation, error conditions, bus arbitration, and reset operations.
- [Chapter 18, “SDRAM Controller \(SDRAMC\),”](#) describes the configuration and operation of the SDRAM controller. It begins with a general description and includes a description of

signals involved in DRAM operations. The remainder of the chapter describes the programming model and signal timing, as well as the command set required for synchronous operations.

- [Chapter 19, “Fast Ethernet Controller \(FEC\),”](#) provides a feature-set overview, a functional block diagram, and transceiver connection information for MII (media independent interface) and 7-wire serial interfaces. It also provides describes operation and the programming model.
- [Chapter 20, “Watchdog Timer Module,”](#) describes software watchdog timer functionality, including operation in low power mode.
- [Chapter 21, “Programmable Interrupt Timers \(PIT0–PIT1\),”](#) describes the functionality of the PIT timers, including operation in low power mode.
- [Chapter 22, “DMA Timers \(DTIM0–DTIM3\),”](#) describes the configuration and operation of the DMA timer modules. These 32-bit timers provide input capture and reference compare capabilities with optional signaling of events using interrupts or triggers. This chapter also provides programming examples.
- [Chapter 23, “Queued Serial Peripheral Interface \(QSPI\),”](#) provides a feature-set overview and a description of operation, including details of the QSPI’s internal storage organization. The chapter concludes with the programming model and a timing diagram.
- [Chapter 24, “UART Modules,”](#) describes the use of the universal asynchronous receiver/transmitters (UARTs) implemented on the device and includes programming examples.
- [Chapter 25, “I²C Interface,”](#) describes the I²C module, including I²C protocol, clock synchronization, and I²C programming model registers.
- [Chapter 26, “Debug Module,”](#) describes the hardware debug support in the device.
- [Chapter 27, “IEEE 1149.1 Test Access Port \(JTAG\),”](#) describes configuration and operation of the Joint Test Action Group (JTAG) implementation. It describes those items required by the IEEE 1149.1 standard and provides additional information specific to the device. For internal details and sample applications, see the IEEE 1149.1 document.

This manual includes the following appendices:

- [Appendix A, “Register Memory Map Quick Reference,”](#) provides the entire address map for memory-mapped registers.
- [Appendix B, “Revision History,”](#) provides a revision history for all previously released versions of this document.

Suggested Reading

This section lists additional reading that provides background for the information in this manual as well as general information about the ColdFire architecture.

Hardware Specification

The MCF5208EC document contains the mechanical and electrical specifications of the MCF5208. It can be found at <http://www.freescale.com/coldfire>.

General Information

The following documentation provides useful information about the ColdFire architecture and computer architecture in general:

- *ColdFire Programmers Reference Manual, R1.0* (MCF5200PRM/AD)
- *Using Microprocessors and Microcomputers: The Motorola Family*, William C. Wray, Ross Bannatyne, Joseph D. Greenfield
- *Computer Architecture: A Quantitative Approach*, Second Edition, by John L. Hennessy and David A. Patterson.
- *Computer Organization and Design: The Hardware/Software Interface*, Second Edition, David A. Patterson and John L. Hennessy.

ColdFire Documentation

ColdFire documentation is available from the sources listed on the back cover of this manual.

- Reference manuals (formerly called user's manuals)—These books provide details about individual ColdFire implementations and are intended to be used in conjunction with *The ColdFire Programmers Reference Manual*.
- Addenda/errata to reference manuals—Because some processors have follow-on parts, an addendum is provided that describes the additional features and functionality changes. Also, if mistakes are found within a reference manual, an errata document will be issued before the next published release of the reference manual. These addenda/errata are intended for use with the corresponding reference manuals.
- Hardware specifications—Hardware specifications provide specific data regarding bus timing, signal behavior, and AC, DC, and thermal characteristics, as well as other design considerations.
- Product briefs—Each device has a product brief that provides an overview of its features. This document is roughly equivalent to the overview (Chapter 1) of an implementation's reference manual.
- Application notes—These short documents address specific design issues useful to programmers and engineers working with Freescale Semiconductor processors.

Additional literature is published as new processors become available. For a current list of ColdFire documentation, refer to <http://www.freescale.com/coldfire>.

Conventions

This document uses the following notational conventions:

cleared/set	When a bit takes the value zero, it is said to be cleared; when it takes a value of one, it is said to be set.
MNEMONICS	In text, instruction mnemonics are shown in uppercase.
mnemonics	In code and tables, instruction mnemonics are shown in lowercase.
<i>italics</i>	Italics indicate variable command parameters. Book titles in text are set in italics.
0x0	Prefix to denote hexadecimal number
0b0	Prefix to denote binary number
REG[FIELD]	Abbreviations for registers are shown in uppercase. Specific bits, fields, or ranges appear in brackets. For example, RAMBAR[BA] identifies the base address field in the RAM base address register.
nibble	A 4-bit data unit
byte	An 8-bit data unit
word	A 16-bit data unit ¹
longword	A 32-bit data unit
x	In some contexts, such as signal encodings, x indicates a don't care.
<i>n</i>	Used to express an undefined numerical value
~	NOT logical operator
&	AND logical operator
	OR logical operator
<u>OVERBAR</u>	An overbar indicates that a signal is active-low.

Register Figure Conventions

This document uses the following conventions for the register reset values:

—	Undefined at reset.
u	Unaffected by reset.
[<i>signal_name</i>]	Reset value is determined by the polarity of the indicated signal.

The following register fields are used:

1. The only exceptions to this appear in the discussion of serial communication modules that support variable-length data transmission units. To simplify the discussion these units are referred to as words regardless of length.

R	0	Indicates a reserved bit field in a memory-mapped register. These bits are always read as zeros.
W		
R	1	Indicates a reserved bit field in a memory-mapped register. These bits are always read as ones.
W		
R	FIELDNAME	Indicates a read/write bit.
W		
R	FIELDNAME	Indicates a read-only bit field in a memory-mapped register.
W		
R		Indicates a write-only bit field in a memory-mapped register.
W	FIELDNAME	
R	FIELDNAME	Write 1 to clear: indicates that writing a 1 to this bit field clears it.
W	w1c	
R	0	Indicates a self-clearing bit.
W	FIELDNAME	

Acronyms and Abbreviations

Table 1 lists acronyms and abbreviations used in this document.

Table 1. Acronyms and Abbreviated Terms

Term	Meaning
ADC	Analog-to-digital conversion
ALU	Arithmetic logic unit
BDM	Background debug mode
BIST	Built-in self test
BSDL	Boundary-scan description language
CODEC	Code/decode
DAC	Digital-to-analog conversion
DMA	Direct memory access
DSP	Digital signal processing
EA	Effective address
FIFO	First-in, first-out
GPIO	General-purpose I/O

Table 1. Acronyms and Abbreviated Terms (continued)

Term	Meaning
I ² C	Inter-integrated circuit
IEEE	Institute for Electrical and Electronics Engineers
IFP	Instruction fetch pipeline
IPL	Interrupt priority level
JEDEC	Joint Electron Device Engineering Council
JTAG	Joint Test Action Group
LIFO	Last-in, first-out
LRU	Least recently used
LSB	Least-significant byte
lsb	Least-significant bit
MAC	Multiply accumulate unit, also Media access controller
MBAR	Memory base address register
MSB	Most-significant byte
msb	Most-significant bit
Mux	Multiplex
NOP	No operation
OEP	Operand execution pipeline
PC	Program counter
PCLK	Processor clock
PLIC	Physical layer interface controller
PLL	Phase-locked loop
POR	Power-on reset
PQFP	Plastic quad flat pack
PWM	Pulse width modulation
QSPI	Queued serial peripheral interface
RISC	Reduced instruction set computing
Rx	Receive
SIM	System integration module
SOF	Start of frame
TAP	Test access port
TTL	Transistor transistor logic
Tx	Transmit

Table 1. Acronyms and Abbreviated Terms (continued)

Term	Meaning
UART	Universal asynchronous/synchronous receiver transmitter
USB	Universal serial bus

Terminology Conventions

Table 2 shows terminology conventions used throughout this document.

Table 2. Notational Conventions

Instruction	Operand Syntax
Opcode Wildcard	
cc	Logical condition (example: NE for not equal)
Register Specifications	
An	Any address register n (example: A3 is address register 3)
Ay,Ax	Source and destination address registers, respectively
Dn	Any data register n (example: D5 is data register 5)
Dy,Dx	Source and destination data registers, respectively
Rc	Any control register (example VBR is the vector base register)
Rm	MAC registers (ACC, MAC, MASK)
Rn	Any address or data register
Rw	Destination register w (used for MAC instructions only)
Ry,Rx	Any source and destination registers, respectively
Xi	Index register i (can be an address or data register: Ai, Di)
Miscellaneous Operands	
#<data>	Immediate data following the 16-bit operation word of the instruction
<ea>	Effective address
<ea>y,<ea>x	Source and destination effective addresses, respectively
<label>	Assembly language program label
<list>	List of registers for MOVEM instruction (example: D3–D0)
<shift>	Shift operation: shift left (<<), shift right (>>)
<size>	Operand data size: byte (B), word (W), longword (L)
bc	Instruction and data caches
dc	Data cache
ic	Instruction cache

Table 2. Notational Conventions (continued)

Instruction	Operand Syntax
# <vector>	Identifies the 4-bit vector number for trap instructions
<>	identifies an indirect data address referencing memory
<xxx>	identifies an absolute address referencing memory
d <i>n</i>	Signal displacement value, <i>n</i> bits wide (example: d16 is a 16-bit displacement)
SF	Scale factor (x1, x2, x4 for indexed addressing mode, <<1 <i>n</i> >> for MAC operations)
Operations	
+	Arithmetic addition or postincrement indicator
–	Arithmetic subtraction or predecrement indicator
x	Arithmetic multiplication
/	Arithmetic division
~	Invert; operand is logically complemented
&	Logical AND
	Logical OR
^	Logical exclusive OR
<<	Shift left (example: D0 << 3 is shift D0 left 3 bits)
>>	Shift right (example: D0 >> 3 is shift D0 right 3 bits)
→	Source operand is moved to destination operand
↔	Two operands are exchanged
sign-extended	All bits of the upper portion are made equal to the high-order bit of the lower portion
If <condition> then <operations> else <operations>	Test the condition. If true, the operations after then are performed. If the condition is false and the optional else clause is present, the operations after else are performed. If the condition is false and else is omitted, the instruction performs no operation. Refer to the Bcc instruction description as an example.

Table 2. Notational Conventions (continued)

Instruction	Operand Syntax
Subfields and Qualifiers	
{ }	Optional operation
()	Identifies an indirect address
d_n	Displacement value, n-bits wide (example: d_{16} is a 16-bit displacement)
Address	Calculated effective address (pointer)
Bit	Bit selection (example: Bit 3 of D0)
lsb	Least significant bit (example: lsb of D0)
LSB	Least significant byte
LSW	Least significant word
msb	Most significant bit
MSB	Most significant byte
MSW	Most significant word

Chapter 1

Overview

The MCF5207 and MCF5208 devices are highly-integrated 32-bit microprocessors based on the Version 2 ColdFire microarchitecture. Both devices contain a 16-Kbyte internal SRAM, 8-Kbyte configurable cache, a two-bank SDR/DDR SDRAM controller, a 16-channel DMA controller, up to three UARTs, a queued SPI, as well as other peripherals that enable the MCF5207 and MCF5208 for use in general purpose industrial control applications. The MCF5208 device also features a 10/100 Mbps Fast Ethernet controller.

This chapter provides an overview of the MCF5207 and MCF5208 microprocessors. It was written from the perspective of the MCF5208 device. See the following section for a summary of differences between the two devices.

1.1 MCF5207/8 Device Configurations

The following table compares the various devices derivatives available:

Table 1-1. MCF5207 & MCF5208 Configurations

Module	MCF5207	MCF5208
Version 2 ColdFire Core with EMAC (Enhanced Multiply-Accumulate Unit)	•	•
Core (System) Clock	up to 166.67 MHz	
Peripheral and External Bus Clock (Core clock ÷ 2)	up to 83.33 MHz	
Performance (Dhrystone/2.1 MIPS)	up to 159	
Unified Cache	8 Kbytes	
Static RAM (SRAM)	16 Kbytes	
SDR/DDR SDRAM Controller	•	•
Fast Ethernet Controller (FEC)	—	•
UARTs	3	3
I ² C	•	•
QSPI	•	•
32-bit DMA Timers	4	4
Watchdog Timer (WDT)	•	•
Periodic Interrupt Timers (PIT)	2	2
Edge Port Module (EPORT)	•	•

Table 1-1. MCF5207 & MCF5208 Configurations (continued)

Module	MCF5207	MCF5208
Interrupt Controllers (INTC)	1	1
16-channel Direct Memory Access (DMA)	•	•
FlexBus External Interface	•	•
General Purpose I/O Module (GPIO)	•	•
JTAG - IEEE® 1149.1 Test Access Port	•	•
Package	144 LQFP 144 MAPBGA	160 QFP 196 MAPBGA

1.2 Block Diagram

The MCF5208 superset device is available in a 196 mold array process ball grid array (MAPBGA) or 160-pin quad flat pack (QFP) package. Figure 1-1 shows a top-level block diagram of the MCF5208.

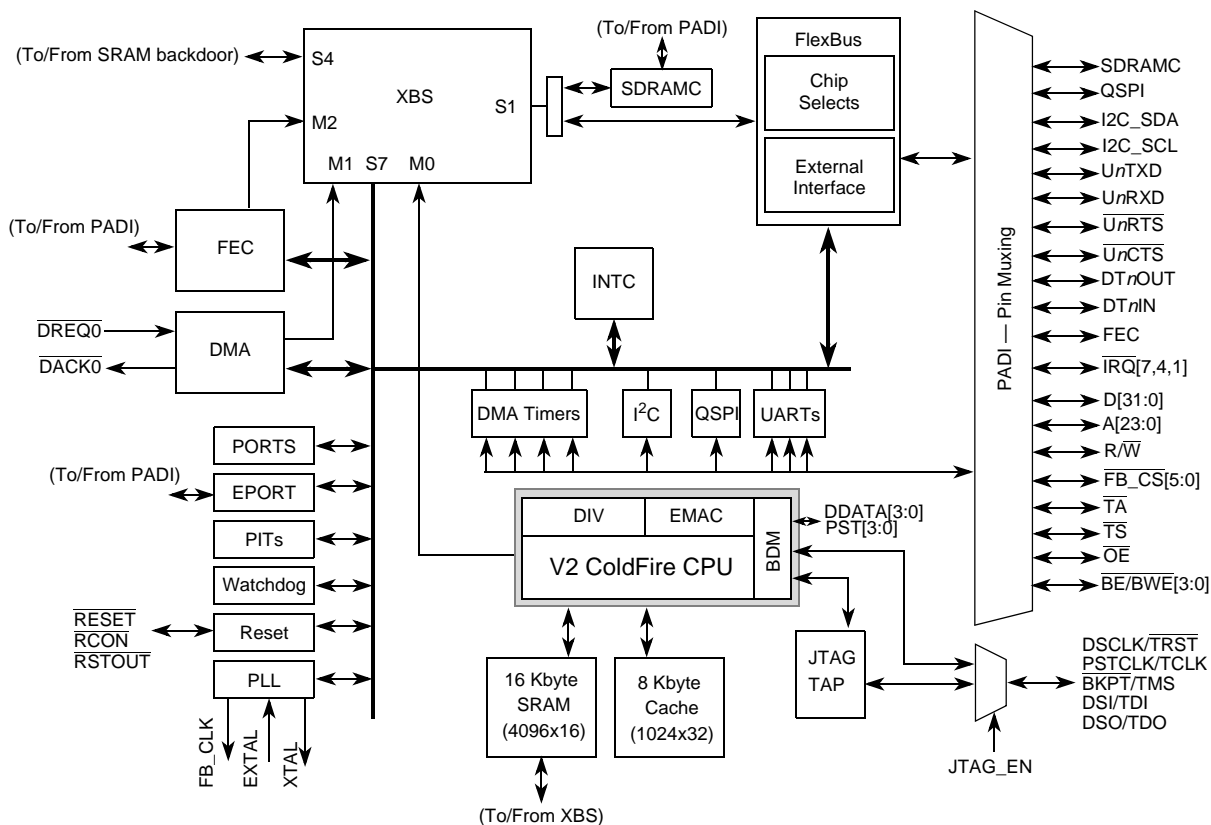


Figure 1-1. MCF5208 Block Diagram

1.3 Features

The following is a brief summary of the functional blocks in the MCF5208 superset device.

- Version 2 ColdFire variable-length RISC processor core
 - Static operation
 - 32-bit address and data path on-chip
 - Processor core runs at twice the bus frequency
 - Sixteen general-purpose 32-bit data and address registers
 - Implements the ColdFire instruction set architecture, ISA_A+, with extensions to support the user stack pointer register, and 4 new instructions for improved bit processing
 - Enhanced multiply-accumulate (EMAC) unit with four 48-bit accumulators to support 32-bit signal processing algorithms
 - Hardware divide execution unit supporting various 32-bit operations
 - Illegal instruction decode that allows for 68K emulation support
- System debug support
 - Background debug mode (BDM) revision B+ for in-circuit debugging
 - Real time debug support, with nine user-visible hardware breakpoint registers (PC and address with optional data) that can be configured into a 1- or 2-level trigger
- JTAG support for system level board testing
- On-Chip memories
 - 8-Kbyte cache, configurable as instruction-only, data-only, or split I-/D-cache
 - 16-Kbyte dual-ported SRAM on CPU internal bus, accessible by core and non-core bus masters (DMA and FEC)
- Power management
 - Fully static operation with processor wait, doze, and stop modes
 - Very rapid response to interrupts from sleep mode
 - Global clock disable register to disable clocks to most modules
 - Ability to bypass PLL circuitry for low-power and low-speed mode
- SDR/DDR SDRAM controller
 - Supports a glueless interface to SDR and DDR SDRAM devices
 - 16-bit (DDR) or 32-bit (SDR) fixed memory port width
 - 16 bytes critical word first burst transfer
 - Up to 14 lines of row address, up to 12 (in 32-bit mode) or 13 (in 16-bit bus mode) column address lines, 2 bits of bank address, and a maximum of two pinned-out chip selects. The maximum row bits plus column bits equals 24 in 32-bit bus mode or 25 in 16-bit mode.
 - Supports up to 256 MBytes of memory per chip select, 512 MBytes total
 - Supports page mode to maximize the data rate
 - Supports sleep and self-refresh modes
- Fast Ethernet controller (FEC)
 - 10/100 BaseT/TX capability, half duplex or full duplex
 - On-chip transmit and receive FIFOs

- Built-in dedicated DMA controller
- Memory-based flexible descriptor rings
- Media independent interface (MII) to external transceiver (PHY)
- Three universal asynchronous receiver transmitters (UARTs)
 - 16-bit divider for clock generation
 - Interrupt control logic
 - DMA support with separate transmit and receive requests
 - Data formats can be 5, 6, 7, or 8 bits with even, odd, or no parity
 - Up to two stop bits in 1/16 increments
 - Error-detection capabilities
 - Flow control support includes request-to-send (\overline{UnRTS}) and clear-to-send (\overline{UnCTS}) lines
- I²C module
 - Interchip bus interface for EEPROMs, A/D converters, and keypads
 - Fully compatible with industry-standard I²C bus
 - Master or slave modes support multiple masters
 - Automatic interrupt generation with programmable level
- Queued serial peripheral interface (QSPI)
 - Full-duplex, three-wire synchronous transfers
 - Up to three chip selects available
 - Master mode operation only with programmable master bit rates
 - Up to 16 pre-programmed transfers
- Four 32-bit DMA timers
 - 12-ns resolution at 83.33 MHz
 - Programmable prescaler and sources for clock input, including an external clock option
 - Input-capture capability with programmable trigger edge on input pin
 - Output-compare with programmable mode for the output pin
 - Free run and restart modes
 - Maskable interrupts and DMA trigger capability on input capture or output compare
- Software watchdog timer
 - 16-bit counter
 - Low-power mode support
- Two periodic interrupt timers (PITs)
 - 16-bit counter
 - Selectable as free running or count down
- Phase locked loop (PLL)
 - 16 MHz reference frequency
 - Programmable dithering

- Interrupt controller
 - Support for up to 63 interrupt sources
 - Unique vector number for each interrupt source
 - Ability to mask any individual interrupt source or all interrupt sources (global mask-all)
 - Support for hardware and software interrupt acknowledge (IACK) cycles
 - Combinatorial path to provide wake-up from low power modes
- DMA controller
 - 16 fully programmable channels with 32-byte transfer control
 - Data movement via dual-address transfers for 8-, 16-, 32-, and 128-bit data values
 - Programmable source and destination addresses, transfer size, and support for enhanced address modes
 - Support for major and minor nested counters with one request and one interrupt per channel
 - Support for channel-to-channel linking and scatter/gather for continuous transfers with fixed priority and round-robin channel arbitration
 - External request pins for a single channels
- FlexBus (external interface)
 - Glueless connections to 8-, 16-, or 32-bit external memory devices (SRAM, Flash, ROM, etc.)
 - Support for independent primary and secondary wait states per chip select
 - Programmable address setup and hold time with respect to chip select negation, per transfer direction
 - Glueless interface to SRAM devices with or without byte strobe inputs
 - Programmable wait state generator
 - 32-bit bidirectional data bus and 24-bit address bus
 - Up to six chip selects available
 - Byte/write enables (byte strobes)
 - Ability to boot from external memories that are 8, 16, or 32 bits wide
- Chip configuration module (CCM)
 - System configuration during reset
 - Unique part identification number and part revision number
- Reset controller
 - Separate reset in and reset out signals
 - Five reset sources: power-on reset (POR), external, software, watchdog, PLL loss of lock
 - Status flag indication of source of last reset
- General purpose I/O interface
 - Up to 30 bits of GPIO for the MCF5207
 - Up to 50 bits of GPIO for the MCF5208 (196 MAPBGA)
 - Up to 46 bits of GPIO for the MCF5208 (160 QFP)
 - Bit manipulation supported via set/clear functions

- Unused peripheral pins may be used as extra GPIO
- Programmable drive strength or slew rate control for related group of pins

1.3.1 V2 Core Overview

The processor core is comprised of two separate pipelines that are decoupled by an instruction buffer. The two-stage instruction fetch pipeline (IFP) is responsible for instruction-address generation and instruction fetch. The instruction buffer is a first-in-first-out (FIFO) buffer that holds prefetched instructions awaiting execution in the operand execution pipeline (OEP). The OEP includes two pipeline stages. The first stage decodes instructions and selects operands (DSOC); the second stage (AGEX) performs instruction execution and calculates operand effective addresses, if needed.

The V2 core implements the ColdFire instruction set architecture revision A+ with added support for a separate user stack pointer register and four new instructions to assist in bit processing. Additionally, the MCF5208 core includes the enhanced multiply-accumulate unit (EMAC) for improved signal processing capabilities. The EMAC implements a 4-stage execution pipeline, optimized for 32 x 32 bit operations, with support for four 48-bit accumulators. Supported operands include 16- and 32-bit signed and unsigned integers, as well as signed fractional operands, plus a complete set of instructions to process these data types. The EMAC provides superb support for execution of DSP operations within the context of a single processor at a minimal hardware cost.

The core also includes a hardware divide unit that performs a number of integer-divide operations. The supported divide functions include: 32-bit dividend and 16-bit divisor producing a 16-bit quotient and a 16-bit remainder, 32-bit dividend and 32-bit divisor producing a 32-bit quotient, and 32-bit dividend and 32-bit divisor producing a 32-bit remainder.

1.3.2 Debug Module

The ColdFire processor core debug interface is provided to support system debugging with low-cost debug and emulator development tools. Through a standard debug interface, you can access debug information. This allows the processor and system to be debugged without the need for costly in-circuit emulators.

The on-chip breakpoint resources include a total of nine programmable registers—a pair of upper and lower address registers, a pair of data registers (a 32-bit data register and a 32-bit data mask register), and four 32-bit PC registers plus a 32-bit PC mask register. These registers can be accessed through the dedicated debug serial communication channel or from the processor's supervisor mode programming model. The breakpoint registers can be configured to generate triggers by combining the address, data, and PC conditions in a variety of single or dual-level definitions. The trigger event can be programmed to generate a processor halt or initiate a debug interrupt exception.

To support program trace, the V3 Coldfire core's debug module provides processor status (PST[3:0]) and debug data (DDATA[3:0]) ports. These buses and the PSTCLK output provide execution status, captured operand data, and branch target addresses defining processor activity at one-half the CPU's clock rate.

The MCF5207L and MCF5208L contain an ALLPST signal in place of the PST and DDATA signals. It is the result of an AND operation of the four PST lines and signals when the processor has halted.

1.3.3 JTAG

The device supports circuit board test strategies based on the Test Technology Committee of IEEE and the Joint Test Action Group (JTAG). The test logic includes a test access port (TAP) consisting of a 16-state controller, an instruction register, and three test registers (a bypass register, a boundary-scan register, and an ID register). The boundary scan register links the device's pins into one shift register. Test logic, implemented using static logic design, is independent of the device system logic.

The implementation can do the following:

- Perform boundary-scan operations to test circuit board electrical continuity
- Sample device system pins during operation and transparently shift out the result in the boundary scan register
- Bypass the device for a given circuit board test by effectively reducing the boundary-scan register to a single bit
- Disable the output drive to pins during circuit-board testing
- Drive output pins to stable levels

1.3.4 On-chip Memories

1.3.4.1 Cache

The MCF5208 architecture includes a 8-Kbyte configurable cache. The 8-Kbyte cache can be configured into one of three possible organizations: an 8-Kbyte instruction cache, an 8-Kbyte data cache or a split 4-Kbyte instruction/4-Kbyte data cache. The configuration is software-programmable by control bits within the privileged Cache Configuration Register (CACR). In all configurations, the cache is a direct-mapped single-cycle memory, organized as 512 lines, each containing 16 bytes of data. The memories consist of a 512-entry tag array (containing addresses and control bits) and a 8-Kbyte data array, organized as 2048 x 32 bits.

If the desired address is mapped into the cache memory, the output of the data array is driven onto the ColdFire core's local data bus, completing the access in a single cycle. If the data is not mapped into the tag memory, a cache miss occurs and the processor core initiates a 16-byte line-sized fetch. The cache module includes a 16-byte line fill buffer used as temporary storage during miss processing. For all data cache configurations, the memory operates in write-through mode and all operand writes generate an external bus cycle.

1.3.4.2 SRAM

The SRAM module provides a general-purpose 16-Kbyte memory block that the ColdFire core can access in a single cycle. The memory is ideal for storing critical code or data structures or for use as the system stack. Because the SRAM module is physically connected to the processor's high-speed local bus, it can quickly service core-initiated accesses or memory-referencing commands from the debug module.

The dual-port SRAM module is also accessible by the DMA and FEC non-core bus masters through the crossbar switch. The dual-ported nature of the SRAM makes it ideal for implementing applications with double-buffer schemes, where the processor and a bus-mastering device operate in alternate regions of the

SRAM to maximize system performance. As an example, system performance can be increased significantly if Ethernet packets are moved from the FEC into the SRAM (rather than external memory) prior to any processing.

1.3.5 SDR/DDR SDRAM Controller

The SDRAM controller provides a glueless interface to SDR and DDR SDRAM memory devices. The module uses a 32-bit (for SDR) or a 16-bit (for DDR) memory port and can address up to 512 MB of data (256 MB per chip select). The controller supports DDR and SDR SDRAM, but both cannot be used at the same time.

1.3.6 Fast Ethernet Controller (FEC)

The device's integrated fast Ethernet controller (FEC) performs the full set of IEEE[®] 802.3/Ethernet CSMA/CD media access control and channel interface functions. The FEC supports connection and functionality for the 10/100 Mbps 802.3 media independent interface (MII). It requires an external transceiver (PHY) to complete the interface to the media.

1.3.7 UARTs

The device contains three independent, full-duplex UARTs. The three UARTs can be clocked by the system bus clock, eliminating the need for an externally supplied clock. They can use DMA requests on transmit-ready and receive-ready as well as interrupt requests for servicing.

1.3.8 I²C Bus

The I²C bus is a two-wire, bidirectional serial bus that provides an efficient method of data exchange, minimizing the interconnection between devices. This bus is suitable for applications requiring occasional communications over a short distance between many devices.

1.3.9 QSPI

The queued serial peripheral interface module provides a high-speed synchronous serial peripheral interface with queued transfer capability. It allows up to 16 transfers to be queued at once, eliminating CPU intervention between transfers.

1.3.10 DMA Timers (DTIM0-DTIM3)

There are four independent, DMA-transfer-generating 32-bit timers (DTIM[3:0]). Each timer module incorporates a 32-bit timer with a separate register set for configuration and control. The timers can be configured to operate from the system clock or from an external clock source using one of the DT_nIN signals. If the system clock is selected, it can be divided by 16 or 1. The input clock is further divided by a user-programmable 8-bit prescaler that clocks the actual timer counter register (TCR_n). Each of these timers can be configured for input-capture or output-compare mode. By configuring the internal registers,

each timer may be configured to assert an external pin, generate an interrupt on a particular event, or cause a DMA transfer.

1.3.11 Software Watchdog Timer

The watchdog timer is a 16-bit timer that facilitates recovery from runaway code. The watchdog counter is a free-running down-counter that generates a reset on underflow. To prevent a reset, software must periodically restart the countdown.

1.3.12 Periodic Interrupt Timers (PIT0–PIT1)

The two periodic interrupt timers (PIT[1:0]) are 16-bit timers that provide precise interrupts at regular intervals with minimal processor intervention. Each timer can count down from the value written in its PIT modulus register, or it can be a free-running down-counter.

1.3.13 Clock Module and Phase Locked Loop (PLL)

The device contains a 16 MHz crystal oscillator, a phase-locked loop, as well as status and control registers. The PLL's output dividers and dithering waveform are register programmable. The system operates via two main clocks generated by the PLL, typically 166.67 MHz (core) and 83.33 MHz (peripherals). To improve noise immunity, the PLL has its own power supply inputs, PLL_VDD and PLL_VSS. All other circuits are powered by the normal internal supply pins, IVDD (core), EVDD (I/O), SD_VDD (SDRAM), and VSS.

The PLL circuitry may be bypassed to reduce system speed and decrease power consumption. The external clock (EXTAL) is used directly, with an optional programmable divider, to produce the internal core and bus clocks.

1.3.14 Interrupt Controller

There is a single interrupt controller on the MCF5208, which can support up to 63 interrupt sources. Each interrupt source has a unique interrupt vector, and all sources of the controller provide a programmable level (1-7).

1.3.15 DMA Controller

The implementation of the DMA is targeted towards cost-sensitive applications while providing a high level of functionality. The DMA executes in parallel with the core, enabling transfers of data between the memory and peripherals with little intervention from the core, thus increasing system performance, as well as simplifying software development. The DMA is capable of performing complex data transfers via 16 programmable DMA channels. The hardware microarchitecture includes the DMA engine (which performs source/destination address calculations and data movement operations), and a dedicated memory array containing transfer control descriptors.

1.3.16 FlexBus External Interface

The FlexBus provides an external interface to 8-, 16-, or 32-bit memory devices (SRAM, flash, ROM, etc.). The FlexBus's internal data lines are shared with the SDRAM controller. When the SDRAMC is in DDR mode (DRAMSEL = 0) the data bus signals, D[31:16], are dedicated to the SDRAM controller and the D[15:0] data bus signals are dedicated to the FlexBus. In SDR mode (DRAMSEL = 1), all 32 data lines are shared between the FlexBus and SDRAM controller.

Features are available to support external flash modules and secondary wait states on reads and writes and a signal to support active-low address valid (\overline{TS}). Six programmable chip-select outputs provide signals to enable external memory and peripheral circuits, providing all handshaking and timing signals for automatic wait-state insertion and data bus sizing.

Base memory address and block size are programmable, with some restrictions. For example, the starting address must be on a boundary that is a multiple of the block size. Each chip select can be configured to provide read and write enable signals suitable for use with most popular static RAMs and peripherals. Data bus width (8-bit, 16-bit, or 32-bit) is programmable on all chip selects, and further decoding is available for protection from user mode access or read-only access.

1.3.17 Reset Controller Module

The reset controller is provided to determine the cause of reset, assert the appropriate reset signals to the system, and keep track of what caused the last reset. There are five sources of reset:

- External
- Power-on reset (POR)
- Watchdog timer
- Phase locked-loop (PLL) loss of lock
- Software

External reset on the \overline{RSTOUT} pin is software-assertable independent of chip reset state. There are also software-readable status flags indicating the cause of the last reset.

1.3.18 GPIO

Unused bus interface and peripheral pins can be used as discrete general-purpose inputs and outputs. These are managed by a dedicated GPIO module that logically groups all pins into ports located within a contiguous block of memory-mapped control registers. Each port has registers that configure, monitor, and control the port pins. Slew rate control or output pad drive strength control is available on all pins.

Most of the pins associated with the FlexBus interface may be used for several different functions. Their primary function is to provide an external interface to access off-chip resources. When not used for this, the pins may be used as general-purpose digital I/O pins.

1.4 Documentation

Documentation is available from a local Freescale distributor, a Freescale sales office, the Freescale Literature Distribution Center, or through the Freescale World Wide Web address at <http://www.freescale.com/coldfire>.

Chapter 2

Signal Descriptions

2.1 Introduction

This chapter describes the external signals on the device. It includes an alphabetical listing of signals that characterizes each signal as an input or output, defines its state at reset, and identifies whether a pull-up resistor should be used.

NOTE

The terms assertion and negation are used to avoid confusion when dealing with a mixture of active-low and active-high signals. The term asserted indicates that a signal is active, independent of the voltage level. The term negated indicates that a signal is inactive.

Active-low signals, such as $\overline{\text{SD_SRAS}}$ and $\overline{\text{TA}}$, are indicated with an overbar.

2.2 Signal Properties Summary

The below table lists the signals grouped by functionality.

NOTE

In this table and throughout this document, a single signal within a group is designated without square brackets (i.e., A23), while designations for multiple signals within a group use brackets (i.e., A[23:21]) and is meant to include all signals within the two bracketed numbers when these numbers are separated by a colon.

NOTE

The primary functionality of a pin is not necessarily its default functionality. Pins that are muxed with GPIO default to their GPIO functionality.

Table 2-1. MCF5207/8 Signal Information and Muxing

Signal Name	GPIO	Alternate 1	Alternate 2	Dir. ¹	Voltage Domain	MCF5207 144 LQFP	MCF5207 144 MAPBGA	MCF5208 160 QFP	MCF5208 196 MAPBGA
Reset									
$\overline{\text{RESET}}^2$	—	—	—	I	EVDD	82	J10	90	J14
$\overline{\text{RSTOUT}}$	—	—	—	O	EVDD	74	M12	82	N14

Table 2-1. MCF5207/8 Signal Information and Muxing (continued)

Signal Name	GPIO	Alternate 1	Alternate 2	Dir. ¹	Voltage Domain	MCF5207 144 LQFP	MCF5207 144 MAPBGA	MCF5208 160 QFP	MCF5208 196 MAPBGA
Clock									
EXTAL	—	—	—	I	EVDD	78	K12	86	L14
XTAL	—	—	—	O	EVDD	80	J12	88	K14
FB_CLK	—	—	—	O	SDVDD	34	L1	40	N1
Mode Selection									
$\overline{\text{RCON}}^2$	—	—	—	I	EVDD	144	C4	160	C3
DRAMSEL	—	—	—	I	EVDD	79	H10	87	K11
FlexBus									
A[23:22]	—	$\overline{\text{FB_CS}}[5:4]$	—	O	SDVDD	118, 117	B9, A10	126, 125	B11, A11
A[21:16]	—	—	—	O	SDVDD	116–114, 112, 108, 107	C9, A11, B10, A12, C11, B11	124, 123, 122, 120, 116, 115	B12, A12, A13, B13, B14, C13
A[15:14]	—	SD_BA[1:0] ³	—	O	SDVDD	106, 105	B12, C12	114, 113	C14, D12
A[13:11]	—	SD_A[13:11] ³	—	O	SDVDD	104–102	D11, E10, D12	112, 111, 110	D13, D14, E11
A10	—	—	—	O	SDVDD	101	C10	109	E12
A[9:0]	—	SD_A[9:0] ³	—	O	SDVDD	100–91	E11, D9, E12, F10, F11, E9, F12, G10, G12, F9	108–99	E13, E14, F11–F14, G11–G14
D[31:16]	—	SD_D[31:16] ⁴	—	I/O	SDVDD	21–28, 40–47	F1, F2, G1, G2, G4, G3, H1, H2, K3, L2, L3, K2, M3, J4, M4, K4	27–34, 46–53	J4–J1, K4–K1, M3, N3, M4, N4, P4, L5, M5, N5
D[15:0]	—	FB_D[31:16] ⁴	—	I/O	SDVDD	8–15, 51–58	B2, B1, C2, C1, D2, D1, E2, E1, L5, K5, L6, J6, M6, J7, L7, K7	16–23, 57–64	F3–F1, G4–G1, H1, N6, P6, L7, M7, N7, P7, N8, P8
$\overline{\text{BE/BWE}}[3:0]$	PBE[3:0]	$\overline{\text{SD_DQM}}[3:0]^3$	—	O	SDVDD	20, 48, 18, 50	F4, L4, E3, J5	26, 54, 24, 56	H2, P5, H4, M6
$\overline{\text{OE}}$	PBUSCTL3	—	—	O	SDVDD	60	J8	66	M8
$\overline{\text{TA}}^2$	PBUSCTL2	—	—	I	SDVDD	90	G11	98	H14
$\text{R}\overline{\text{W}}$	PBUSCTL1	—	—	O	SDVDD	59	K6	65	L8

Table 2-1. MCF5207/8 Signal Information and Muxing (continued)

Signal Name	GPIO	Alternate 1	Alternate 2	Dir. ¹	Voltage Domain	MCF5207 144 LQFP	MCF5207 144 MAPBGA	MCF5208 160 QFP	MCF5208 196 MAPBGA
\overline{TS}	PBUSCTL0	$\overline{DACK0}$	—	O	SDVDD	4	B3	12	E3
Chip Selects									
$\overline{FB_CS}[3:2]$	PCS[3:2]	—	—	O	SDVDD	119, 120	D7, A9	—	C11, A10
$\overline{FB_CS1}$	PCS1	$\overline{SD_CS1}$	—	O	SDVDD	121	C8	127	B10
$\overline{FB_CS0}$	—	—	—	O	SDVDD	122	B8	128	C10
SDRAM Controller									
SD_A10	—	—	—	O	SDVDD	37	M1	43	N2
SD_CKE	—	—	—	O	SDVDD	6	C3	14	E1
SD_CLK	—	—	—	O	SDVDD	31	J1	37	L1
$\overline{SD_CLK}$	—	—	—	O	SDVDD	32	K1	38	M1
$\overline{SD_CS0}$	—	—	—	O	SDVDD	7	A1	15	F4
SD_DQS[3:2]	—	—	—	O	SDVDD	19, 49	F3, M5	25, 55	H3, L6
$\overline{SD_SCAS}$	—	—	—	O	SDVDD	38	M2	44	P2
$\overline{SD_SRAS}$	—	—	—	O	SDVDD	39	J2	45	P3
SD_SDR_DQS	—	—	—	O	SDVDD	29	H3	35	L3
$\overline{SD_WE}$	—	—	—	O	SDVDD	5	D3	13	E2
External Interrupts Port⁵									
$\overline{IRQ7}^2$	PIRQ7 ²	—	—	I	EVDD	134	A5	142	C7
$\overline{IRQ4}^2$	PIRQ4 ²	$\overline{DREQ0}^2$	—	I	EVDD	133	C6	141	D7
$\overline{IRQ1}^2$	PIRQ1 ²	—	—	I	EVDD	132	B6	140	D8
FEC									
FEC_MDC	PFECI2C3	I2C_SCL ²	U2TXD	O	EVDD	—	—	148	D6
FEC_MDIO	PFECI2C2	I2C_SDA ²	U2RXD	I/O	EVDD	—	—	147	C6
FEC_TXCLK	PFECH7	—	—	I	EVDD	—	—	157	B3
—	PFECH6	—	$\overline{U1RTS}$	O	EVDD	142	A2	—	—
FEC_TXEN	PFECH6	—	$\overline{U1RTS}$	O	EVDD	—	—	158	A2
FEC_TXD0	PFECH5	—	—	O	EVDD	—	—	3	B1
FEC_COL	PFECH4	—	—	I	EVDD	—	—	7	D3
FEC_RXCLK	PFECH3	—	—	I	EVDD	—	—	154	B4
FEC_RXDV	PFECH2	—	—	I	EVDD	—	—	153	A4
FEC_RXD0	PFECH1	—	—	I	EVDD	—	—	152	D5

Table 2-1. MCF5207/8 Signal Information and Muxing (continued)

Signal Name	GPIO	Alternate 1	Alternate 2	Dir. ¹	Voltage Domain	MCF5207 144 LQFP	MCF5207 144 MAPBGA	MCF5208 160 QFP	MCF5208 196 MAPBGA
FEC_CRS	PFECH0	—	—	I	EVDD	—	—	8	D2
FEC_TXD[3:1]	PFECL[7:5]	—	—	O	EVDD	—	—	6–4	C1, C2, B2
—	PFECL4	—	$\overline{U0RTS}$	O	EVDD	141	D5	—	—
FEC_TXER	PFECL4	—	$\overline{U0RTS}$	O	EVDD	—	—	156	A3
FEC_RXD[3:2]	PFECL[3:2]	—	—	I	EVDD	—	—	149–150	A5, B5
—	PFECL1	—	$\overline{U1CTS}$	I	EVDD	139	B4	—	—
FEC_RXD1	PFECL1	—	$\overline{U1CTS}$	I	EVDD	—	—	151	C5
—	PFECL0	—	$\overline{U0CTS}$	I	EVDD	140	E4	—	—
FEC_RXER	PFECL0	—	$\overline{U0CTS}$	I	EVDD	—	—	155	C4
Note: The MCF5207 does not contain an FEC module. However, the UART0 and UART1 control signals (as well as their GPIO signals) are available by setting the appropriate FEC GPIO port registers.									
I²C									
I2C_SDA ²	PFECI2C0 ²	U2RXD ²	—	I/O	EVDD	—	—	—	D1
I2C_SCL ²	PFECI2C1 ²	U2TXD ²	—	I/O	EVDD	—	—	—	E4
DMA									
$\overline{DACK0}$ and $\overline{DREQ0}$ do not have a dedicated bond pads. Please refer to the following pins for muxing: \overline{TS} and QSPI_CS2 for $\overline{DACK0}$, $\overline{IRQ4}$ and QSPI_DIN for $\overline{DREQ0}$.									
QSPI									
QSPI_CS2	PQSPI3	$\overline{DACK0}$	$\overline{U2RTS}$	O	EVDD	126	A8	132	D10
QSPI_CLK	PQSPI0	I2C_SCL ²	—	O	EVDD	127	C7	133	A9
QSPI_DOUT	PQSPI1	I2C_SDA ²	—	O	EVDD	128	A7	134	B9
QSPI_DIN	PQSPI2	$\overline{DREQ0}$ ²	$\overline{U2CTS}$	I	EVDD	129	B7	135	C9
Note: The QSPI_CS1 and QSPI_CS0 signals are available on the $\overline{U1CTS}$, $\overline{U1RTS}$, $\overline{U0CTS}$, or $\overline{U0RTS}$ pins for the 196 and 160-pin packages.									
UARTs									
$\overline{U1CTS}$	PUARTL7	DT1IN	QSPI_CS1	I	EVDD	—	—	136	D9
$\overline{U1RTS}$	PUARTL6	DT1OUT	QSPI_CS1	O	EVDD	—	—	137	C8
U1TXD	PUARTL5	—	—	O	EVDD	131	A6	139	A8
U1RXD	PUARTL4	—	—	I	EVDD	130	D6	138	B8
$\overline{U0CTS}$	PUARTL3	DT0IN	QSPI_CS0	I	EVDD	—	—	76	N12
$\overline{U0RTS}$	PUARTL2	DT0OUT	QSPI_CS0	O	EVDD	—	—	77	P12
U0TXD	PUARTL1	—	—	O	EVDD	71	L10	79	P13

Table 2-1. MCF5207/8 Signal Information and Muxing (continued)

Signal Name	GPIO	Alternate 1	Alternate 2	Dir. ¹	Voltage Domain	MCF5207 144 LQFP	MCF5207 144 MAPBGA	MCF5208 160 QFP	MCF5208 196 MAPBGA
U0RXD	PUARTL0	—	—	I	EVDD	70	M10	78	N13
Note: The UART2 signals are multiplexed on the DMA Timers, QSPI, FEC, and I2C pins. For the MCF5207 devices, the UART0 and UART1 control signals are multiplexed internally on the FEC signals.									
DMA Timers									
DT3IN	PTIMER3	DT3OUT	$\overline{U2CTS}$	I	EVDD	135	B5	143	B7
DT2IN	PTIMER2	DT2OUT	$\overline{U2RTS}$	I	EVDD	136	C5	144	A7
DT1IN	PTIMER1	DT1OUT	U2RXD	I	EVDD	137	A4	145	A6
DT0IN	PTIMER0	DT0OUT	U2TXD	I	EVDD	138	A3	146	B6
BDM/JTAG⁶									
JTAG_EN ⁷	—	—	—	I	EVDD	83	J11	91	J13
DSCLK	—	\overline{TRST}^2	—	I	EVDD	76	K11	84	L12
PSTCLK	—	TCLK ²	—	O	EVDD	64	M7	70	P9
\overline{BKPT}	—	TMS ²	—	I	EVDD	75	L12	83	M14
DSI	—	TDI ²	—	I	EVDD	77	H9	85	K12
DSO	—	TDO	—	O	EVDD	69	M9	75	M12
DDATA[3:0]	—	—	—	O	EVDD	—	K9, L9, M11, M8	—	P11, N11, M11, P10
PST[3:0]	—	—	—	O	EVDD	—	L11, L8, K10, K8	—	N10, M10, L10, L9
ALLPST	—	—	—	O	EVDD	67	—	73	—
Test									
TEST ⁷	—	—	—	I	EVDD	109	—	—	C12
PLL_TEST	—	—	—	I	EVDD	—	—	—	M13
Power Supplies									
EVDD	—	—	—	—	—	1, 33, 63, 66, 72, 81, 87, 125	E5–E6, F5, G8–G9, H7–H8	2, 9, 69, 72, 80, 89, 95, 131	E5–E7, F5, F6, G5, H10, J9, J10, K8–K10, K13, M9
IVDD	—	—	—	—	—	30, 68, 84, 113, 143	D4, D8, H4, H11, J9	36, 74, 92, 121, 159	J12, D4, D11, H11, L4, L11,
PLL_VDD	—	—	—	—	—	86	H12	94	H13

Table 2-1. MCF5207/8 Signal Information and Muxing (continued)

Signal Name	GPIO	Alternate 1	Alternate 2	Dir. ¹	Voltage Domain	MCF5207 144 LQFP	MCF5207 144 MAPBGA	MCF5208 160 QFP	MCF5208 196 MAPBGA
SD_VDD	—	—	—	—	—	3, 17, 35, 61, 89, 110, 123	E7–E8, F8, G5, H5–H6, J3	11, 39, 41, 67, 97, 118, 129	E8–E10, F9, F10, G10, H5, J5, J6, K5–K7, L2
VSS	—	—	—	—	—	2, 16, 36, 62, 65, 73, 88, 111, 124	D10, F6–F7, G6–G7	1, 10, 42, 68, 71, 81, 96, 117, 119, 130	A1, A14, F7–F8, G6–G9, H6–H9, J7–J8, L13, M2, N9, P1, P14
PLL_VSS	—	—	—	—	—	85	—	93	H12

¹ Refers to pin's primary function.

² Pull-up enabled internally on this signal for this mode.

³ The SDRAM functions of these signals are not programmable by the user. They are dynamically switched by the processor when accessing SDRAM memory space and are included here for completeness.

⁴ Primary functionality selected by asserting the DRAMSEL signal (SDR mode). Alternate functionality selected by negating the DRAMSEL signal (DDR mode). The GPIO module is not responsible for assigning these pins.

⁵ GPIO functionality is determined by the edge port module. The GPIO module is only responsible for assigning the alternate functions.

⁶ If JTAG_EN is asserted, these pins default to Alternate 1 (JTAG) functionality. The GPIO module is not responsible for assigning these pins.

⁷ Pull-down enabled internally on this signal for this mode.

2.2.1 Internal Pull-up/Pull-downs Resistors

The following table summarizes which external signals contain internal pull-up or pull-down resistors.

Table 2-2. Internal Pull-up/down Resistors

Pin Name	Pull-Up	Pull-Down	Comment
$\overline{\text{RESET}}$	x		Always, except JTAG mode
TEST		x	Always, except JTAG mode
$\overline{\text{RCON}}$	x		Always, except JTAG mode
$\overline{\text{IRQ}}[7,4,1]$	x		All modes
$\overline{\text{TA}}$	x		Only when used as $\overline{\text{TA}}$
QSPI_DIN	x		DMA mode only ($\overline{\text{DREQ0}}$)
QSPI_DOUT	x		I ² C mode only (I2C_SDA)
QSPI_CLK	x		I ² C mode only (I2C_SCL)
FEC_MDIO	x		I ² C mode only (I2C_SDA)

Table 2-2. Internal Pull-up/down Resistors (continued)

Pin Name	Pull-Up	Pull-Down	Comment
FEC_MDC	x		I ² C mode only (I2C_SCL)
I2C_SDA	x		I ² C mode only (I2C_SDA)
I2C_SCL	x		I ² C mode only (I2C_SCL)
JTAG_EN		x	
TDI	x		JTAG mode only
TMS	x		JTAG mode only
$\overline{\text{TRST}}$	x		JTAG mode only
TCLK	x		JTAG mode only
D0	x		During reset only

2.3 Signal Primary Functions

2.3.1 Reset Signals

Table 2-3 describes signals that are used to reset the chip or as a reset indication.

Table 2-3. Reset Signals

Signal Name	Abbreviation	Function	I/O
Reset In	$\overline{\text{RESET}}$	Primary reset input to the device. Asserting $\overline{\text{RESET}}$ immediately resets the core and peripherals, which stay in reset until $\overline{\text{RESET}}$ is negated.	I
Reset Out	$\overline{\text{RSTOUT}}$	Reset output ($\overline{\text{RSTOUT}}$) is an indicator that the chip is in reset. $\overline{\text{RSTOUT}}$ is driven low for 512 FB_CLK clock cycles in response to any internal or external reset.	O

2.3.2 PLL and Clock Signals

Table 2-4 describes signals that are used to support the on-chip clock generation circuitry.

Table 2-4. PLL and Clock Signals

Signal Name	Abbreviation	Function	I/O
External Clock In	EXTAL	Always driven by an external clock input except when used as a connection to the external crystal when the internal oscillator circuit is used. The clock source may be configured during reset by asserting $\overline{\text{RCON}}$. See Chapter 9, “Chip Configuration Module (CCM)” for more details.	I
Crystal	XTAL	Used as a connection to the external crystal when the internal oscillator circuit is used to drive the crystal.	O
FlexBus Clock Out	FB_CLK	Reflects the internal bus clock (or one-half the core/system clock). ($f_{\text{sys}}/2$)	O

2.3.3 Mode Selection

Table 2-5 describes signals used in mode selection.

Table 2-5. Mode Selection Signals

Signal Name	Abbreviation	Function	I/O
Reset Configuration	$\overline{\text{RCON}}$	Indicates whether the external D[15:0] pin states affect chip configuration at reset.	I
SDR/DDR SDRAM Select	DRAMSEL	Controls whether certain pins act as FlexBus or SDRAMC signals. When asserted, D[31:0] dynamically switches between SDR data and FlexBus data. When negated, D[31:16] are dedicated for DDR data while D[15:0] are dedicated for FlexBus data.	I

2.3.4 FlexBus Signals

Table 2-6 describes signals that are used for doing transactions on the external bus.

Table 2-6. FlexBus Signals

Signal Name	Abbreviation	Function	I/O
Address Bus	A[23:0]	The 24 dedicated address signals define the address of external byte, word, and longword accesses. These three-state outputs are the 24 lsbs of the internal 32-bit address bus and multiplexed with the SDRAM controller row and column addresses.	O
Data Bus	D[31:0]	These three-state bidirectional signals provide the general purpose data path between the processor and all other devices.	I/O
Byte Enables	$\overline{\text{BE/BWE}}[3:0]$	<p>Define the flow of data on the data bus. During peripheral accesses, these output signals indicate that data is to be latched or driven onto a byte of the data when driven low. The $\overline{\text{BE/BWE}}[3:0]$ signals are asserted only to the memory bytes used during a read or write access. $\overline{\text{BE/BWE}}_0$ controls access to the most significant byte lane of data, and $\overline{\text{BE/BWE}}_3$ controls access to the least significant byte lane of data.</p> <p>For SRAM or Flash devices, the $\overline{\text{BE/BWE}}_n$ outputs should be connected to individual byte strobe signals.</p> <p>The $\overline{\text{BE/BWE}}_n$ signals are asserted during accesses to on-chip peripherals, but not to on-chip SRAM or cache. During SDRAM accesses, these signals act as the SD_DQM[3:0] signals, which indicate a byte transfer between SDRAM and the chip when driven high. See Table 2-7 for more details.</p>	O
Output Enable	$\overline{\text{OE}}$	Indicates when an external device can drive data during external read cycles.	O
Transfer Acknowledge	$\overline{\text{TA}}$	Indicates that the external data transfer is complete. During a read cycle, when the processor recognizes $\overline{\text{TA}}$, it latches the data and then terminates the bus cycle. During a write cycle, when the processor recognizes $\overline{\text{TA}}$, the bus cycle is terminated.	I

Table 2-6. FlexBus Signals (continued)

Signal Name	Abbreviation	Function	I/O
Read/Write	R/\overline{W}	Indicates the direction of the data transfer on the bus for SRAM (R/\overline{W}) accesses. A logic 1 indicates a read from a slave device and a logic 0 indicates a write to a slave device.	O
Transfer Start	\overline{TS}	Bus control output signal indicating the start of a transfer.	O
Chip Selects	$\overline{FB_CS}[5:0]$	These output signals select external devices for external bus transactions.	O

2.3.5 SDRAM Controller Signals

Table 2-7 describes signals that are used for SDRAM accesses.

Table 2-7. SDRAM Controller Signals

Signal Name	Abbreviation	Function	I/O
SDRAM A10	SD_A10	Bit 10 of the SDRAM Address bus	O
SDRAM Clock Enable	SD_CKE	SDRAM clock enable.	O
DDR SDRAM Clock	SD_CLK	Output clock for DDR SDRAM.	O
DDR SDRAM Clock	$\overline{SD_CLK}$	Inverted output clock for DDR SDRAM.	O
SDRAM Chip Selects	$\overline{SD_CS}[1:0]$	SDRAM chip select signals.	O
DDR SDRAM Data Strobes	SD_DQS[3:2]	Indicates when valid data is on the data bus. SD_DQS1 is tied to SD_DQS3 and SD_DQS0 is tied to SD_DQS2 internally.	I/O
SDR SDRAM Write Data Byte Mask	SD_DQM[3:0]	Used to determine which byte lanes of the data bus should be latched during a write cycle. These pins are multiplexed with the $\overline{BE/BWEn}$ pins. The SD_DQM n should be connected to individual SDRAM DQM signals. Most SDRAMs associate DQM3 with the MSB, in which case SD_DQM3 should be connected to the SDRAM's DQM3 input.	O
SDRAM Synchronous Column Address Strobe	$\overline{SD_SCAS}$	SDRAM synchronous column address strobe.	O
SDRAM Synchronous Row Address Strobe	$\overline{SD_SRAS}$	SDRAM synchronous row address strobe.	O
SDR SDRAM Data Strobe	SD_SDRDQS	Generated by the memory controller in SDR mode, to mimic the DQS generated by DDR memories during reads. It is routed out and connected back to SD_DQS inputs.	O
SDRAM Write Enable	$\overline{SD_WE}$	Indicates the direction of the data transfer on the bus for SDRAM accesses. A logic 1 indicates a read from a slave device and a logic 0 indicates a write to a slave device.	O

2.3.6 External Interrupt Signals

Table 2-8 describes the external interrupt signals.

Table 2-8. External Interrupt Signals

Signal Name	Abbreviation	Function	I/O
External Interrupts	$\overline{\text{IRQ}}[7,4,1]$	External interrupt sources.	I

2.3.7 DMA Signals

Table 2-9 describes the external DMA signals.

Table 2-9. DMA Signals

Signal Name	Abbreviation	Function	I/O
DMA Request	$\overline{\text{DREQ0}}$	Active low external DMA request lines.	I
DMA Acknowledge	$\overline{\text{DACK0}}$	Active low external DMA acknowledge lines.	O

2.3.8 Ethernet Module (FEC) Signals

The following signals are used by the Ethernet module for data and clock signals.

Table 2-10. Ethernet Module (FEC) Signals

Signal Name	Abbreviation	Function	I/O
Management Data	FEC_MDIO	Transfers control information between the external PHY and the media-access controller. Data is synchronous to FEC_MDC. Applies to MII mode operation. This signal is an input after reset. When the FEC is operated in 10Mbps 7-wire interface mode, this signal should be connected to VSS.	I/O
Management Data Clock	FEC_MDC	In Ethernet mode, FEC_MDC is an output clock which provides a timing reference to the PHY for data transfers on the FEC_MDIO signal. Applies to MII mode operation.	O
Collision	FEC_COL	Asserted upon detection of a collision and remains asserted while the collision persists. This signal is not defined for full-duplex mode.	I
Carrier Receive Sense	FEC_CRs	When asserted, indicates that transmit or receive medium is not idle. Applies to MII mode operation.	I
Transmit Clock	FEC_TXCLK	Input clock which provides a timing reference for FEC_TXEN, FEC_TXD[3:0] and FEC_TXER	I
Transmit Enable	FEC_TXEN	Indicates when valid nibbles are present on the MII. This signal is asserted with the first nibble of a preamble and is negated before the first FEC_TXCLK following the final nibble of the frame.	O
Transmit Data 0	FEC_TXD0	FEC_TXD0 is the serial output Ethernet data and is only valid during the assertion of FEC_TXEN. This signal is used for 10-Mbps Ethernet data. It is also used for MII mode data in conjunction with FEC_TXD[3:1].	O
Transmit Data 1–3	FEC_TXD[3:1]	In Ethernet mode, these pins contain the serial output Ethernet data and are valid only during assertion of FEC_TXEN in MII mode.	O

Table 2-10. Ethernet Module (FEC) Signals (continued)

Signal Name	Abbreviation	Function	I/O
Transmit Error	FEC_TXER	In Ethernet mode, when FEC_TXER is asserted for one or more clock cycles while FEC_TXEN is also asserted, the PHY sends one or more illegal symbols. FEC_TXER has no effect at 10 Mbps or when FEC_TXEN is negated. Applies to MII mode operation.	O
Receive Clock	FEC_RXCLK	Provides a timing reference for FEC_RXDV, FEC_RXD[3:0], and FEC_RXER.	I
Receive Data Valid	FEC_RXDV	Asserting the FEC_RXDV input indicates that the PHY has valid nibbles present on the MII. FEC_RXDV should remain asserted from the first recovered nibble of the frame through to the last nibble. Assertion of FEC_RXDV must start no later than the SFD and exclude any EOF.	I
Receive Data 0	FEC_RXD0	FEC_RXD0 is the Ethernet input data transferred from the PHY to the media-access controller when FEC_RXDV is asserted. This signal is used for 10-Mbps Ethernet data. This signal is also used for MII mode Ethernet data in conjunction with FEC_RXD[3:1].	I
Receive Data 1–3	FEC_RXD[3:1]	In Ethernet mode, these pins contain the Ethernet input data transferred from the PHY to the media access controller when FEC_RXDV is asserted in MII mode operation.	I
Receive Error	FEC_RXER	In Ethernet mode, FEC_RXER—when asserted with FEC_RXDV—indicates that the PHY has detected an error in the current frame. When FEC_RXDV is not asserted FEC_RXER has no effect. Applies to MII mode operation.	I

2.3.9 I²C I/O Signals

Table 2-11 describes the I²C serial interface module signals.

Table 2-11. I²C I/O Signals

Signal Name	Abbreviation	Function	I/O
Serial Clock	I2C_SCL	Open-drain clock signal for the I ² C interface. It is driven by the I ² C module when the bus is in the master mode or it becomes the clock input when the I ² C is in the slave mode.	I/O
Serial Data	I2C_SDA	Open-drain signal that serves as the data input/output for the I ² C interface.	I/O

2.3.10 Queued Serial Peripheral Interface (QSPI)

Table 2-12 describes QSPI signals.

Table 2-12. Queued Serial Peripheral Interface (QSPI) Signals

Signal Name	Abbreviation	Function	I/O
QSPI Synchronous Serial Output	QSPI_DOUT	Provides the serial data from the QSPI and can be programmed to be driven on the rising or falling edge of QSPI_CLK. Each byte is sent msb first.	O
QSPI Synchronous Serial Data Input	QSPI_DIN	Provides the serial data to the QSPI and can be programmed to be sampled on the rising or falling edge of QSPI_CLK. Each byte is written to RAM lsb first.	I
QSPI Serial Clock	QSPI_CLK	Provides the serial clock from the QSPI. The polarity and phase of QSPI_CLK are programmable. The output frequency is programmed according to the following formula, in which n can be any value between 1 and 255: $\text{SPI_CLK} = f_{\text{sys}/2} \div (2 \times n)$	O
Synchronous Peripheral Chip Selects	QSPI_CS[2:0]	Provide QSPI peripheral chip selects that can be programmed to be active high or low.	O

2.3.11 UART Module Signals

Table 2-13 describes the signals of the three UART modules, where $n=0-2$. Baud rate clock inputs are not supported.

Table 2-13. UART Module Signals

Signal Name	Abbreviation	Function	I/O
Transmit Serial Data Output	$\overline{U}n\text{TXD}$	Transmitter serial data outputs. Data is shifted out lsb first on this pin at the falling edge of the serial clock source. The output is held high when the transmitter is disabled, idle, or in local loopback mode.	O
Receive Serial Data Input	$\overline{U}n\text{RXD}$	Receiver serial data inputs. Data is sampled on the rising edge of the serial clock source lsb first. When the UART clock is stopped for power-down mode, any transition on this pin restarts it.	I
Clear-to-Send	$\overline{U}n\text{CTS}$	Indicates that the UART modules can begin data transmission	I
Request-to-Send	$\overline{U}n\text{RTS}$	Automatic request-to-send outputs from the UART modules. They may also be asserted and negated as a function of the receive FIFO level.	O

2.3.12 DMA Timer Signals

Table 2-14 describes the signals of the four DMA timer modules, where $n=0-3$.

Table 2-14. DMA Timer Signals

Signal Name	Abbreviation	Function	I/O
DMA Timer n Input	DT n IN	Can be programmed to cause events to occur in the respective timer. It can clock the event counter or provide a trigger to the timer value capture logic.	I
DMA Timer n Output	DT n OUT	The output from the respective timer.	O

2.3.13 Debug Support Signals

These signals are used as the interface to the on-chip JTAG controller and the BDM logic. Pin functionality between JTAG and BDM is dependent upon the JTAG_EN pin.

Table 2-15. Debug Support Signals

Signal Name	Abbreviation	Function	I/O
Test Reset	$\overline{\text{TRST}}$	This active-low signal is used to initialize the JTAG logic asynchronously.	I
Test Clock	TCLK	Used to synchronize the JTAG logic.	I
Test Mode Select	TMS	Used to sequence the JTAG state machine. TMS is sampled on the rising edge of TCLK.	I
Test Data Input	TDI	Serial input for test instructions and data. TDI is sampled on the rising edge of TCLK.	I
Test Data Output	TDO	Serial output for test instructions and data. TDO is three-stateable and is actively driven in the shift-IR and shift-DR controller states. TDO changes on the falling edge of TCLK.	O
Development Serial Clock	DSCLK	Clocks the serial communication port to the BDM module during packet transfers.	I
Breakpoint	$\overline{\text{BKPT}}$	Used to request a manual breakpoint.	I
Development Serial Input	DSI	This internally-synchronized signal provides data input for the serial communication port to the BDM module.	I
Development Serial Output	DSO	This internally-registered signal provides serial output communication for BDM module responses.	O
Processor Status Clock	PSTCLK	Used by the development system to know when to sample the DDATA and PST signals.	O
Debug Data	DDATA[3:0]	Display captured processor data and breakpoint status. The PSTCLK signal can be used by the development system to know when to sample DDATA[3:0]. Only present on the BGA devices (MCF5208CVM and MCF5207CVM).	O
Processor Status Outputs	PST[3:0]	Indicate core status, as shown in Table 2-16 . Debug mode timing is synchronous with the processor clock; status is unrelated to the current bus transfer. The PSTCLK signal can be used by the development system to know when to sample PST[3:0]. Only present on the BGA devices (MCF5208CVM and MCF5207CVM).	O
All Processor Status Outputs	ALLPST	ALLPST is a logical 'AND' of the four PST signals and is present in place of PST[3:0] and DDATA[3:0] on the QFP devices (MCF5207CABxxx and MCF5208CABxxx). When asserted, reflects that the core is halted.	O

Table 2-16. Processor Status

PST[3:0] (BGA Devices)	ALLPST (QFP Devices)	Processor Status
0000	0	Continue execution
0001	0	Begin execution of one instruction
0010	0	Reserved
0011	0	Entry into user mode
0100	0	Begin execution of PULSE and WDDATA instructions
0101	0	Begin execution of taken branch
0110	0	Reserved
0111	0	Begin execution of RTE instruction
1000	0	Begin one-byte transfer on DDATA
1001	0	Begin two-byte transfer on DDATA
1010	0	Begin three-byte transfer on DDATA
1011	0	Begin four-byte transfer on DDATA
1100	0	Exception processing
1101	0	Reserved
1110	0	Processor is stopped
1111	1	Processor is halted

2.3.14 Test Signals

Table 2-17 describes test signals which are reserved for factory testing.

Table 2-17. Test Signals

Signal Name	Abbreviation	Function	I/O
Test	TEST	Reserved for factory testing only and in normal modes of operation should be connected to VSS to prevent unintentional activation of test functions.	I
PLL Test	PLL_TEST	Reserved for factory testing only and should be treated as a no-connect (NC).	O

2.3.15 Power and Ground Pins

The pins described in Table 2-18 provide system power and ground to the chip. Multiple pins are provided for adequate current capability. All power supply pins must have adequate bypass capacitance for high-frequency noise suppression.

Table 2-18. Power and Ground Pins

Signal Name	Abbreviation	Function	I/O
PLL Analog Supply	PLL_VDD PLL_VSS	Dedicated power supply signals to isolate the sensitive PLL analog (VCO) circuitry from the normal levels of noise present on the digital power supply.	—
Positive I/O Supply	EVDD	These pins supply positive power to the I/O pads.	—
Positive Core Supply	IVDD	These pins supply positive power to the core logic.	—
SDRAMC Supply	SD_VDD	These pins supply positive power to the SDRAM controller.	—
USB Supply	USB_VDD	These pins supply positive power to the USB controllers.	—
USB Ground	USB_VSS	These pins are the negative supply (ground) for the USB controllers.	—
Ground	VSS	These pins are the negative supply (ground) for the device.	—

2.4 External Boot Mode

After reset, the address bus, data bus, FlexBus control signals, and SDRAM control signals default to their bus functionalities. All other signals default to GPIO inputs (if applicable).

Chapter 3 ColdFire Core

3.1 Introduction

This section describes the organization of the Version 2 (V2) ColdFire[®] processor core and an overview of the program-visible registers. For detailed information on instructions, see the ISA_A+ definition in the *ColdFire Family Programmer's Reference Manual*.

3.1.1 Overview

As with all ColdFire cores, the V2 ColdFire core is comprised of two separate pipelines decoupled by an instruction buffer.

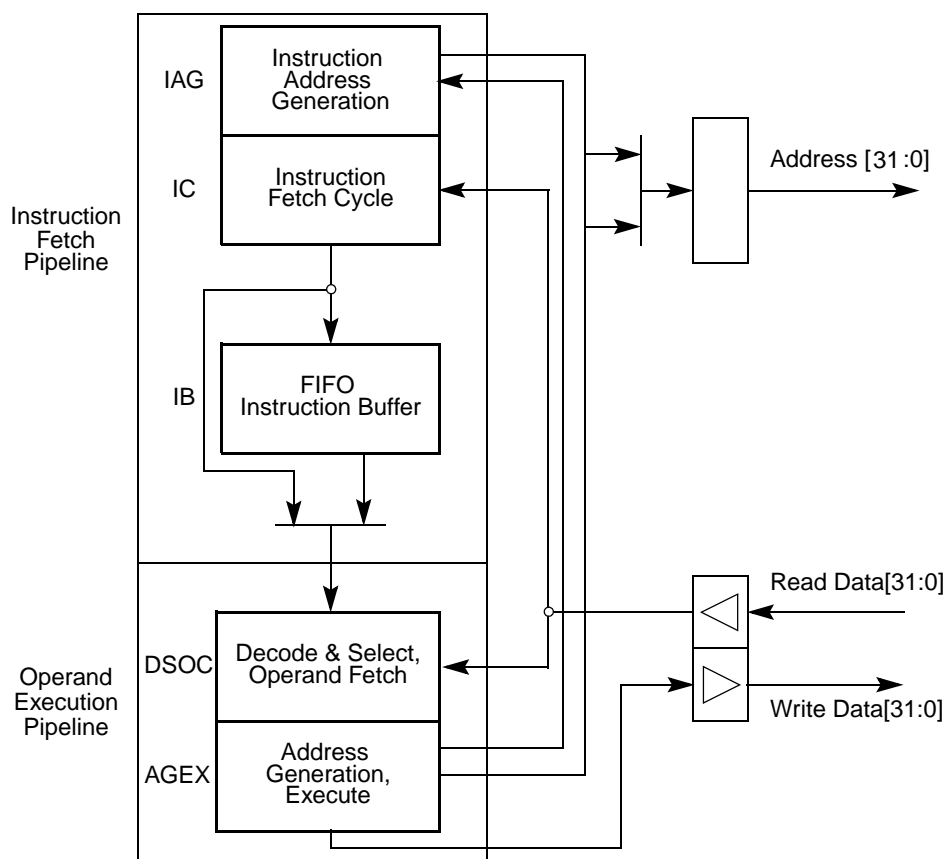


Figure 3-1. V2 ColdFire Core Pipelines

The instruction fetch pipeline (IFP) is a two-stage pipeline for prefetching instructions. The prefetched instruction stream is then gated into the two-stage operand execution pipeline (OEP), which decodes the

instruction, fetches the required operands and then executes the required function. Because the IFP and OEP pipelines are decoupled by an instruction buffer serving as a FIFO queue, the IFP is able to prefetch instructions in advance of their actual use by the OEP thereby minimizing time stalled waiting for instructions.

The V2 ColdFire core pipeline stages include the following:

- Two-stage instruction fetch pipeline (IFP) (plus optional instruction buffer stage)
 - Instruction address generation (IAG) — Calculates the next prefetch address
 - Instruction fetch cycle (IC)—Initiates prefetch on the processor's local bus
 - Instruction buffer (IB) — Optional buffer stage minimizes fetch latency effects using FIFO queue
- Two-stage operand execution pipeline (OEP)
 - Decode and select/operand fetch cycle (DSOC)—Decodes instructions and fetches the required components for effective address calculation, or the operand fetch cycle
 - Address generation/execute cycle (AGEX)—Calculates operand address or executes the instruction

When the instruction buffer is empty, opcodes are loaded directly from the IC cycle into the operand execution pipeline. If the buffer is not empty, the IFP stores the contents of the fetched instruction in the IB until it is required by the OEP.

For register-to-register and register-to-memory store operations, the instruction passes through both OEP stages once. For memory-to-register and read-modify-write memory operations, an instruction is effectively staged through the OEP twice: the first time to calculate the effective address and initiate the operand fetch on the processor's local bus, and the second time to complete the operand reference and perform the required function defined by the instruction.

The resulting pipeline and local bus structure allow the V2 ColdFire core to deliver sustained high performance across a variety of demanding embedded applications.

3.2 Memory Map/Register Description

The following sections describe the processor registers in the user and supervisor programming models. The programming model is selected based on the processor privilege level (user mode or supervisor mode) as defined by the S bit of the status register (SR). [Table 3-1](#) lists the processor registers.

The user-programming model consists of the following registers:

- 16 general-purpose 32-bit registers (D0–D7, A0–A7)
- 32-bit program counter (PC)
- 8-bit condition code register (CCR)
- EMAC registers (described fully in [Chapter 4, “Enhanced Multiply-Accumulate Unit \(EMAC\)”](#)):
 - Four 48-bit accumulator registers partitioned as follows:
 - Four 32-bit accumulators (ACC0–ACC3)
 - Eight 8-bit accumulator extension bytes (two per accumulator). These are grouped into two 32-bit values for load and store operations (ACCEXT01 and ACCEXT23).

Accumulators and extension bytes can be loaded, copied, and stored, and results from EMAC arithmetic operations generally affect the entire 48-bit destination.

- One 16-bit mask register (MASK)
- One 32-bit Status register (MACSR) including four indicator bits signaling product or accumulation overflow (one for each accumulator: PAV0–PAV3)

The supervisor programming model is to be used only by system control software to implement restricted operating system functions, I/O control, and memory management. All accesses that affect the control features of ColdFire processors are in the supervisor programming model, which consists of registers available in user mode as well as the following control registers:

- 16-bit status register (SR)
- 32-bit supervisor stack pointer (SSP)
- 32-bit vector base register (VBR)
- 32-bit cache control register (CACR)
- 32-bit access control registers (ACR0, ACR1)
- One 32-bit memory base address register (RAMBAR)

Table 3-1. ColdFire Core Programming Model

BDM ¹	Register	Width (bits)	Access	Reset Value	Written with MOVEC	Section/Page
Supervisor/User Access Registers						
Load: 0x080 Store: 0x180	Data Register 0 (D0)	32	R/W	0xCF20_60	No	3.2.1/3-4
Load: 0x081 Store: 0x181	Data Register 1 (D1)	32	R/W	0x1500_1060	No	3.2.1/3-4
Load: 0x082–7 Store: 0x182–7	Data Register 2–7 (D2–D7)	32	R/W	Undefined	No	3.2.1/3-4
Load: 0x088–8E Store: 0x188–8E	Address Register 0–6 (A0–A6)	32	R/W	Undefined	No	3.2.2/3-4
Load: 0x08F Store: 0x18F	Supervisor/User A7 Stack Pointer (A7)	32	R/W	Undefined	No	3.2.3/3-5
0x804	MAC Status Register (MACSR)	32	R/W	0x0000_0000	No	4.2.1/4-3
0x805	MAC Address Mask Register (MASK)	32	R/W	0xFFFF_FFFF	No	4.2.2/4-5
0x806, 0x809, 0x80A, 0x80B	MAC Accumulators 0–3 (ACC0–3)	32	R/W	Undefined	No	4.2.3/4-6
0x807	MAC Accumulator 0,1 Extension Bytes (ACCext01)	32	R/W	Undefined	No	4.2.4/4-7
0x808	MAC Accumulator 2,3 Extension Bytes (ACCext23)	32	R/W	Undefined	No	4.2.4/4-7
0x80E	Condition Code Register (CCR)	8	R/W	Undefined	No	3.2.4/3-6

Table 3-1. ColdFire Core Programming Model (continued)

BDM ¹	Register	Width (bits)	Access	Reset Value	Written with MOVEC	Section/Page
0x80F	Program Counter (PC)	32	R/W	Contents of location 0x0000_0004	No	3.2.5/3-7
Supervisor Access Only Registers						
0x002	Cache Control Register (CACR)	32	R/W	0x0000_0000	Yes	3.2.6/3-7
0x004–5	Access Control Register 0–1 (ACR0–1)	32	R/W	See Section	Yes	3.2.7/3-7
0x800	User/Supervisor A7 Stack Pointer (OTHER_A7)	32	R/W	Contents of location 0x0000_0000	No	3.2.3/3-5
0x801	Vector Base Register (VBR)	32	R/W	0x0000_0000	Yes	3.2.8/3-7
0x80E	Status Register (SR)	16	R/W	0x27--	No	3.2.9/3-8
0xC05	RAM Base Address Register (RAMBAR)	32	R/W	See Section	Yes	3.2.10/3-8

¹ The values listed in this column represent the Rc field used when accessing the core registers via the BDM port. For more information see [Chapter 26, “Debug Module”](#).

3.2.1 Data Registers (D0–D7)

D0–D7 data registers are for bit (1-bit), byte (8-bit), word (16-bit) and longword (32-bit) operations; they can also be used as index registers.

NOTE

Registers D0 and D1 contain hardware configuration details after reset. See [Section 3.3.4.15, “Reset Exception”](#) for more details.

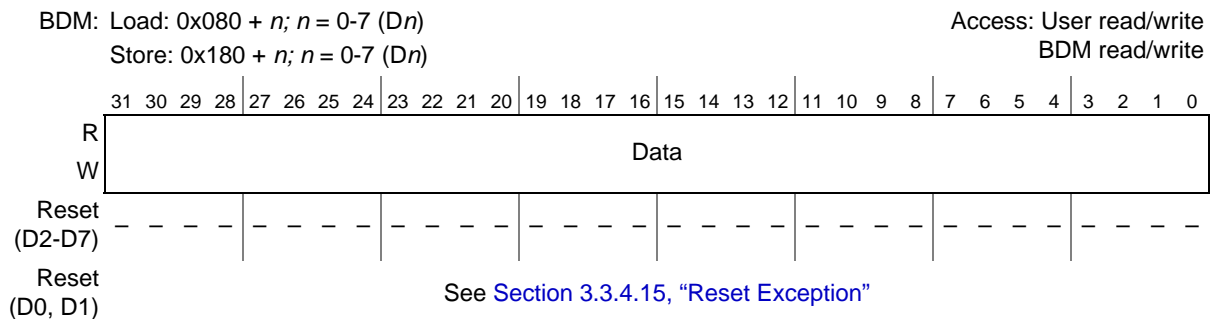


Figure 3-2. Data Registers (D0–D7)

3.2.2 Address Registers (A0–A6)

These registers can be used as software stack pointers, index registers, or base address registers. They can also be used for word and longword operations.

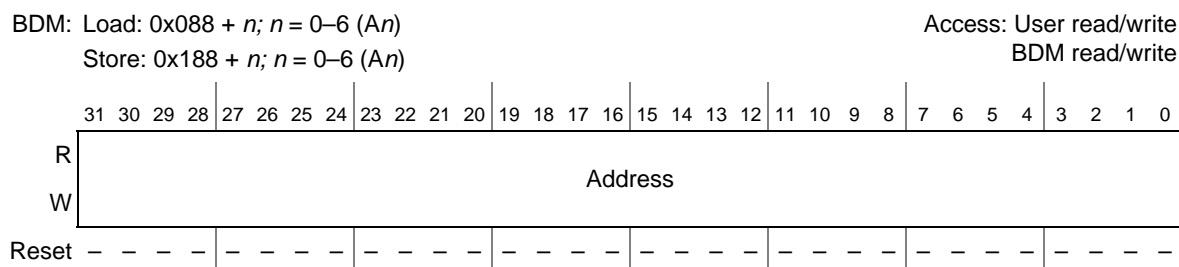


Figure 3-3. Address Registers (A0–A6)

3.2.3 Supervisor/User Stack Pointers (A7 and OTHER_A7)

This ColdFire architecture supports two independent stack pointer (A7) registers—the supervisor stack pointer (SSP) and the user stack pointer (USP). The hardware implementation of these two program-visible 32-bit registers does not identify one as the SSP and the other as the USP. Instead, the hardware uses one 32-bit register as the active A7 and the other as OTHER_A7. Thus, the register contents are a function of the processor operation mode, as shown in the following:

```
if SR[S] = 1
then    A7 = Supervisor Stack Pointer
        OTHER_A7 = User Stack Pointer
else    A7 = User Stack Pointer
        OTHER_A7 = Supervisor Stack Pointer
```

The BDM programming model supports direct reads and writes to A7 and OTHER_A7. It is the responsibility of the external development system to determine, based on the setting of SR[S], the mapping of A7 and OTHER_A7 to the two program-visible definitions (SSP and USP). This functionality is enabled by setting the enable user stack pointer bit, CACR[EUSP]. If this bit is cleared, only a single stack pointer (A7), defined for ColdFire ISA_A, is available. EUSP is cleared at reset.

To support dual stack pointers, the following two supervisor instructions are included in the ColdFire instruction set architecture to load/store the USP:

```
move.l Ay,USP;move to USP
move.l USP,Ax;move from USP
```

These instructions are described in the *ColdFire Family Programmer's Reference Manual*. All other instruction references to the stack pointer, explicit or implicit, access the active A7 register.

NOTE

The SSP is loaded during reset exception processing with the contents of location 0x0000_0000.

BDM: Load: 0x08F (A7)
 Store: 0x18F (A7)
 0x800 (OTHER_A7)

Access: A7: User or BDM read/write
 OTHER_A7: Supervisor or BDM read/write

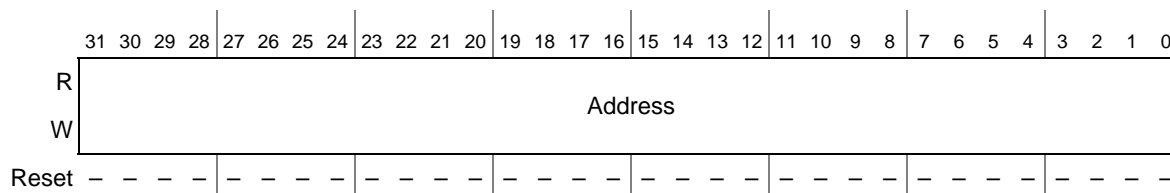


Figure 3-4. Stack Pointer Registers (A7 and OTHER_A7)

3.2.4 Condition Code Register (CCR)

The CCR is the LSB of the processor status register (SR). Bits 4–0 act as indicator flags for results generated by processor operations. The extend bit (X) is also an input operand during multiprecision arithmetic computations. The CCR register must be explicitly loaded after reset and before any compare (CMP), Bcc, or Scc instructions are executed.

BDM: LSB of Status Register (SR)

Access: User read/write
 BDM read/write

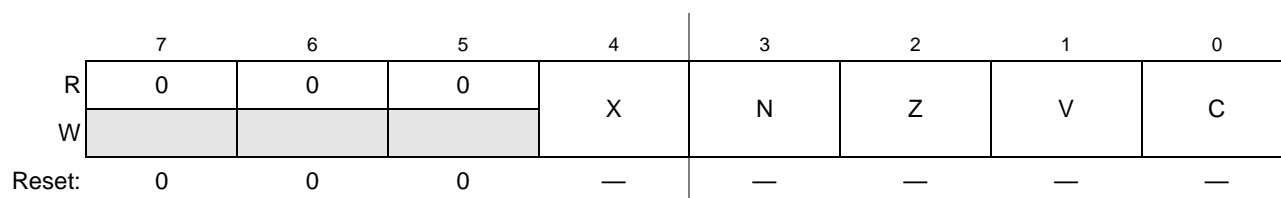


Figure 3-5. Condition Code Register (CCR)

Table 3-2. CCR Field Descriptions

Field	Description
7–5	Reserved, must be cleared.
4 X	Extend condition code bit. Set to the C-bit value for arithmetic operations; otherwise not affected or set to a specified result.
3 N	Negative condition code bit. Set if most significant bit of the result is set; otherwise cleared.
2 Z	Zero condition code bit. Set if result equals zero; otherwise cleared.
1 V	Overflow condition code bit. Set if an arithmetic overflow occurs implying the result cannot be represented in operand size; otherwise cleared.
0 C	Carry condition code bit. Set if a carry out of the operand msb occurs for an addition or if a borrow occurs in a subtraction; otherwise cleared.

3.2.5 Program Counter (PC)

The PC contains the currently executing instruction address. During instruction execution and exception processing, the processor automatically increments contents of the PC or places a new value in the PC, as appropriate. The PC is a base address for PC-relative operand addressing.

The PC is initially loaded during reset exception processing with the contents of location 0x0000_0004.

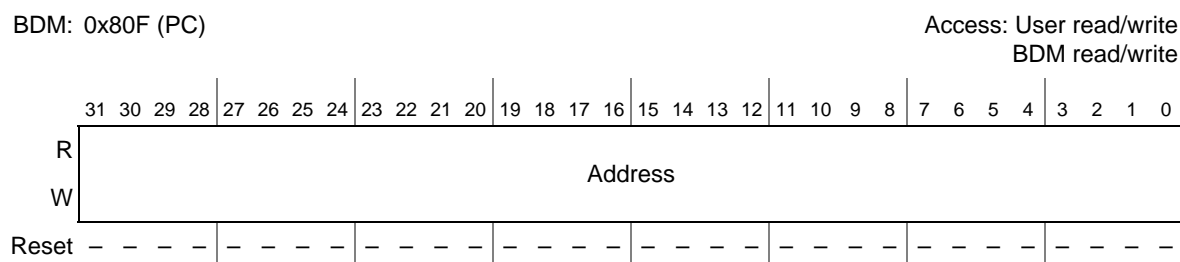


Figure 3-6. Program Counter Register (PC)

3.2.6 Cache Control Register (CACR)

The CACR controls operation of the instruction/data cache memories. It includes bits for enabling, freezing, and invalidating cache contents. It also includes bits for defining the default cache mode and write-protect fields. The CACR is described in [Section 5.2.1, “Cache Control Register \(CACR\).”](#)

3.2.7 Access Control Registers (ACR_n)

The access control registers define attributes for user-defined memory regions. These attributes include the definition of cache mode, write protect, and buffer write enables. The ACRs are described in [Section 5.2.2, “Access Control Registers \(ACR₀, ACR₁\).”](#)

3.2.8 Vector Base Register (VBR)

The VBR contains the base address of the exception vector table in memory. To access the vector table, the displacement of an exception vector is added to the value in VBR. The lower 20 bits of the VBR are not implemented by ColdFire processors. They are assumed to be zero, forcing the table to be aligned on a 1 MByte boundary.

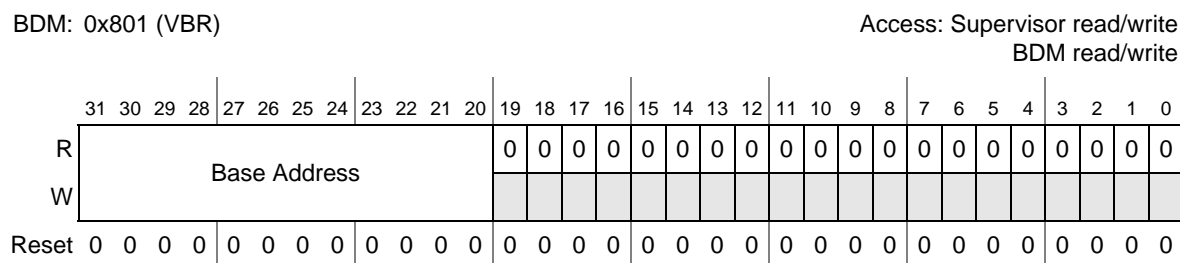


Figure 3-7. Vector Base Register (VBR)

3.2.9 Status Register (SR)

The SR stores the processor status and includes the CCR, the interrupt priority mask, and other control bits. In supervisor mode, software can access the entire SR. In user mode, only the lower 8 bits (CCR) are accessible. The control bits indicate the following states for the processor: trace mode (T bit), supervisor or user mode (S bit), and master or interrupt state (M bit). All defined bits in the SR have read/write access when in supervisor mode. The lower byte of the SR (the CCR) must be loaded explicitly after reset and before any compare (CMP), Bcc, or Scc instructions execute.

BDM: 0x80E (SR)

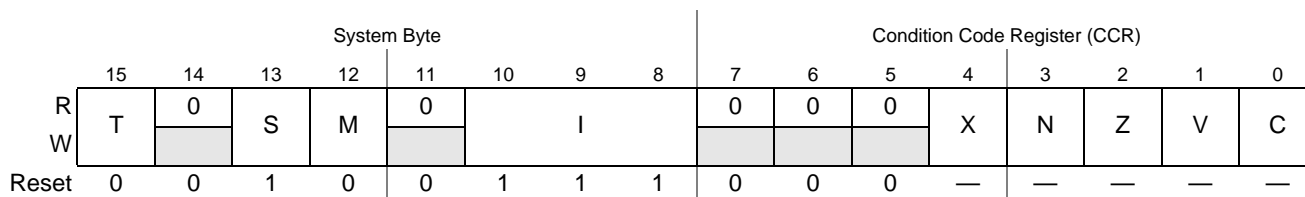
Access: Supervisor read/write
BDM read/write

Figure 3-8. Status Register (SR)

Table 3-3. SR Field Descriptions

Field	Description
15 T	Trace enable. When set, the processor performs a trace exception after every instruction.
14	Reserved, must be cleared.
13 S	Supervisor/user state. 0 User mode 1 Supervisor mode
12 M	Master/interrupt state. Bit is cleared by an interrupt exception and software can set it during execution of the RTE or move to SR instructions.
11	Reserved, must be cleared.
10–8 I	Interrupt level mask. Defines current interrupt level. Interrupt requests are inhibited for all priority levels less than or equal to current level, except edge-sensitive level 7 requests, which cannot be masked.
7–0 CCR	Refer to Section 3.2.4, “Condition Code Register (CCR)” .

3.2.10 Memory Base Address Register (RAMBAR)

The memory base address register is used to specify the base address of the internal SRAM module and indicates the types of references mapped to it. The base address register includes a base address, write-protect bit, address space mask bits, and an enable bit. RAMBAR determines the base address of the on-chip RAM. For more information, refer to [Section 6.2.1, “SRAM Base Address Register \(RAMBAR\)”](#).

3.3 Functional Description

3.3.1 Version 2 ColdFire Microarchitecture

From the block diagram in [Figure 3-1](#), the non-Harvard architecture of the processor is readily apparent. The processor interfaces to the local memory subsystem via a single 32-bit address and two unidirectional 32-bit data buses. This structure minimizes the core size without compromising performance to a large degree.

A more detailed view of the hardware structure within the two pipelines is presented in [Figure 3-9](#) and [Figure 3-10](#) below. In these diagrams, the internal structure of the instruction fetch and operand execution pipelines is shown:

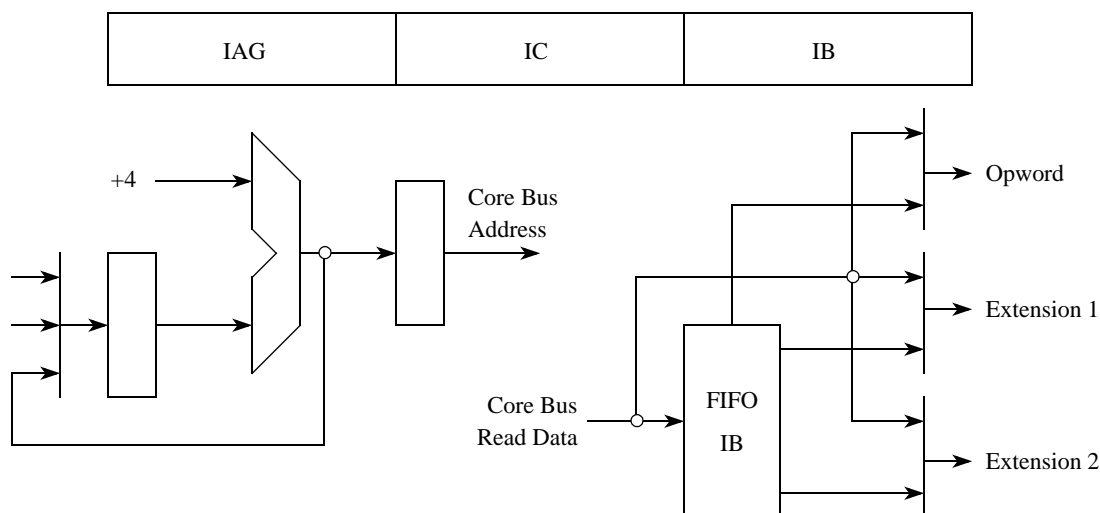


Figure 3-9. Version 2 ColdFire Processor Instruction Fetch Pipeline Diagram

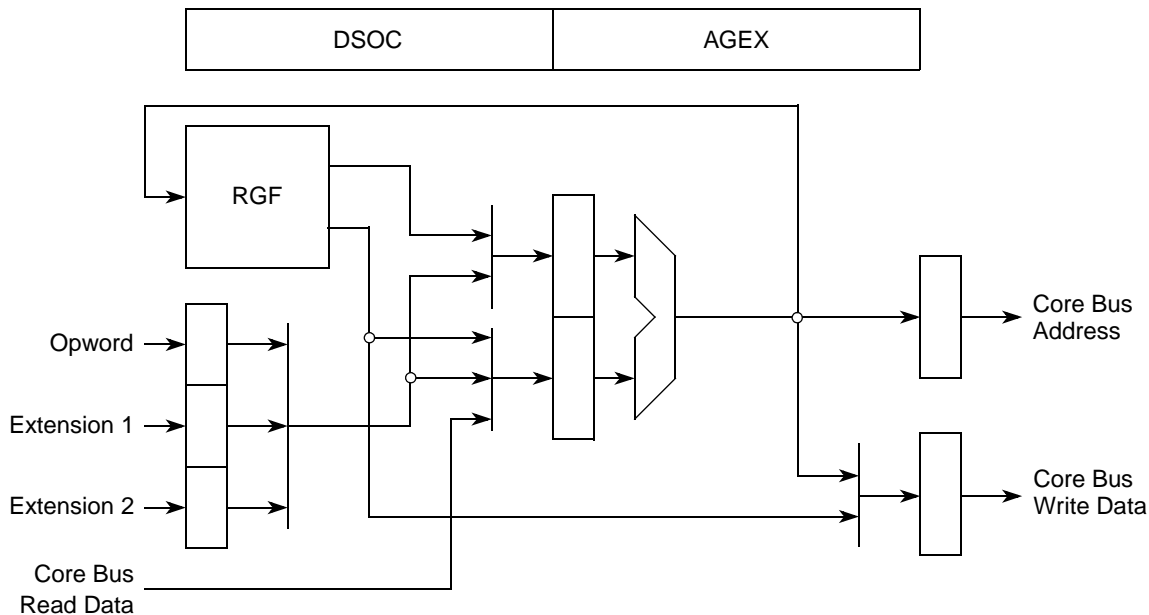


Figure 3-10. Version 2 ColdFire Processor Operand Execution Pipeline Diagram

The instruction fetch pipeline prefetches instructions from local memory using a two-stage structure. For sequential prefetches, the next instruction address is generated by adding four to the last prefetch address. This function is performed during the IAG stage and the resulting prefetch address gated onto the core bus (if there are no pending operand memory accesses assigned a higher priority). After the prefetch address is driven onto the core bus, the instruction fetch cycle accesses the appropriate local memory and returns the instruction read data back to the IFP during the cycle. If the accessed data is not present in a local memory (e.g., an instruction cache miss, or an external access cycle is required), the IFP is stalled in the IC stage until the referenced data is available. As the prefetch data arrives in the IFP, it can be loaded into the FIFO instruction buffer or gated directly into the OEP.

The V2 design uses a simple static conditional branch prediction algorithm (forward-assumed as not-taken, backward-assumed as taken), and all change-of-flow operations are calculated by the OEP and the target instruction address fed back to the IFP.

The IFP and OEP are decoupled by the FIFO instruction buffer, allowing instruction prefetching to occur with the available core bus bandwidth not used for operand memory accesses. For the V2 design, the instruction buffer contains three 32-bit locations.

Consider the operation of the OEP for three basic classes of non-branch instructions:

- Register-to-register:
op Ry, Rx
- Embedded load:
op <mem>y, Rx
- Register-to-memory (store)
move Ry, <mem>x

For simple register-to-register instructions, the first stage of the OEP performs the instruction decode and fetching of the required register operands (OC) from the dual-ported register file, while the actual

instruction execution is performed in the second stage (EX) in one of the execute engines (e.g., ALU, barrel shifter, divider, EMAC). There are no operand memory accesses associated with this class of instructions, and the execution time is typically a single machine cycle. See [Figure 3-11](#).

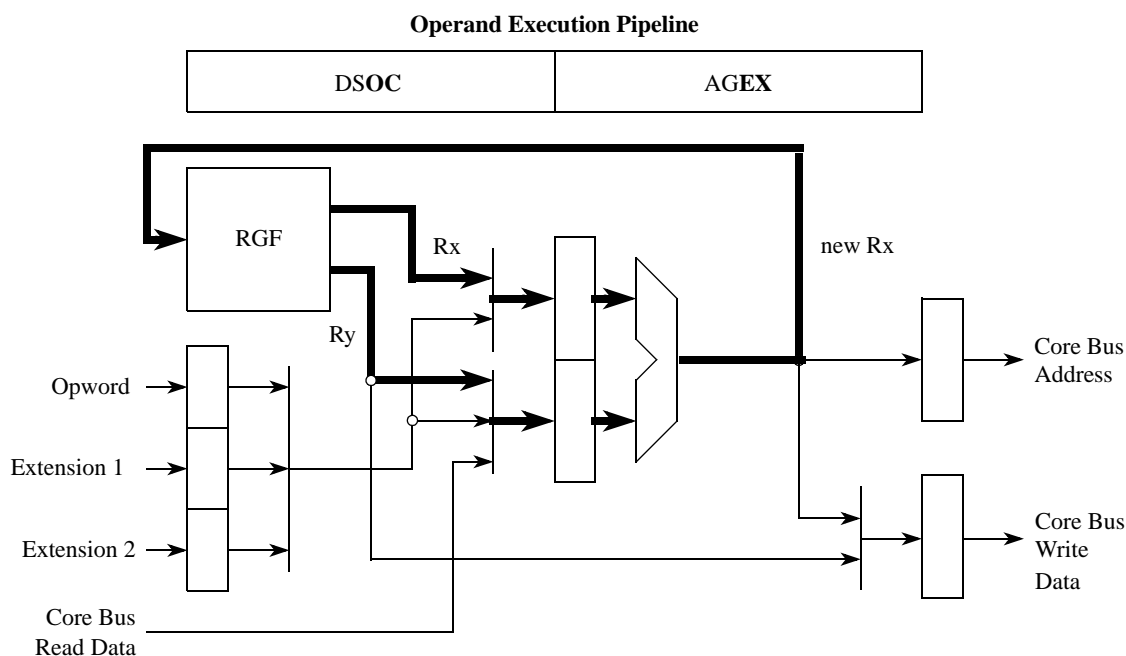


Figure 3-11. V2 OEP Register-to-Register

For memory-to-register (embedded-load) instructions, the instruction is effectively staged through the OEP twice with a basic execution time of three cycles. First, the instruction is decoded and the components of the operand address (base register from the RGF and displacement) are selected (DS). Second, the operand effective address is generated using the ALU execute engine (AG). Third, the memory read operand is fetched from the core bus, while any required register operand is simultaneously fetched (OC) from the RGF. Finally, in the fourth cycle, the instruction is executed (EX). The heavily-used 32-bit load instruction (`move.l <mem>y, Rx`) is optimized to support a two-cycle execution time. The following example in [Figure 3-12](#) shows an effective address of the form $\langle ea \rangle_y = (d16, Ay)$, i.e., a 16-bit signed displacement added to a base register Ay.

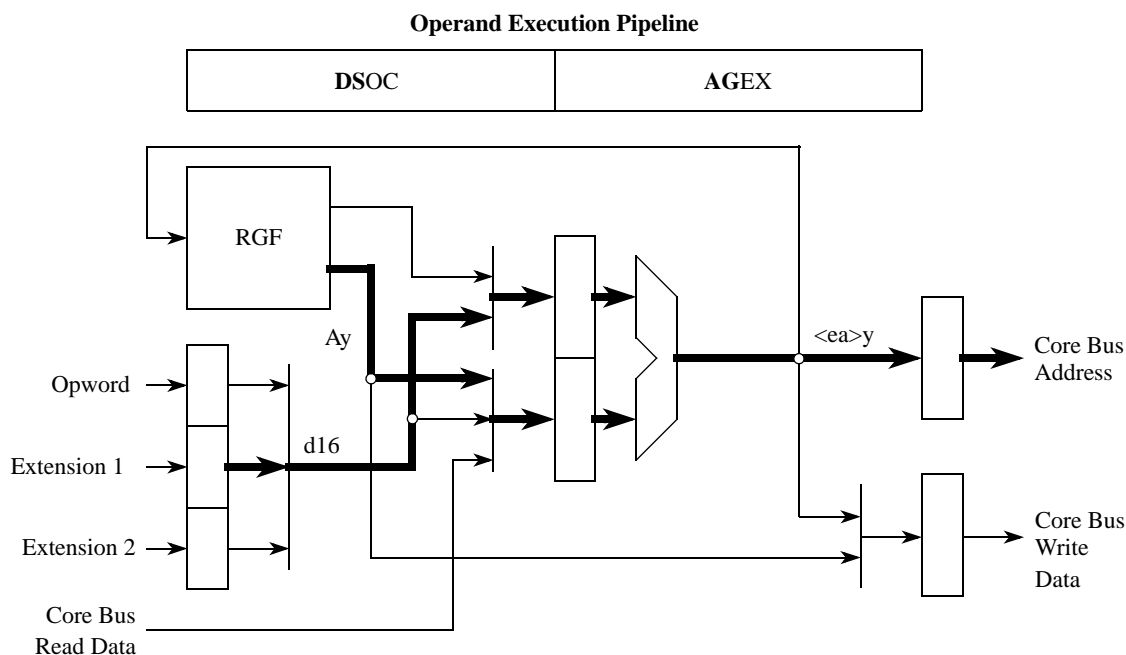


Figure 3-12. V2 OEP Embedded-Load Part 1

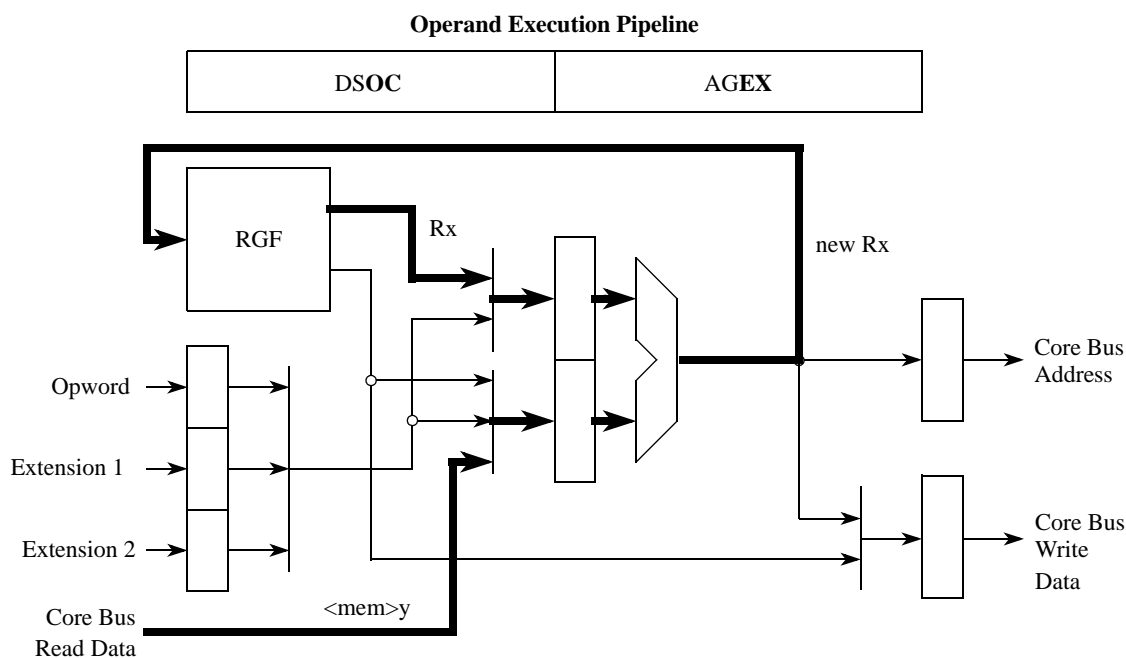


Figure 3-13. V2 OEP Embedded-Load Part 2

For register-to-memory (store) operations, the stage functions (DS/OC, AG/EX) are effectively performed simultaneously allowing single-cycle execution. See [Figure 3-14](#) where the effective address is of the form $\langle ea \rangle x = (d16, Ax)$, i.e., a 16-bit signed displacement added to a base register Ax .

For read-modify-write instructions, the pipeline effectively combines an embedded-load with a store operation for a three-cycle execution time.

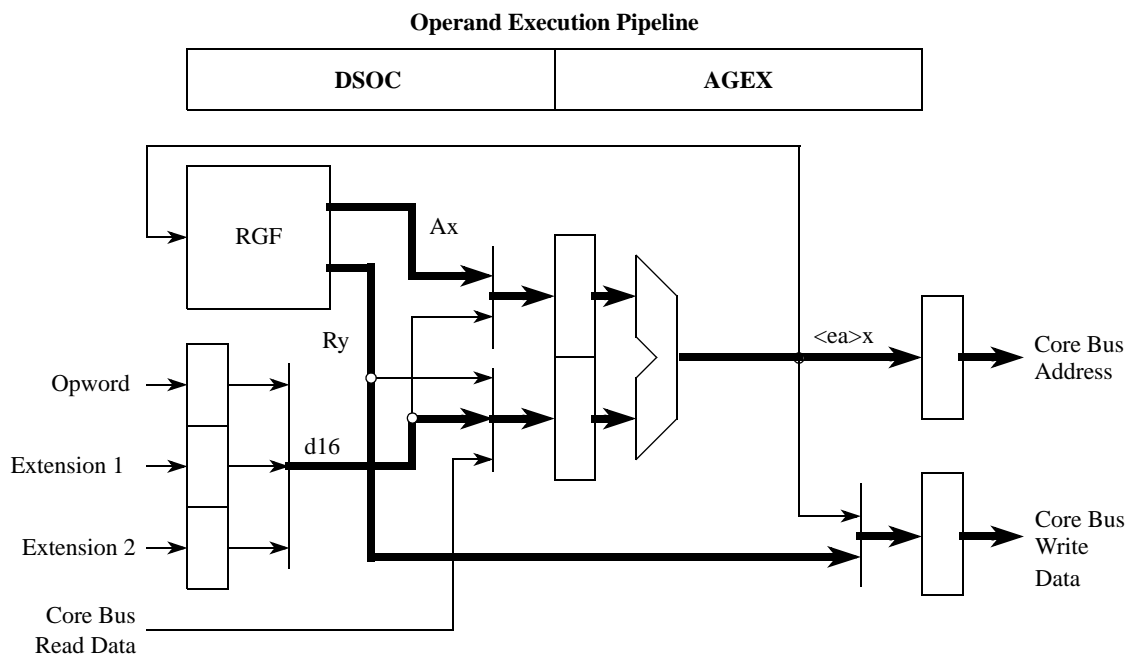


Figure 3-14. V2 OEP Register-to-Memory

The pipeline timing diagrams of [Figure 3-15](#) depict the execution templates for these three classes of instructions. In these diagrams, the x-axis represents time, and the various instruction operations are shown progressing down the operand execution pipeline.

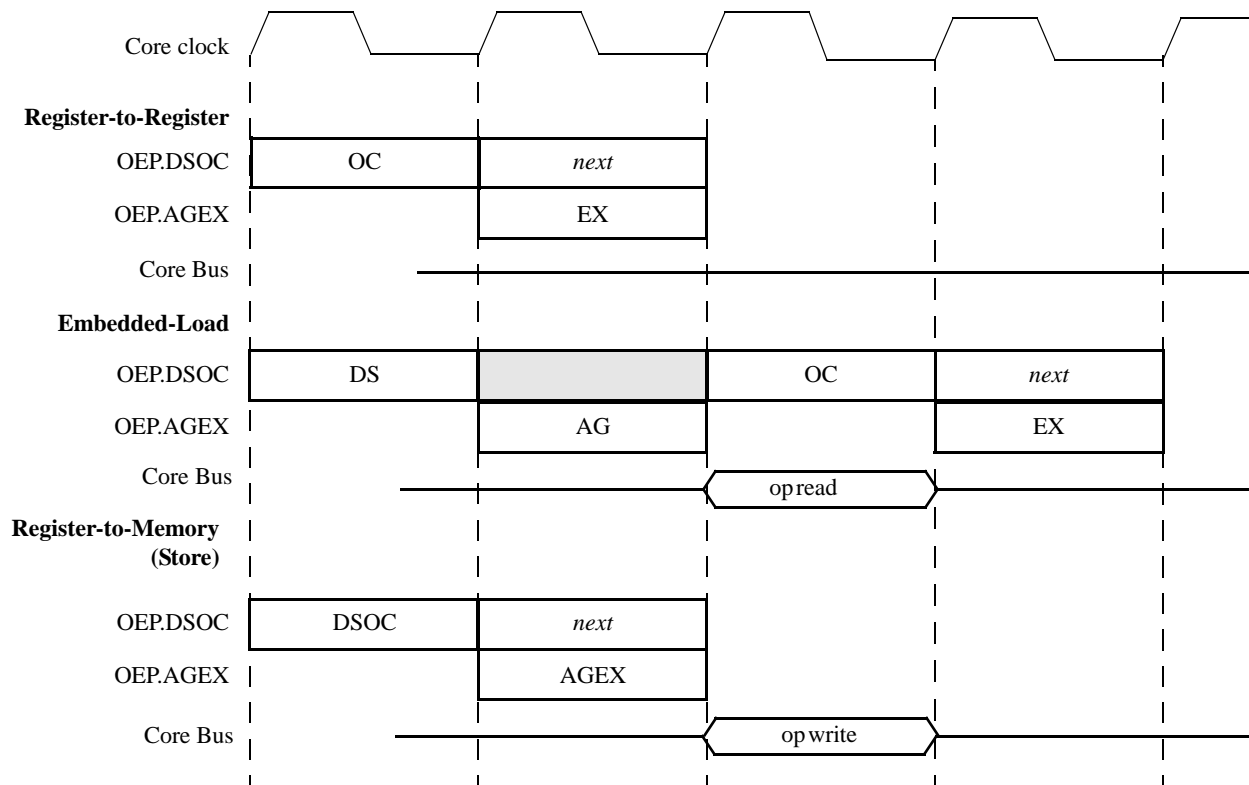


Figure 3-15. V2 OEP Pipeline Execution Templates

3.3.2 Instruction Set Architecture (ISA_A+)

The original ColdFire Instruction Set Architecture (ISA_A) was derived from the M68000 family opcodes based on extensive analysis of embedded application code. The ISA was optimized for code compiled from high-level languages where the dominant operand size was the 32-bit integer declaration. This approach minimized processor complexity and cost, while providing excellent performance for compiled applications.

After the initial ColdFire compilers were created, developers noted there were certain ISA additions that would enhance code density and overall performance. Additionally, as users implemented ColdFire-based designs into a wide range of embedded systems, they found certain frequently-used instruction sequences that could be improved by the creation of additional instructions.

The original ISA definition minimized support for instructions referencing byte- and word-sized operands. Full support for the move byte and move word instructions was provided, but the only other opcodes supporting these data types are CLR (clear) and TST (test). A set of instruction enhancements has been implemented in subsequent ISA revisions, ISA_B and ISA_C. The new opcodes primarily addressed three areas:

1. Enhanced support for byte and word-sized operands
2. Enhanced support for position-independent code
3. Miscellaneous instruction additions to address new functionality

Table 3-4 summarizes the instructions added to revision ISA_A to form revision ISA_A+. For more details see the *ColdFire Family Programmer's Reference Manual*.

Table 3-4. Instruction Enhancements over Revision ISA_A

Instruction	Description
BITREV	The contents of the destination data register are bit-reversed; new Dn[31] equals old Dn[0], new Dn[30] equals old Dn[1],..., new Dn[0] equals old Dn[31].
BYTEREV	The contents of the destination data register are byte-reversed; new Dn[31:24] equals old Dn[7:0],..., new Dn[7:0] equals old Dn[31:24].
FF1	The data register, Dn, is scanned, beginning from the most-significant bit (Dn[31]) and ending with the least-significant bit (Dn[0]), searching for the first set bit. The data register is then loaded with the offset count from bit 31 where the first set bit appears.
Move from USP	USP → Destination register
Move to USP	Source register → USP
STLDSR	Pushes the contents of the status register onto the stack and then reloads the status register with the immediate data value.

3.3.3 Exception Processing Overview

Exception processing for ColdFire processors is streamlined for performance. The ColdFire processors differ from the M68000 family because they include:

- A simplified exception vector table
- Reduced relocation capabilities using the vector-base register
- A single exception stack frame format
- Use of separate system stack pointers for user and supervisor modes.

All ColdFire processors use an instruction restart exception model. However, Version 2 ColdFire processors require more software support to recover from certain access errors. See [Section 3.3.4.1, “Access Error Exception”](#) for details.

Exception processing includes all actions from fault condition detection to the initiation of fetch for first handler instruction. Exception processing is comprised of four major steps:

1. The processor makes an internal copy of the SR and then enters supervisor mode by setting the S bit and disabling trace mode by clearing the T bit. The interrupt exception also forces the M bit to be cleared and the interrupt priority mask to set to current interrupt request level.
2. The processor determines the exception vector number. For all faults except interrupts, the processor performs this calculation based on exception type. For interrupts, the processor performs an interrupt-acknowledge (IACK) bus cycle to obtain the vector number from the interrupt controller. The IACK cycle is mapped to special locations within the interrupt controller's address space with the interrupt level encoded in the address.

3. The processor saves the current context by creating an exception stack frame on the system stack. The exception stack frame is created at a 0-modulo-4 address on top of the system stack pointed to by the supervisor stack pointer (SSP). As shown in [Figure 3-16](#), the processor uses a simplified fixed-length stack frame for all exceptions. The exception type determines whether the program counter placed in the exception stack frame defines the location of the faulting instruction (fault) or the address of the next instruction to be executed (next).
4. The processor calculates the address of the first instruction of the exception handler. By definition, the exception vector table is aligned on a 1 Mbyte boundary. This instruction address is generated by fetching an exception vector from the table located at the address defined in the vector base register. The index into the exception table is calculated as $(4 \times \text{vector number})$. After the exception vector has been fetched, the vector contents determine the address of the first instruction of the desired handler. After the instruction fetch for the first opcode of the handler has initiated, exception processing terminates and normal instruction processing continues in the handler.

All ColdFire processors support a 1024-byte vector table aligned on any 1 Mbyte address boundary (see [Table 3-5](#)).

The table contains 256 exception vectors; the first 64 are defined for the core and the remaining 192 are device-specific peripheral interrupt vectors. See [Chapter 14, “Interrupt Controller Module”](#) for details on the device-specific interrupt sources.

Table 3-5. Exception Vector Assignments

Vector Number(s)	Vector Offset (Hex)	Stacked Program Counter	Assignment
0	0x000	—	Initial supervisor stack pointer
1	0x004	—	Initial program counter
2	0x008	Fault	Access error
3	0x00C	Fault	Address error
4	0x010	Fault	Illegal instruction
5	0x014	Fault	Divide by zero
6–7	0x018–0x01C	—	Reserved
8	0x020	Fault	Privilege violation
9	0x024	Next	Trace
10	0x028	Fault	Unimplemented line-A opcode
11	0x02C	Fault	Unimplemented line-F opcode
12	0x030	Next	Debug interrupt
13	0x034	—	Reserved
14	0x038	Fault	Format error
15–23	0x03C–0x05C	—	Reserved
24	0x060	Next	Spurious interrupt
25–31	0x064–0x07C	—	Reserved

Table 3-5. Exception Vector Assignments (continued)

Vector Number(s)	Vector Offset (Hex)	Stacked Program Counter	Assignment
32–47	0x080–0x0BC	Next	Trap # 0-15 instructions
48–63	0x0C0–0x0FC	—	Reserved
64–255	0x100–0x3FC	Next	Device-specific interrupts

¹ Fault refers to the PC of the instruction that caused the exception. Next refers to the PC of the instruction that follows the instruction that caused the fault.

All ColdFire processors inhibit interrupt sampling during the first instruction of all exception handlers. This allows any handler to disable interrupts effectively, if necessary, by raising the interrupt mask level contained in the status register. In addition, the ISA_A+ architecture includes an instruction (STLDSR) that stores the current interrupt mask level and loads a value into the SR. This instruction is specifically intended for use as the first instruction of an interrupt service routine that services multiple interrupt requests with different interrupt levels. For more details, see *ColdFire Family Programmer's Reference Manual*.

3.3.3.1 Exception Stack Frame Definition

Figure 3-16 shows exception stack frame. The first longword contains the 16-bit format/vector word (F/V) and the 16-bit status register, and the second longword contains the 32-bit program counter address.

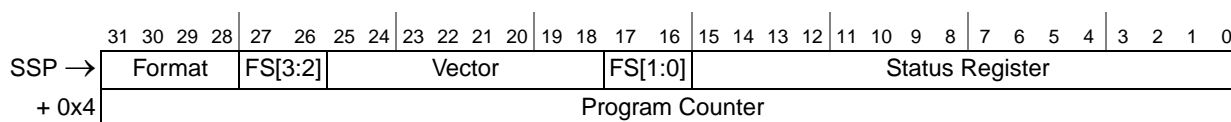


Figure 3-16. Exception Stack Frame Form

The 16-bit format/vector word contains three unique fields:

- A 4-bit format field at the top of the system stack is always written with a value of 4, 5, 6, or 7 by the processor, indicating a two-longword frame format. See Table 3-6.

Table 3-6. Format Field Encodings

Original SSP @ Time of Exception, Bits 1:0	SSP @ 1st Instruction of Handler	Format Field
00	Original SSP - 8	0100
01	Original SSP - 9	0101
10	Original SSP - 10	0110
11	Original SSP - 11	0111

- There is a 4-bit fault status field, FS[3:0], at the top of the system stack. This field is defined for access and address errors only and written as zeros for all other exceptions. See Table 3-7.

Table 3-7. Fault Status Encodings

FS[3:0]	Definition
00xx	Reserved
0100	Error on instruction fetch
0101	Reserved
011x	Reserved
1000	Error on operand write
1001	Attempted write to write-protected space
101x	Reserved
1100	Error on operand read
1101	Reserved
111x	Reserved

- The 8-bit vector number, vector[7:0], defines the exception type and is calculated by the processor for all internal faults and represents the value supplied by the interrupt controller in case of an interrupt. See [Table 3-5](#).

3.3.4 Processor Exceptions

3.3.4.1 Access Error Exception

The exact processor response to an access error depends on the memory reference being performed. For an instruction fetch, the processor postpones the error reporting until the faulted reference is needed by an instruction for execution. Therefore, faults during instruction prefetches followed by a change of instruction flow do not generate an exception. When the processor attempts to execute an instruction with a faulted opword and/or extension words, the access error is signaled and the instruction aborted. For this type of exception, the programming model has not been altered by the instruction generating the access error.

If the access error occurs on an operand read, the processor immediately aborts the current instruction's execution and initiates exception processing. In this situation, any address register updates attributable to the auto-addressing modes, (for example, (An)+, -(An)), have already been performed, so the programming model contains the updated An value. In addition, if an access error occurs during a MOVEM instruction loading from memory, any registers already updated before the fault occurs contain the operands from memory.

The V2 ColdFire processor uses an imprecise reporting mechanism for access errors on operand writes. Because the actual write cycle may be decoupled from the processor's issuing of the operation, the signaling of an access error appears to be decoupled from the instruction that generated the write. Accordingly, the PC contained in the exception stack frame merely represents the location in the program when the access error was signaled. All programming model updates associated with the write instruction are completed. The NOP instruction can collect access errors for writes. This instruction delays its

execution until all previous operations, including all pending write operations, are complete. If any previous write terminates with an access error, it is guaranteed to be reported on the NOP instruction.

3.3.4.2 Address Error Exception

Any attempted execution transferring control to an odd instruction address (if bit 0 of the target address is set) results in an address error exception.

Any attempted use of a word-sized index register (Xn.w) or a scale factor of eight on an indexed effective addressing mode generates an address error, as does an attempted execution of a full-format indexed addressing mode, which is defined by bit 8 of extension word 1 being set.

If an address error occurs on a JSR instruction, the Version 2 ColdFire processor calculates the target address then the return address is pushed onto the stack. If an address error occurs on an RTS instruction, the Version 2 ColdFire processor overwrites the faulting return PC with the address error stack frame.

3.3.4.3 Illegal Instruction Exception

The ColdFire variable-length instruction set architecture supports three instruction sizes: 16, 32, or 48 bits. The first instruction word is known as the operation word (or opword), while the optional words are known as extension word 1 and extension word 2. The opword is further subdivided into three sections: the upper four bits segment the entire ISA into 16 instruction lines, the next 6 bits define the operation mode (opmode), and the low-order 6 bits define the effective address. See [Figure 3-17](#). The opword line definition is shown in [Table 3-8](#).

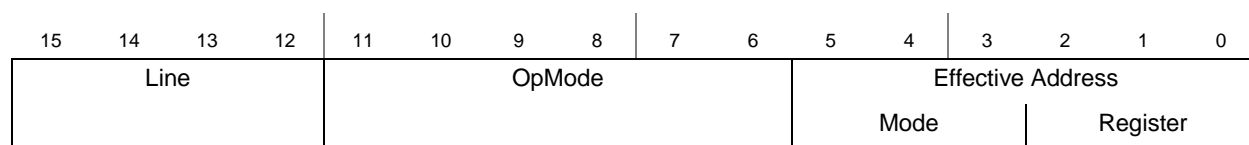


Figure 3-17. ColdFire Instruction Operation Word (Opword) Format

Table 3-8. ColdFire Opword Line Definition

Opword[Line]	Instruction Class
0x0	Bit manipulation, Arithmetic and Logical Immediate
0x1	Move Byte
0x2	Move Long
0x3	Move Word
0x4	Miscellaneous
0x5	Add (ADDQ) and Subtract Quick (SUBQ), Set according to Condition Codes (SCC)
0x6	PC-relative change-of-flow instructions Conditional (BCC) and unconditional (BRA) branches, subroutine calls (BSR)
0x7	Move Quick (MOVEQ), Move with sign extension (MVS) and zero fill (MVZ)
0x8	Logical OR (OR)
0x9	Subtract (SUB), Subtract Extended (SUBX)

Table 3-8. ColdFire Opword Line Definition (continued)

Opword[Line]	Instruction Class
0xA	EMAC, Move 3-bit Quick (MOV3Q)
0xB	Compare (CMP), Exclusive-OR (EOR)
0xC	Logical AND (AND), Multiply Word (MUL)
0xD	Add (ADD), Add Extended (ADDX)
0xE	Arithmetic and logical shifts (ASL, ASR, LSL, LSR)
0xF	Cache Push (CPUSHL), Write DDATA (WDDATA), Write Debug (WDEBUG)

In the original M68000 ISA definition, lines A and F were effectively reserved for user-defined operations (line A) and co-processor instructions (line F). Accordingly, there are two unique exception vectors associated with illegal opwords in these two lines.

Any attempted execution of an illegal 16-bit opcode (except for line-A and line-F opcodes) generates an illegal instruction exception (vector 4). Additionally, any attempted execution of any non-MAC line-A and most line-F opcodes generate their unique exception types, vector numbers 10 and 11, respectively. ColdFire cores do not provide illegal instruction detection on the extension words on any instruction, including MOVEC.

3.3.4.4 Divide-By-Zero

Attempting to divide by zero causes an exception (vector 5, offset equal 0x014).

3.3.4.5 Privilege Violation

The attempted execution of a supervisor mode instruction while in user mode generates a privilege violation exception. See *ColdFire Programmer's Reference Manual* for a list of supervisor-mode instructions.

There is one special case involving the HALT instruction. Normally, this opcode is a supervisor mode instruction, but if the debug module's CSR[UHE] is set, then this instruction can be also be executed in user mode for debugging purposes.

3.3.4.6 Trace Exception

To aid in program development, all ColdFire processors provide an instruction-by-instruction tracing capability. While in trace mode, indicated by setting of the SR[T] bit, the completion of an instruction execution (for all but the stop instruction) signals a trace exception. This functionality allows a debugger to monitor program execution.

The stop instruction has the following effects:

1. The instruction before the stop executes and then generates a trace exception. In the exception stack frame, the PC points to the stop opcode.
2. When the trace handler is exited, the stop instruction executes, loading the SR with the immediate operand from the instruction.

3. The processor then generates a trace exception. The PC in the exception stack frame points to the instruction after the stop, and the SR reflects the value loaded in the previous step.

If the processor is not in trace mode and executes a stop instruction where the immediate operand sets SR[T], hardware loads the SR and generates a trace exception. The PC in the exception stack frame points to the instruction after the stop, and the SR reflects the value loaded in step 2.

Because ColdFire processors do not support any hardware stacking of multiple exceptions, it is the responsibility of the operating system to check for trace mode after processing other exception types. As an example, consider a TRAP instruction execution while in trace mode. The processor initiates the trap exception and then passes control to the corresponding handler. If the system requires that a trace exception be processed, it is the responsibility of the trap exception handler to check for this condition (SR[T] in the exception stack frame set) and pass control to the trace handler before returning from the original exception.

3.3.4.7 Unimplemented Line-A Opcode

A line-A opcode is defined when bits 15-12 of the opword are 0b1010. This exception is generated by the attempted execution of an undefined line-A opcode.

3.3.4.8 Unimplemented Line-F Opcode

A line-F opcode is defined when bits 15-12 of the opword are 0b1111. This exception is generated when attempting to execute an undefined line-F opcode.

3.3.4.9 Debug Interrupt

See [Chapter 26, “Debug Module,”](#) for a detailed explanation of this exception, which is generated in response to a hardware breakpoint register trigger. The processor does not generate an IACK cycle, but rather calculates the vector number internally (vector number 12). Additionally, SR[M,I] are unaffected by the interrupt.

3.3.4.10 RTE and Format Error Exception

When an RTE instruction is executed, the processor first examines the 4-bit format field to validate the frame type. For a ColdFire core, any attempted RTE execution (where the format is not equal to {4,5,6,7}) generates a format error. The exception stack frame for the format error is created without disturbing the original RTE frame and the stacked PC pointing to the RTE instruction.

The selection of the format value provides some limited debug support for porting code from M68000 applications. On M68000 family processors, the SR was located at the top of the stack. On those processors, bit 30 of the longword addressed by the system stack pointer is typically zero. Thus, if an RTE is attempted using this old format, it generates a format error on a ColdFire processor.

If the format field defines a valid type, the processor: (1) reloads the SR operand, (2) fetches the second longword operand, (3) adjusts the stack pointer by adding the format value to the auto-incremented address after the fetch of the first longword, and then (4) transfers control to the instruction address defined by the second longword operand within the stack frame.

3.3.4.11 TRAP Instruction Exception

The TRAP #n instruction always forces an exception as part of its execution and is useful for implementing system calls. The TRAP instruction may be used to change from user to supervisor mode.

3.3.4.12 Unsupported Instruction Exception

If execution of a valid instruction is attempted but the required hardware is not present in the processor, an unsupported instruction exception is generated. The instruction functionality can then be emulated in the exception handler, if desired.

All ColdFire cores record the processor hardware configuration in the D0 register immediately after the negation of RESET. See [Section 3.3.4.15, “Reset Exception,”](#) for details.

3.3.4.13 Interrupt Exception

Interrupt exception processing includes interrupt recognition and the fetch of the appropriate vector from the interrupt controller using an IACK cycle. See [Chapter 14, “Interrupt Controller Module,”](#) for details on the interrupt controller.

3.3.4.14 Fault-on-Fault Halt

If a ColdFire processor encounters any type of fault during the exception processing of another fault, the processor immediately halts execution with the catastrophic fault-on-fault condition. A reset is required to exit this state.

3.3.4.15 Reset Exception

Asserting the reset input signal ($\overline{\text{RESET}}$) to the processor causes a reset exception. The reset exception has the highest priority of any exception; it provides for system initialization and recovery from catastrophic failure. Reset also aborts any processing in progress when the reset input is recognized. Processing cannot be recovered.

The reset exception places the processor in the supervisor mode by setting the SR[S] bit and disables tracing by clearing the SR[T] bit. This exception also clears the SR[M] bit and sets the processor's SR[I] field to the highest level (level 7, 0b111). Next, the VBR is initialized to zero (0x0000_0000). The control registers specifying the operation of any memories (e.g., cache and/or RAM modules) connected directly to the processor are disabled.

NOTE

Other implementation-specific registers are also affected. Refer to each module in this reference manual for details on these registers.

After the processor is granted the bus, it performs two longword read-bus cycles. The first longword at address 0x0000_0000 is loaded into the supervisor stack pointer and the second longword at address 0x0000_0004 is loaded into the program counter. After the initial instruction is fetched from memory, program execution begins at the address in the PC. If an access error or address error occurs before the first instruction is executed, the processor enters the fault-on-fault state.

ColdFire processors load hardware configuration information into the D0 and D1 general-purpose registers after system reset. The hardware configuration information is loaded immediately after the reset-in signal is negated. This allows an emulator to read out the contents of these registers via the BDM to determine the hardware configuration.

Information loaded into D0 defines the processor hardware configuration as shown in [Figure 3-18](#).

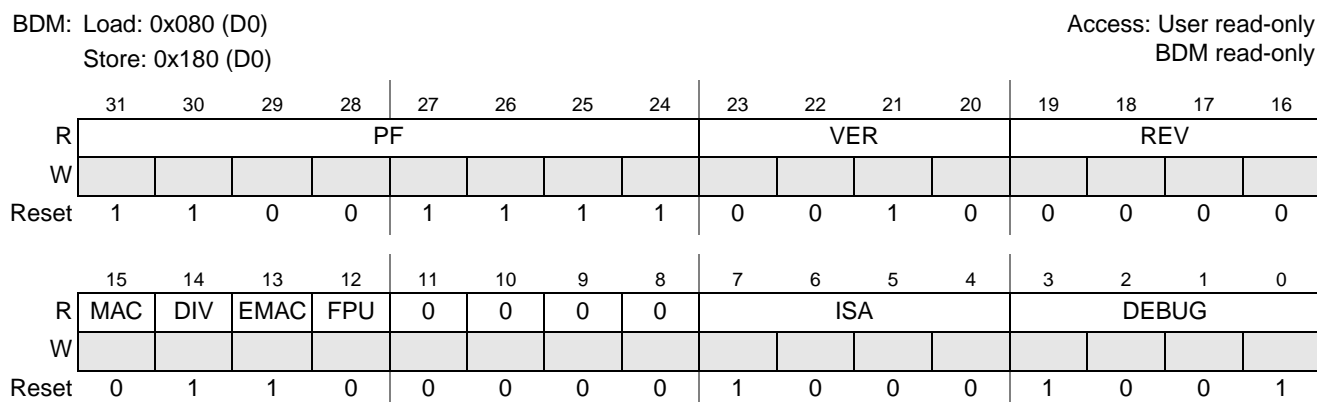


Figure 3-18. D0 Hardware Configuration Info

Table 3-9. D0 Hardware Configuration Info Field Description

Field	Description
31–24 PF	Processor family. This field is fixed to a hex value of 0xCF indicating a ColdFire core is present.
23–20 VER	ColdFire core version number. Defines the hardware microarchitecture version of ColdFire core. 0001 V1 ColdFire core 0010 V2 ColdFire core (This is the value used for this device.) 0011 V3 ColdFire core 0100 V4 ColdFire core 0101 V5 ColdFire core Else Reserved for future use
19–16 REV	Processor revision number. The default is 0b0000.
15 MAC	MAC present. This bit signals if the optional multiply-accumulate (MAC) execution engine is present in processor core. 0 MAC execute engine not present in core. (This is the value used for this device.) 1 MAC execute engine is present in core.
14 DIV	Divide present. This bit signals if the hardware divider (DIV) is present in the processor core. 0 Divide execute engine not present in core. 1 Divide execute engine is present in core. (This is the value used for this device.)
13 EMAC	EMAC present. This bit signals if the optional enhanced multiply-accumulate (EMAC) execution engine is present in processor core. 0 EMAC execute engine not present in core. 1 EMAC execute engine is present in core. (This is the value used for this device.)
12 FPU	FPU present. This bit signals if the optional floating-point (FPU) execution engine is present in processor core. 0 FPU execute engine not present in core. (This is the value used for this device.) 1 FPU execute engine is present in core.

Table 3-9. D0 Hardware Configuration Info Field Description (continued)

Field	Description
10–8	Reserved.
7–4 ISA	ISA revision. Defines the instruction-set architecture (ISA) revision level implemented in ColdFire processor core. 0000 ISA_A 0001 ISA_B 0010 ISA_C 1000 ISA_A+ (This is the value used for this device.) Else Reserved
3–0 DEBUG	Debug module revision number. Defines revision level of the debug module used in the ColdFire processor core. 0000 DEBUG_A 0001 DEBUG_B 0010 DEBUG_C 0011 DEBUG_D 0100 DEBUG_E 1001 DEBUG_B+ (This is the value used for this device.) 1011 DEBUG_D+ 1111 DEBUG_D+PST Buffer Else Reserved

Information loaded into D1 defines the local memory hardware configuration as shown in the figure below.

BDM: Load: 0x081 (D1)

Store: 0x181 (D1)

Access: User read-only

BDM read-only

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
R	CLSZ		CCAS		CCSZ				0	0	0	0	0	0	0	0
W																
Reset	0	0	0	1	0	1	0	1	0	0	0	0	0	0	0	0

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	MBSZ		0	0	0	0	0	0	SRAMSZ				0	0	0	
W																
Reset	0	0	0	1	0	0	0	0	0	1	1	0	0	0	0	0

Figure 3-19. D1 Hardware Configuration Info**Table 3-10. D1 Hardware Configuration Information Field Description**

Field	Description
31–30 CLSZ	Cache line size. This field is fixed to a hex value of 0x0 indicating a 16-byte cache line size.
29–28 CCAS	Configurable cache associativity. 00 Four-way 01 Direct mapped (This is the value used for this device) Else Reserved for future use

Table 3-10. D1 Hardware Configuration Information Field Description (continued)

Field	Description
27–24 CCSZ	Configurable cache size. Indicates the amount of instruction/data cache. The cache configuration options available are 50% instruction/50% data, 100% instruction, or 100% data, and are specified in the CACR register. 0000 No configurable cache 0001 512B configurable cache 0010 1KB configurable cache 0011 2KB configurable cache 0100 4KB configurable cache 0101 8KB configurable cache 0110 16KB configurable cache 0111 32KB configurable cache Else Reserved
23–16	Reserved.
15–14 MBSZ	Bus size. Defines the width of the ColdFire master bus datapath. 00 32-bit system bus datapath (This is the value used for this device) 01 64-bit system bus datapath Else Reserved
13–8	Reserved, resets to 0b010000
7–3 SRAMSZ	SRAM bank size. 00000 No SRAM 00010 512 bytes 00100 1 Kbytes 00110 2 Kbytes 01000 4 Kbytes 01010 8 Kbytes 01100 16 Kbytes (This is the value used for this device) 01110 32 Kbytes 10000 64 Kbytes 10010 128 Kbytes Else Reserved for future use
2–0	Reserved.

3.3.5 Instruction Execution Timing

This section presents processor instruction execution times in terms of processor-core clock cycles. The number of operand references for each instruction is enclosed in parentheses following the number of processor clock cycles. Each timing entry is presented as C(R/W) where:

- C is the number of processor clock cycles, including all applicable operand fetches and writes, and all internal core cycles required to complete the instruction execution.
- R/W is the number of operand reads (R) and writes (W) required by the instruction. An operation performing a read-modify-write function is denoted as (1/1).

This section includes the assumptions concerning the timing values and the execution time details.

3.3.5.1 Timing Assumptions

For the timing data presented in this section, these assumptions apply:

1. The OEP is loaded with the opword and all required extension words at the beginning of each instruction execution. This implies that the OEP does not wait for the IFP to supply opwords and/or extension words.
2. The OEP does not experience any sequence-related pipeline stalls. The most common example of stall involves consecutive store operations, excluding the MOVEM instruction. For all STORE operations (except MOVEM), certain hardware resources within the processor are marked as busy for two clock cycles after the final decode and select/operand fetch cycle (DSOC) of the store instruction. If a subsequent STORE instruction is encountered within this 2-cycle window, it is stalled until the resource again becomes available. Thus, the maximum pipeline stall involving consecutive STORE operations is two cycles. The MOVEM instruction uses a different set of resources and this stall does not apply.
3. The OEP completes all memory accesses without any stall conditions caused by the memory itself. Thus, the timing details provided in this section assume that an infinite zero-wait state memory is attached to the processor core.
4. All operand data accesses are aligned on the same byte boundary as the operand size; for example, 16-bit operands aligned on 0-modulo-2 addresses, 32-bit operands aligned on 0-modulo-4 addresses.

The processor core decomposes misaligned operand references into a series of aligned accesses as shown in [Table 3-11](#).

Table 3-11. Misaligned Operand References

address[1:0]	Size	Bus Operations	Additional C(R/W)
01 or 11	Word	Byte, Byte	2(1/0) if read 1(0/1) if write
01 or 11	Long	Byte, Word, Byte	3(2/0) if read 2(0/2) if write
10	Long	Word, Word	2(1/0) if read 1(0/1) if write

3.3.5.2 MOVE Instruction Execution Times

[Table 3-12](#) lists execution times for MOVE.{B,W} instructions; [Table 3-13](#) lists timings for MOVE.L.

NOTE

For all tables in this section, the execution time of any instruction using the PC-relative effective addressing modes is the same for the comparable An-relative mode.

ET with {<ea> = (d16,PC)} equals ET with {<ea> = (d16,An)}
 ET with {<ea> = (d8,PC,Xi*SF)} equals ET with {<ea> = (d8,An,Xi*SF)}

The nomenclature xxx.wl refers to both forms of absolute addressing, xxx.w and xxx.l.

Table 3-12. MOVE Byte and Word Execution Times

Source	Destination						
	Rx	(Ax)	(Ax)+	-(Ax)	(d16,Ax)	(d8,Ax,Xi*SF)	xxx.wl
Dy	1(0/0)	1(0/1)	1(0/1)	1(0/1)	1(0/1)	2(0/1)	1(0/1)
Ay	1(0/0)	1(0/1)	1(0/1)	1(0/1)	1(0/1)	2(0/1)	1(0/1)
(Ay)	3(1/0)	3(1/1)	3(1/1)	3(1/1)	3(1/1)	4(1/1))	3(1/1)
(Ay)+	3(1/0)	3(1/1)	3(1/1)	3(1/1)	3(1/1)	4(1/1))	3(1/1)
-(Ay)	3(1/0)	3(1/1)	3(1/1)	3(1/1)	3(1/1)	4(1/1))	3(1/1)
(d16,Ay)	3(1/0)	3(1/1)	3(1/1)	3(1/1)	3(1/1)	—	—
(d8,Ay,Xi*SF)	4(1/0)	4(1/1)	4(1/1)	4(1/1)	—	—	—
xxx.w	3(1/0)	3(1/1)	3(1/1)	3(1/1)	—	—	—
xxx.l	3(1/0)	3(1/1)	3(1/1)	3(1/1)	—	—	—
(d16,PC)	3(1/0)	3(1/1)	3(1/1)	3(1/1)	3(1/1)	—	—
(d8,PC,Xi*SF)	4(1/0)	4(1/1)	4(1/1)	4(1/1))	—	—	—
#xxx	1(0/0)	3(0/1)	3(0/1)	3(0/1)	—	—	—

Table 3-13. MOVE Long Execution Times

Source	Destination						
	Rx	(Ax)	(Ax)+	-(Ax)	(d16,Ax)	(d8,Ax,Xi*SF)	xxx.wl
Dy	1(0/0)	1(0/1)	1(0/1)	1(0/1)	1(0/1)	2(0/1)	1(0/1)
Ay	1(0/0)	1(0/1)	1(0/1)	1(0/1)	1(0/1)	2(0/1)	1(0/1)
(Ay)	2(1/0)	2(1/1)	2(1/1)	2(1/1)	2(1/1)	3(1/1)	2(1/1)
(Ay)+	2(1/0)	2(1/1)	2(1/1)	2(1/1)	2(1/1)	3(1/1)	2(1/1)
-(Ay)	2(1/0)	2(1/1)	2(1/1)	2(1/1)	2(1/1)	3(1/1)	2(1/1)
(d16,Ay)	2(1/0)	2(1/1)	2(1/1)	2(1/1)	2(1/1)	—	—
(d8,Ay,Xi*SF)	3(1/0)	3(1/1)	3(1/1)	3(1/1)	—	—	—
xxx.w	2(1/0)	2(1/1)	2(1/1)	2(1/1)	—	—	—
xxx.l	2(1/0)	2(1/1)	2(1/1)	2(1/1)	—	—	—
(d16,PC)	2(1/0)	2(1/1)	2(1/1)	2(1/1)	2(1/1)	—	—
(d8,PC,Xi*SF)	3(1/0)	3(1/1)	3(1/1)	3(1/1)	—	—	—
#xxx	1(0/0)	2(0/1)	2(0/1)	2(0/1)	—	—	—

3.3.5.3 Standard One Operand Instruction Execution Times

Table 3-14. One Operand Instruction Execution Times

Opcode	<EA>	Effective Address							
		Rn	(An)	(An)+	-(An)	(d16,An)	(d8,An,Xn*SF)	xxx.wl	#xxx
BITREV	Dx	1(0/0)	—	—	—	—	—	—	—
BYTEREV	Dx	1(0/0)	—	—	—	—	—	—	—
CLR.B	<ea>	1(0/0)	1(0/1)	1(0/1)	1(0/1)	1(0/1)	2(0/1)	1(0/1)	—
CLR.W	<ea>	1(0/0)	1(0/1)	1(0/1)	1(0/1)	1(0/1)	2(0/1)	1(0/1)	—
CLR.L	<ea>	1(0/0)	1(0/1)	1(0/1)	1(0/1)	1(0/1)	2(0/1)	1(0/1)	—
EXT.W	Dx	1(0/0)	—	—	—	—	—	—	—
EXT.L	Dx	1(0/0)	—	—	—	—	—	—	—
EXTB.L	Dx	1(0/0)	—	—	—	—	—	—	—
FF1	Dx	1(0/0)	—	—	—	—	—	—	—
NEG.L	Dx	1(0/0)	—	—	—	—	—	—	—
NEGX.L	Dx	1(0/0)	—	—	—	—	—	—	—
NOT.L	Dx	1(0/0)	—	—	—	—	—	—	—
SCC	Dx	1(0/0)	—	—	—	—	—	—	—
SWAP	Dx	1(0/0)	—	—	—	—	—	—	—
TST.B	<ea>	1(0/0)	3(1/0)	3(1/0)	3(1/0)	3(1/0)	4(1/0)	3(1/0)	1(0/0)
TST.W	<ea>	1(0/0)	3(1/0)	3(1/0)	3(1/0)	3(1/0)	4(1/0)	3(1/0)	1(0/0)
TST.L	<ea>	1(0/0)	2(1/0)	2(1/0)	2(1/0)	2(1/0)	3(1/0)	2(1/0)	1(0/0)

3.3.5.4 Standard Two Operand Instruction Execution Times

Table 3-15. Two Operand Instruction Execution Times

Opcode	<EA>	Effective Address							
		Rn	(An)	(An)+	-(An)	(d16,An) (d16,PC)	(d8,An,Xn*SF) (d8,PC,Xn*SF)	xxx.wl	#xxx
ADD.L	<ea>,Rx	1(0/0)	3(1/0)	3(1/0)	3(1/0)	3(1/0)	4(1/0)	3(1/0)	1(0/0)
ADD.L	Dy,<ea>	—	3(1/1)	3(1/1)	3(1/1)	3(1/1)	4(1/1)	3(1/1)	—
ADDI.L	#imm,Dx	1(0/0)	—	—	—	—	—	—	—
ADDQ.L	#imm,<ea>	1(0/0)	3(1/1)	3(1/1)	3(1/1)	3(1/1)	4(1/1)	3(1/1)	—
ADDX.L	Dy,Dx	1(0/0)	—	—	—	—	—	—	—
AND.L	<ea>,Rx	1(0/0)	3(1/0)	3(1/0)	3(1/0)	3(1/0)	4(1/0)	3(1/0)	1(0/0)
AND.L	Dy,<ea>	—	3(1/1)	3(1/1)	3(1/1)	3(1/1)	4(1/1)	3(1/1)	—
ANDI.L	#imm,Dx	1(0/0)	—	—	—	—	—	—	—

Table 3-15. Two Operand Instruction Execution Times (continued)

Opcode	<EA>	Effective Address							
		Rn	(An)	(An)+	-(An)	(d16,An) (d16,PC)	(d8,An,Xn*SF) (d8,PC,Xn*SF)	xxx.wl	#xxx
ASL.L	<ea>,Dx	1(0/0)	—	—	—	—	—	—	1(0/0)
ASR.L	<ea>,Dx	1(0/0)	—	—	—	—	—	—	1(0/0)
BCHG	Dy,<ea>	2(0/0)	4(1/1)	4(1/1)	4(1/1)	4(1/1)	5(1/1)	4(1/1)	—
BCHG	#imm,<ea>	2(0/0)	4(1/1)	4(1/1)	4(1/1)	4(1/1)	—	—	—
BCLR	Dy,<ea>	2(0/0)	4(1/1)	4(1/1)	4(1/1)	4(1/1)	5(1/1)	4(1/1)	—
BCLR	#imm,<ea>	2(0/0)	4(1/1)	4(1/1)	4(1/1)	4(1/1)	—	—	—
BSET	Dy,<ea>	2(0/0)	4(1/1)	4(1/1)	4(1/1)	4(1/1)	5(1/1)	4(1/1)	—
BSET	#imm,<ea>	2(0/0)	4(1/1)	4(1/1)	4(1/1)	4(1/1)	—	—	—
BTST	Dy,<ea>	2(0/0)	3(1/0)	3(1/0)	3(1/0)	3(1/0)	4(1/0)	3(1/0)	—
BTST	#imm,<ea>	1(0/0)	3(1/0)	3(1/0)	3(1/0)	3(1/0)	—	—	—
CMP.L	<ea>,Rx	1(0/0)	3(1/0)	3(1/0)	3(1/0)	3(1/0)	4(1/0)	3(1/0)	1(0/0)
CMPI.L	#imm,Dx	1(0/0)	—	—	—	—	—	—	—
DIVS.W	<ea>,Dx	20(0/0)	23(1/0)	23(1/0)	23(1/0)	23(1/0)	24(1/0)	23(1/0)	20(0/0)
DIVU.W	<ea>,Dx	20(0/0)	23(1/0)	23(1/0)	23(1/0)	23(1/0)	24(1/0)	23(1/0)	20(0/0)
DIVS.L	<ea>,Dx	≤35(0/0)	≤38(1/0)	≤38(1/0)	≤38(1/0)	≤38(1/0)	—	—	—
DIVU.L	<ea>,Dx	≤35(0/0)	≤38(1/0)	≤38(1/0)	≤38(1/0)	≤38(1/0)	—	—	—
EOR.L	Dy,<ea>	1(0/0)	3(1/1)	3(1/1)	3(1/1)	3(1/1)	4(1/1)	3(1/1)	—
EORI.L	#imm,Dx	1(0/0)	—	—	—	—	—	—	—
LEA	<ea>,Ax	—	1(0/0)	—	—	1(0/0)	2(0/0)	1(0/0)	—
LSL.L	<ea>,Dx	1(0/0)	—	—	—	—	—	—	1(0/0)
LSR.L	<ea>,Dx	1(0/0)	—	—	—	—	—	—	1(0/0)
MOVEQ.L	#imm,Dx	—	—	—	—	—	—	—	1(0/0)
OR.L	<ea>,Rx	1(0/0)	3(1/0)	3(1/0)	3(1/0)	3(1/0)	4(1/0)	3(1/0)	1(0/0)
OR.L	Dy,<ea>	—	3(1/1)	3(1/1)	3(1/1)	3(1/1)	4(1/1)	3(1/1)	—
ORI.L	#imm,Dx	1(0/0)	—	—	—	—	—	—	—
REMS.L	<ea>,Dx	≤35(0/0)	≤38(1/0)	≤38(1/0)	≤38(1/0)	≤38(1/0)	—	—	—
REMU.L	<ea>,Dx	≤35(0/0)	≤38(1/0)	≤38(1/0)	≤38(1/0)	≤38(1/0)	—	—	—
SUB.L	<ea>,Rx	1(0/0)	3(1/0)	3(1/0)	3(1/0)	3(1/0)	4(1/0)	3(1/0)	1(0/0)
SUB.L	Dy,<ea>	—	3(1/1)	3(1/1)	3(1/1)	3(1/1)	4(1/1)	3(1/1)	—
SUBI.L	#imm,Dx	1(0/0)	—	—	—	—	—	—	—
SUBQ.L	#imm,<ea>	1(0/0)	3(1/1)	3(1/1)	3(1/1)	3(1/1)	4(1/1)	3(1/1)	—
SUBX.L	Dy,Dx	1(0/0)	—	—	—	—	—	—	—

3.3.5.5 Miscellaneous Instruction Execution Times

Table 3-16. Miscellaneous Instruction Execution Times

Opcode	<EA>	Effective Address							
		Rn	(An)	(An)+	-(An)	(d16,An)	(d8,An,Xn*SF)	xxx.wl	#xxx
CPUSHL	(Ax)	—	11(0/1)	—	—	—	—	—	—
LINK.W	Ay,#imm	2(0/1)	—	—	—	—	—	—	—
MOVE.L	Ay,USP	3(0/0)	—	—	—	—	—	—	—
MOVE.L	USP,Ax	3(0/0)	—	—	—	—	—	—	—
MOVE.W	CCR,Dx	1(0/0)	—	—	—	—	—	—	—
MOVE.W	<ea>,CCR	1(0/0)	—	—	—	—	—	—	1(0/0)
MOVE.W	SR,Dx	1(0/0)	—	—	—	—	—	—	—
MOVE.W	<ea>,SR	7(0/0)	—	—	—	—	—	—	7(0/0) ²
MOVEC	Ry,Rc	9(0/1)	—	—	—	—	—	—	—
MOVEM.L	<ea>,and list	—	1+n(n/0)	—	—	1+n(n/0)	—	—	—
MOVEM.L	and list,<ea>	—	1+n(0/n)	—	—	1+n(0/n)	—	—	—
NOP		3(0/0)	—	—	—	—	—	—	—
PEA	<ea>	—	2(0/1)	—	—	2(0/1) ⁴	3(0/1) ⁵	2(0/1)	—
PULSE		1(0/0)	—	—	—	—	—	—	—
STLDSR	#imm	—	—	—	—	—	—	—	5(0/1)
STOP	#imm	—	—	—	—	—	—	—	3(0/0) ³
TRAP	#imm	—	—	—	—	—	—	—	15(1/2)
TPF		1(0/0)	—	—	—	—	—	—	—
TPF.W		1(0/0)	—	—	—	—	—	—	—
TPF.L		1(0/0)	—	—	—	—	—	—	—
UNLK	Ax	2(1/0)	—	—	—	—	—	—	—
WDDATA	<ea>	—	3(1/0)	3(1/0)	3(1/0)	3(1/0)	4(1/0)	3(1/0)	—
WDEBUB	<ea>	—	5(2/0)	—	—	5(2/0)	—	—	—

¹The n is the number of registers moved by the MOVEM opcode.

²If a MOVE.W #imm,SR instruction is executed and imm[13] equals 1, the execution time is 1(0/0).

³The execution time for STOP is the time required until the processor begins sampling continuously for interrupts.

⁴PEA execution times are the same for (d16,PC).

⁵PEA execution times are the same for (d8,PC,Xn*SF).

3.3.5.6 EMAC Instruction Execution Times

Table 3-17. EMAC Instruction Execution Times

Opcode	<EA>	Effective Address							
		Rn	(An)	(An)+	-(An)	(d16,An)	(d8,An, Xn*SF)	xxx.wl	#xxx
MAC.L	Ry, Rx, Raccx	1(0/0)	—	—	—	—	—	—	—
MAC.L	Ry, Rx, <ea>, Rw, Raccx	—	2(1/0)	2(1/0)	2(1/0)	2(1/0) ¹	—	—	—
MAC.W	Ry, Rx, Raccx	1(0/0)	—	—	—	—	—	—	—
MAC.W	Ry, Rx, <ea>, Rw, Raccx	—	2(1/0)	2(1/0)	2(1/0)	2(1/0) ¹	—	—	—
MOVE.L	<ea>y, Raccx	1(0/0)	—	—	—	—	—	—	1(0/0)
MOVE.L	Raccy,Raccx	1(0/0)	—	—	—	—	—	—	—
MOVE.L	<ea>y, MACSR	5(0/0)	—	—	—	—	—	—	5(0/0)
MOVE.L	<ea>y, Rmask	4(0/0)	—	—	—	—	—	—	4(0/0)
MOVE.L	<ea>y,Raccext01	1(0/0)	—	—	—	—	—	—	1(0/0)
MOVE.L	<ea>y,Raccext23	1(0/0)	—	—	—	—	—	—	1(0/0)
MOVE.L	Raccx,<ea>x	1(0/0) ²	—	—	—	—	—	—	—
MOVE.L	MACSR,<ea>x	1(0/0)	—	—	—	—	—	—	—
MOVE.L	Rmask, <ea>x	1(0/0)	—	—	—	—	—	—	—
MOVE.L	Raccext01,<ea>x	1(0/0)	—	—	—	—	—	—	—
MOVE.L	Raccext23,<ea>x	1(0/0)	—	—	—	—	—	—	—
MSAC.L	Ry, Rx, Raccx	1(0/0)	—	—	—	—	—	—	—
MSAC.W	Ry, Rx, Raccx	1(0/0)	—	—	—	—	—	—	—
MSAC.L	Ry, Rx, <ea>, Rw, Raccx	—	2(1/0)	2(1/0)	2(1/0)	2(1/0) ¹	—	—	—
MSAC.W	Ry, Rx, <ea>, Rw, Raccx	—	2(1/0)	2(1/0)	2(1/0)	2(1/0) ¹	—	—	—
MULS.L	<ea>y, Dx	4(0/0)	6(1/0)	6(1/0)	6(1/0)	6(1/0)	—	—	—
MULS.W	<ea>y, Dx	4(0/0)	6(1/0)	6(1/0)	6(1/0)	6(1/0)	7(1/0)	6(1/0)	4(0/0)
MULU.L	<ea>y, Dx	4(0/0)	6(1/0)	6(1/0)	6(1/0)	6(1/0)	—	—	—
MULU.W	<ea>y, Dx	4(0/0)	6(1/0)	6(1/0)	6(1/0)	6(1/0)	7(1/0)	6(1/0)	4(0/0)

¹ Effective address of (d16,PC) not supported

² Storing an accumulator requires one additional processor clock cycle when saturation is enabled, or fractional rounding is performed (MACSR[7:4] equals 1---, -11-, --11)

NOTE

The execution times for moving the contents of the Racc, Raccext[01,23], MACSR, or Rmask into a destination location <ea>x shown in this table represent the best-case scenario when the store instruction is executed and there are no load or M{S}AC instructions in the EMAC execution pipeline. In general, these store operations require only a single cycle for execution, but if preceded immediately by a load, MAC, or MSAC instruction, the depth of the EMAC pipeline is exposed and the execution time is four cycles.

3.3.5.7 Branch Instruction Execution Times

Table 3-18. General Branch Instruction Execution Times

Opcode	<EA>	Effective Address							
		Rn	(An)	(An)+	-(An)	(d16,An) (d16,PC)	(d8,An,Xi*SF) (d8,PC,Xi*SF)	xxx.wl	#xxx
BRA		—	—	—	—	2(0/1)	—	—	—
BSR		—	—	—	—	3(0/1)	—	—	—
JMP	<ea>	—	3(0/0)	—	—	3(0/0)	4(0/0)	3(0/0)	—
JSR	<ea>	—	3(0/1)	—	—	3(0/1)	4(0/1)	3(0/1)	—
RTE		—	—	10(2/0)	—	—	—	—	—
RTS		—	—	5(1/0)	—	—	—	—	—

Table 3-19. Bcc Instruction Execution Times

Opcode	Forward Taken	Forward Not Taken	Backward Taken	Backward Not Taken
Bcc	3(0/0)	1(0/0)	2(0/0)	3(0/0)

Chapter 4

Enhanced Multiply-Accumulate Unit (EMAC)

4.1 Introduction

This chapter describes the functionality, microarchitecture, and performance of the enhanced multiply-accumulate (EMAC) unit in the ColdFire family of processors.

4.1.1 Overview

The EMAC design provides a set of DSP operations that can improve the performance of embedded code while supporting the integer multiply instructions of the baseline ColdFire architecture.

The MAC provides functionality in three related areas:

1. Signed and unsigned integer multiplication
2. Multiply-accumulate operations supporting signed and unsigned integer operands as well as signed, fixed-point, and fractional operands
3. Miscellaneous register operations

The ColdFire family supports two MAC implementations with different performance levels and capabilities. The original MAC features a three-stage execution pipeline optimized for 16-bit operands, with a 16x16 multiply array and a single 32-bit accumulator. The EMAC features a four-stage pipeline optimized for 32-bit operands, with a fully pipelined 32×32 multiply array and four 48-bit accumulators.

The first ColdFire MAC supported signed and unsigned integer operands and was optimized for 16x16 operations, such as those found in applications including servo control and image compression. As ColdFire-based systems proliferated, the desire for more precision on input operands increased. The result was an improved ColdFire MAC with user-programmable control to optionally enable use of fractional input operands.

EMAC improvements target three primary areas:

- Improved performance of 32×32 multiply operation.
- Addition of three more accumulators to minimize MAC pipeline stalls caused by exchanges between the accumulator and the pipeline's general-purpose registers
- A 48-bit accumulation data path to allow a 40-bit product, plus 8 extension bits increase the dynamic number range when implementing signal processing algorithms

The three areas of functionality are addressed in detail in following sections. The logic required to support this functionality is contained in a MAC module ([Figure 4-1](#)).

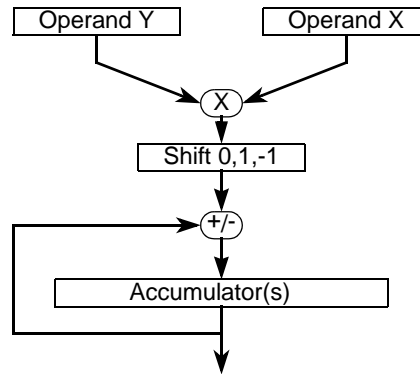


Figure 4-1. Multiply-Accumulate Functionality Diagram

4.1.1.1 Introduction to the MAC

The MAC is an extension of the basic multiplier in most microprocessors. It is typically implemented in hardware within an architecture and supports rapid execution of signal processing algorithms in fewer cycles than comparable non-MAC architectures. For example, small digital filters can tolerate some variance in an algorithm's execution time, but larger, more complicated algorithms such as orthogonal transforms may have more demanding speed requirements beyond scope of any processor architecture and may require full DSP implementation.

To balance speed, size, and functionality, the ColdFire MAC is optimized for a small set of operations that involve multiplication and cumulative additions. Specifically, the multiplier array is optimized for single-cycle pipelined operations with a possible accumulation after product generation. This functionality is common in many signal processing applications. The ColdFire core architecture is also modified to allow an operand to be fetched in parallel with a multiply, increasing overall performance for certain DSP operations.

Consider a typical filtering operation where the filter is defined as in [Equation 4-1](#).

$$y(i) = \sum_{k=1}^{N-1} a(k)y(i-k) + \sum_{k=0}^{N-1} b(k)x(i-k) \quad \text{Eqn. 4-1}$$

Here, the output $y(i)$ is determined by past output values and past input values. This is the general form of an infinite impulse response (IIR) filter. A finite impulse response (FIR) filter can be obtained by setting coefficients $a(k)$ to zero. In either case, the operations involved in computing such a filter are multiplies and product summing. To show this point, reduce [Equation 4-1](#) to a simple, four-tap FIR filter, shown in [Equation 4-2](#), in which the accumulated sum is a past data values and coefficients sum.

$$y(i) = \sum_{k=0}^3 b(k)x(i-k) = b(0)x(i) + b(1)x(i-1) + b(2)x(i-2) + b(3)x(i-3) \quad \text{Eqn. 4-2}$$

4.2 Memory Map/Register Definition

The following table and sections explain the MAC registers:

Table 4-1. EMAC Memory Map

BDM ¹	Register	Width (bits)	Access	Reset Value	Section/Page
0x804	MAC Status Register (MACSR)	32	R/W	0x0000_0000	4.2.1/4-3
0x805	MAC Address Mask Register (MASK)	32	R/W	0xFFFF_FFFF	4.2.2/4-5
0x806	MAC Accumulator 0 (ACC0)	32	R/W	Undefined	4.2.3/4-6
0x807	MAC Accumulator 0,1 Extension Bytes (ACCext01)	32	R/W	Undefined	4.2.4/4-7
0x808	MAC Accumulator 2,3 Extension Bytes (ACCext23)	32	R/W	Undefined	4.2.4/4-7
0x809	MAC Accumulator 1 (ACC1)	32	R/W	Undefined	4.2.3/4-6
0x80A	MAC Accumulator 2 (ACC2)	32	R/W	Undefined	4.2.3/4-6
0x80B	MAC Accumulator 3 (ACC3)	32	R/W	Undefined	4.2.3/4-6

¹ The values listed in this column represent the Rc field used when accessing the core registers via the BDM port. For more information see [Chapter 26, "Debug Module."](#)

4.2.1 MAC Status Register (MACSR)

The MAC status register (MACSR) contains a 4-bit operational mode field and condition flags. Operational mode bits control whether operands are signed or unsigned and whether they are treated as integers or fractions. These bits also control the overflow/saturation mode and the way in which rounding is performed. Negative, zero, and multiple overflow condition flags are also provided.

BDM: 0x804 (MACSR)

Access: Supervisor read/write
BDM read/write

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	PAV _n				OMC	S/U	F/I	R/T	N	Z	V	EV
W																																
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Figure 4-2. MAC Status Register (MACSR)

Table 4-2. MACSR Field Descriptions

Field	Description
31–12	Reserved, must be cleared.
11–8 PAV _n	Product/accumulation overflow flags. Contains four flags, one per accumulator, that indicate if past MAC or MSAC instructions generated an overflow during product calculation or the 48-bit accumulation. When a MAC or MSAC instruction is executed, the PAV _n flag associated with the destination accumulator is used to form the general overflow flag, MACSR[V]. Once set, each flag remains set until V is cleared by a <code>move.l, MACSR</code> instruction or the accumulator is loaded directly.

Table 4-2. MACSR Field Descriptions (continued)

Field	Description
7 OMC	Overflow saturation mode. Enables or disables saturation mode on overflow. If set, the accumulator is set to the appropriate constant (see S/U field description) on any operation that overflows the accumulator. After saturation, the accumulator remains unaffected by any other MAC or MSAC instructions until the overflow bit is cleared or the accumulator is directly loaded.
6 S/U	<p>Signed/unsigned operations.</p> <p>In integer mode: S/U determines whether operations performed are signed or unsigned. It also determines the accumulator value during saturation, if enabled.</p> <p>0 Signed numbers. On overflow, if OMC is enabled, an accumulator saturates to the most positive (0x7FFF_FFFF) or the most negative (0x8000_0000) number, depending on the instruction and the product value that overflowed.</p> <p>1 Unsigned numbers. On overflow, if OMC is enabled, an accumulator saturates to the smallest value (0x0000_0000) or the largest value (0xFFFF_FFFF), depending on the instruction.</p> <p>In fractional mode: S/U controls rounding while storing an accumulator to a general-purpose register.</p> <p>0 Move accumulator without rounding to a 16-bit value. Accumulator is moved to a general-purpose register as a 32-bit value.</p> <p>1 The accumulator is rounded to a 16-bit value using the round-to-nearest (even) method when moved to a general-purpose register. See Section 4.3.1.1, "Rounding". The resulting 16-bit value is stored in the lower word of the destination register. The upper word is zero-filled. This rounding procedure does not affect the accumulator value.</p>
5 F/I	<p>Fractional/integer mode. Determines whether input operands are treated as fractions or integers.</p> <p>0 Integers can be represented in signed or unsigned notation, depending on the value of S/U.</p> <p>1 Fractions are represented in signed, fixed-point, two's complement notation. Values range from -1 to $1 - 2^{-15}$ for 16-bit fractions and -1 to $1 - 2^{-31}$ for 32-bit fractions. See Section 4.3.4, "Data Representation."</p>
4 R/T	<p>Round/truncate mode. Controls rounding procedure for <code>move.l ACCx, Rx</code>, or MSAC.L instructions when in fractional mode.</p> <p>0 Truncate. The product's lsbs are dropped before it is combined with the accumulator. Additionally, when a store accumulator instruction is executed (<code>move.l ACCx, Rx</code>), the 8 lsbs of the 48-bit accumulator logic are truncated.</p> <p>1 Round-to-nearest (even). The 64-bit product of two 32-bit, fractional operands is rounded to the nearest 40-bit value. If the low-order 24 bits equal 0x80_0000, the upper 40 bits are rounded to the nearest even (lsb = 0) value. See Section 4.3.1.1, "Rounding". Additionally, when a store accumulator instruction is executed (<code>move.l ACCx, Rx</code>), the lsbs of the 48-bit accumulator logic round the resulting 16- or 32-bit value. If MACSR[S/U] is cleared and MACSR[R/T] is set, the low-order 8 bits are used to round the resulting 32-bit fraction. If MACSR[S/U] is set, the low-order 24 bits are used to round the resulting 16-bit fraction.</p>
3 N	Negative. Set if the msb of the result is set, otherwise cleared. N is affected only by MAC, MSAC, and load operations; it is not affected by MULS and MULU instructions.
2 Z	Zero. Set if the result equals zero, otherwise cleared. This bit is affected only by MAC, MSAC, and load operations; it is not affected by MULS and MULU instructions.

Table 4-2. MACSR Field Descriptions (continued)

Field	Description
1 V	Overflow. Set if an arithmetic overflow occurs on a MAC or MSAC instruction, indicating that the result cannot be represented in the limited width of the EMAC. V is set only if a product overflow occurs or the accumulation overflows the 48-bit structure. V is evaluated on each MAC or MSAC operation and uses the appropriate PAV _n flag in the next-state V evaluation.
0 EV	Extension overflow. Signals that the last MAC or MSAC instruction overflowed the 32 lsbs in integer mode or the 40 lsbs in fractional mode of the destination accumulator. However, the result remains accurately represented in the combined 48-bit accumulator structure. Although an overflow has occurred, the correct result, sign, and magnitude are contained in the 48-bit accumulator. Subsequent MAC or MSAC operations may return the accumulator to a valid 32/40-bit result.

Table 4-3 summarizes the interaction of the MACSR[S/U,F/I,R/T] control bits.

Table 4-3. Summary of S/U, F/I, and R/T Control Bits

S/U	F/I	R/T	Operational Modes
0	0	x	Signed, integer
0	1	0	Signed, fractional Truncate on MAC.L and MSAC.L No round on accumulator stores
0	1	1	Signed, fractional Round on MAC.L and MSAC.L Round-to-32-bits on accumulator stores
1	0	x	Unsigned, integer
1	1	0	Signed, fractional Truncate on MAC.L and MSAC.L Round-to-16-bits on accumulator stores
1	1	1	Signed, fractional Round on MAC.L and MSAC.L Round-to-16-bits on accumulator stores

4.2.2 Mask Register (MASK)

The 32-bit MASK implements the low-order 16 bits to minimize the alignment complications involved with loading and storing only 16 bits. When the MASK is loaded, the low-order 16 bits of the source operand are actually loaded into the register. When it is stored, the upper 16 bits are all forced to ones.

This register performs a simple AND with the operand address for MAC instructions. The processor calculates the normal operand address and, if enabled, that address is then ANDed with {0xFFFF, MASK[15:0]} to form the final address. Therefore, with certain MASK bits cleared, the operand address can be constrained to a certain memory region. This is used primarily to implement circular queues with the (An)+ addressing mode.

This minimizes the addressing support required for filtering, convolution, or any routine that implements a data array as a circular queue. For MAC + MOVE operations, the MASK contents can optionally be included in all memory effective address calculations. The syntax is as follows:

```
mac.sz Ry,RxSF,<ea>yand ,Rw
```

The `and` operator enables the MASK use and causes bit 5 of the extension word to be set. The exact algorithm for the use of MASK is:

```

if extension word, bit [5] = 1, the MASK bit, then
    if <ea> = (An)
        oa = An and {0xFFFF, MASK}

    if <ea> = (An)+
        oa = An
        An = (An + 4) and {0xFFFF, MASK}

    if <ea> = -(An)
        oa = (An - 4) and {0xFFFF, MASK}
        An = (An - 4) and {0xFFFF, MASK}

    if <ea> = (d16,An)
        oa = (An + se_d16) and {0xFFFF0x, MASK}

```

Here, *oa* is the calculated operand address and *se_d16* is a sign-extended 16-bit displacement. For auto-addressing modes of post-increment and pre-decrement, the updated *An* value calculation is also shown.

Use of the post-increment addressing mode, $\{(An)++\}$ with the MASK is suggested for circular queue implementations.

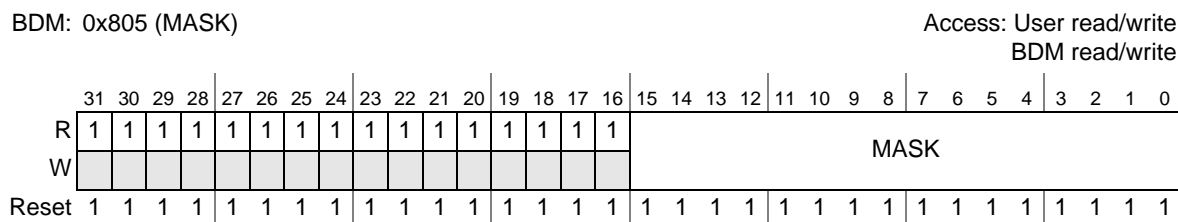


Figure 4-3. Mask Register (MASK)

Table 4-4. MASK Field Descriptions

Field	Description
31–16	Reserved, must be set.
15–0 MASK	Performs a simple AND with the operand address for MAC instructions.

4.2.3 Accumulator Registers (ACC0–3)

The accumulator registers store 32-bits of the MAC operation result. The accumulator extension registers form the entire 48-bit result.

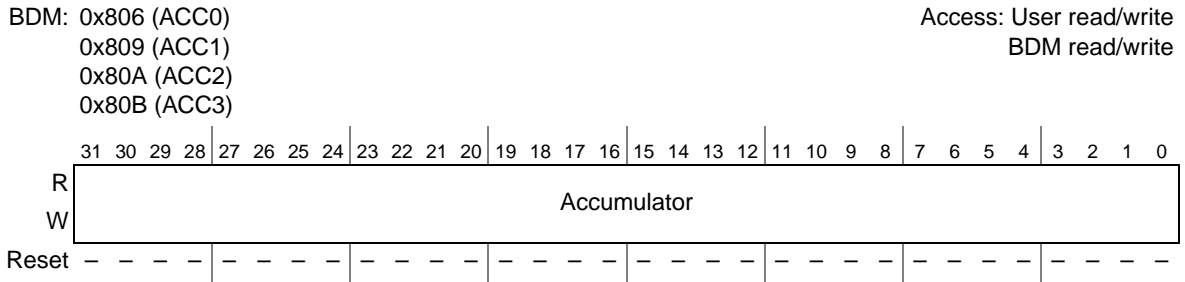


Figure 4-4. Accumulator Registers (ACC0–3)

Table 4-5. ACC0–3 Field Descriptions

Field	Description
31–0 Accumulator	Store 32-bits of the result of the MAC operation.

4.2.4 Accumulator Extension Registers (ACCext01, ACCext23)

Each pair of 8-bit accumulator extension fields are concatenated with the corresponding 32-bit accumulator register to form the 48-bit accumulator. For more information, see [Section 4.3, “Functional Description.”](#)

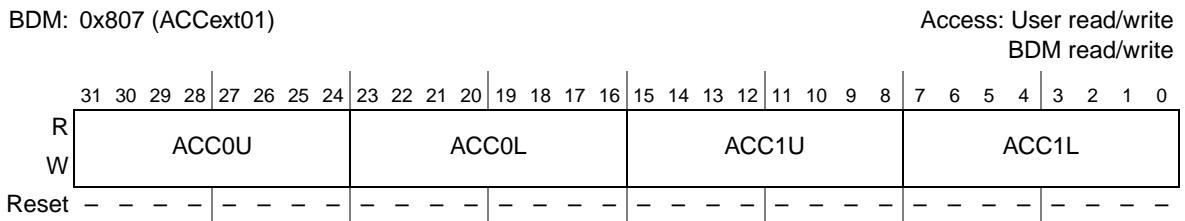
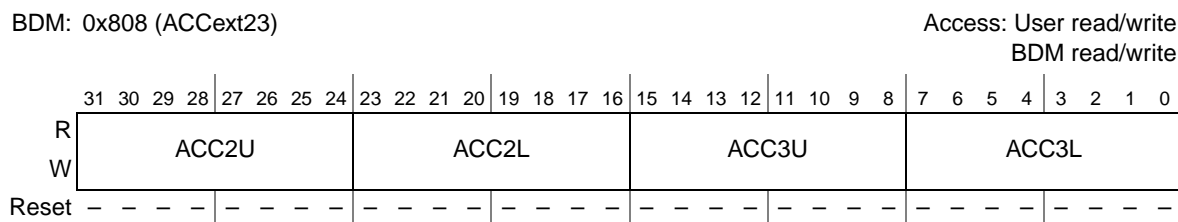


Figure 4-5. Accumulator Extension Register (ACCext01)

Table 4-6. ACCext01 Field Descriptions

Field	Description
31–24 ACC0U	Accumulator 0 upper extension byte
23–16 ACC0L	Accumulator 0 lower extension byte
15–8 ACC1U	Accumulator 1 upper extension byte
7–0 ACC1L	Accumulator 1 lower extension byte

**Figure 4-6. Accumulator Extension Register (ACCext23)****Table 4-7. ACCext23 Field Descriptions**

Field	Description
31–24 ACC2U	Accumulator 2 upper extension byte
23–16 ACC2L	Accumulator 2 lower extension byte
15–8 ACC3U	Accumulator 3 upper extension byte
7–0 ACC3L	Accumulator 3 lower extension byte

4.3 Functional Description

The MAC speeds execution of ColdFire integer-multiply instructions (MULS and MULU) and provides additional functionality for multiply-accumulate operations. By executing MULS and MULU in the MAC, execution times are minimized and deterministic compared to the 2-bit/cycle algorithm with early termination that the OEP normally uses if no MAC hardware is present.

The added MAC instructions to the ColdFire ISA provide for the multiplication of two numbers, followed by the addition or subtraction of the product to or from the value in an accumulator. Optionally, the product may be shifted left or right by 1 bit before addition or subtraction. Hardware support for saturation arithmetic can be enabled to minimize software overhead when dealing with potential overflow conditions. Multiply-accumulate operations support 16- or 32-bit input operands in these formats:

- Signed integers
- Unsigned integers
- Signed, fixed-point, fractional numbers

The EMAC is optimized for single-cycle, pipelined 32×32 multiplications. For word- and longword-sized integer input operands, the low-order 40 bits of the product are formed and used with the destination accumulator. For fractional operands, the entire 64-bit product is calculated and truncated or rounded to the most-significant 40-bit result using the round-to-nearest (even) method before it is combined with the destination accumulator.

For all operations, the resulting 40-bit product is extended to a 48-bit value (using sign-extension for signed integer and fractional operands, zero-fill for unsigned integer operands) before being combined with the 48-bit destination accumulator.

Figure 4-7 and Figure 4-8 show relative alignment of input operands, the full 64-bit product, the resulting 40-bit product used for accumulation, and 48-bit accumulator formats.

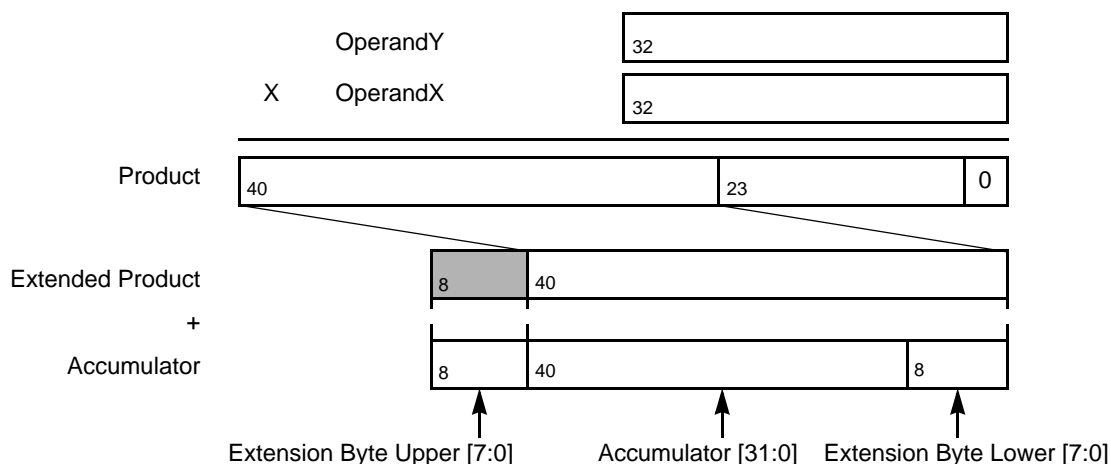


Figure 4-7. Fractional Alignment

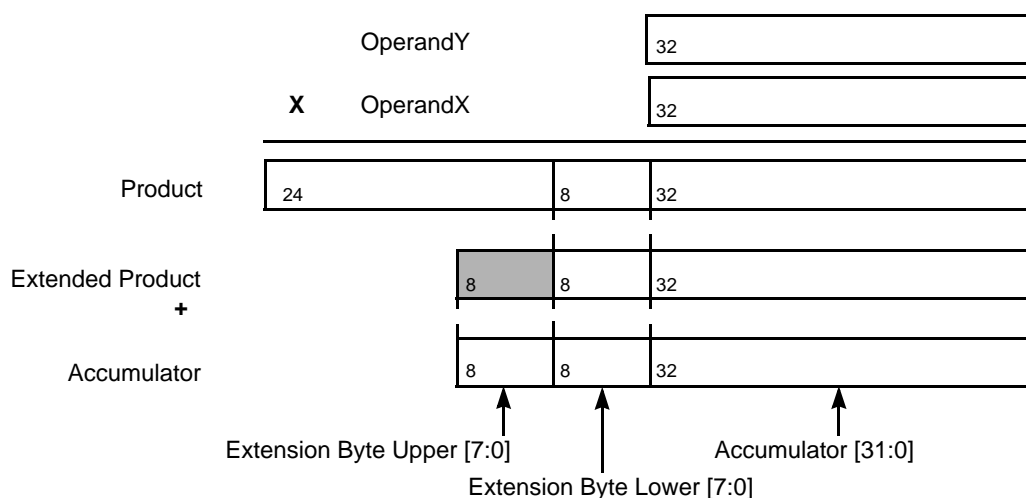


Figure 4-8. Signed and Unsigned Integer Alignment

Therefore, the 48-bit accumulator definition is a function of the EMAC operating mode. Given that each 48-bit accumulator is the concatenation of 16-bit accumulator extension register (ACCextn) contents and 32-bit ACCn contents, the specific definitions are:

```
if MACSR[6:5] == 00      /* signed integer mode */
    Complete Accumulator[47:0] = {ACCextn[15:0], ACCn[31:0]}
if MACSR[6:5] == 01 or 11 /* signed fractional mode */
    Complete Accumulator [47:0] = {ACCextn[15:8], ACCn[31:0], ACCextn[7:0]}
if MACSR[6:5] == 10      /* unsigned integer mode */
    Complete Accumulator[47:0] = {ACCextn[15:0], ACCn[31:0]}
```

The four accumulators are represented as an array, ACCn, where *n* selects the register.

Although the multiplier array is implemented in a four-stage pipeline, all arithmetic MAC instructions have an effective issue rate of 1 cycle, regardless of input operand size or type.

All arithmetic operations use register-based input operands, and summed values are stored in an accumulator. Therefore, an additional MOVE instruction is needed to store data in a general-purpose register. One new feature in EMAC instructions is the ability to choose the upper or lower word of a register as a 16-bit input operand. This is useful in filtering operations if one data register is loaded with the input data and another is loaded with the coefficient. Two 16-bit multiply accumulates can be performed without fetching additional operands between instructions by alternating word choice during calculations.

The EMAC has four accumulator registers versus the MAC's single accumulator. The additional registers improve the performance of some algorithms by minimizing pipeline stalls needed to store an accumulator value back to general-purpose registers. Many algorithms require multiple calculations on a given data set. By applying different accumulators to these calculations, it is often possible to store one accumulator without any stalls while performing operations involving a different destination accumulator.

The need to move large amounts of data presents an obstacle to obtaining high throughput rates in DSP engines. Existing ColdFire instructions can accommodate these requirements. A MOVEM instruction can efficiently move large data blocks by generating line-sized burst references. The ability to load an operand simultaneously from memory into a register and execute a MAC instruction makes some DSP operations such as filtering and convolution more manageable.

The programming model includes a mask register (MASK), which can optionally be used to generate an operand address during MAC + MOVE instructions. The register application with auto-increment addressing mode supports efficient implementation of circular data queues for memory operands.

4.3.1 Fractional Operation Mode

This section describes behavior when the fractional mode is used (MACSR[F/T] is set).

4.3.1.1 Rounding

When the processor is in fractional mode, there are two operations during which rounding can occur:

1. Execution of a store accumulator instruction (`move.l ACCx, Rx`). The lsbs of the 48-bit accumulator logic are used to round the resulting 16- or 32-bit value. If MACSR[S/U] is cleared, the low-order 8 bits round the resulting 32-bit fraction. If MACSR[S/U] is set, the low-order 24 bits are used to round the resulting 16-bit fraction.
2. Execution of a MAC (or MSAC) instruction with 32-bit operands. If MACSR[R/T] is zero, multiplying two 32-bit numbers creates a 64-bit product truncated to the upper 40 bits; otherwise, it is rounded using round-to-nearest (even) method.

To understand the round-to-nearest-even method, consider the following example involving the rounding of a 32-bit number, R0, to a 16-bit number. Using this method, the 32-bit number is rounded to the closest 16-bit number possible. Let the high-order 16 bits of R0 be named R0.U and the low-order 16 bits be R0.L.

- If R0.L is less than 0x8000, the result is truncated to the value of R0.U.
- If R0.L is greater than 0x8000, the upper word is incremented (rounded up).

- If R0.L is 0x8000, R0 is half-way between two 16-bit numbers. In this case, rounding is based on the lsb of R0.U, so the result is always even (lsb = 0).
 - If the lsb of R0.U equals 1 and R0.L equals 0x8000, the number is rounded up.
 - If the lsb of R0.U equals 0 and R0.L equals 0x8000, the number is rounded down.

This method minimizes rounding bias and creates as statistically correct an answer as possible.

The rounding algorithm is summarized in the following pseudocode:

```
if R0.L < 0x8000
    then Result = R0.U
else if R0.L > 0x8000
    then Result = R0.U + 1
else if lsb of R0.U = 0          /* R0.L = 0x8000 */
    then Result = R0.U
else Result = R0.U + 1
```

The round-to-nearest-even technique is also known as convergent rounding.

4.3.1.2 Saving and Restoring the EMAC Programming Model

The presence of rounding logic in the EMAC output datapath requires that special care during the EMAC's save/restore process. In particular, any result rounding modes must be disabled during the save/restore process so the exact bit-wise contents of the EMAC registers are accessed. Consider the memory structure containing the EMAC programming model:

```
struct macState {
    int acc0;
    int acc1;
    int acc2;
    int acc3;
    int accext01;
    int accext02;
    int mask;
    int macsr;
} macState;
```

The following assembly language routine shows the proper sequence for a correct EMAC state save. This code assumes all Dn and An registers are available for use, and the memory location of the state save is defined by A7.

```
EMAC_state_save:
    move.l    macsr,d7          ; save the macsr
    clr.l     d0                ; zero the register to ...
    move.l    d0,macsr          ; disable rounding in the macsr
    move.l    acc0,d0           ; save the accumulators
    move.l    acc1,d1
    move.l    acc2,d2
    move.l    acc3,d3
    move.l    accext01,d4       ; save the accumulator extensions
    move.l    accext23,d5
    move.l    mask,d6           ; save the address mask
    movem.l   #0x00ff,(a7)      ; move the state to memory
```

This code performs the EMAC state restore:

```
EMAC_state_restore:
```

```

movem.l (a7),#0x00ff      ; restore the state from memory
move.l  #0,macsr          ; disable rounding in the macsr
move.l  d0,acc0           ; restore the accumulators
move.l  d1,acc1
move.l  d2,acc2
move.l  d3,acc3
move.l  d4,accext01       ; restore the accumulator extensions
move.l  d5,accext23
move.l  d6,mask           ; restore the address mask
move.l  d7,macsr         ; restore the macsr

```

Executing this sequence type can correctly save and restore the exact state of the EMAC programming model.

4.3.1.3 MULS/MULU

MULS and MULU are unaffected by fractional-mode operation; operands remain assumed to be integers.

4.3.1.4 Scale Factor in MAC or MSAC Instructions

The scale factor is ignored while the MAC is in fractional mode.

4.3.2 EMAC Instruction Set Summary

Table 4-8 summarizes EMAC unit instructions.

Table 4-8. EMAC Instruction Summary

Command	Mnemonic	Description
Multiply Signed	<code>mul s <ea>y,Dx</code>	Multiplies two signed operands yielding a signed result
Multiply Unsigned	<code>mul u <ea>y,Dx</code>	Multiplies two unsigned operands yielding an unsigned result
Multiply Accumulate	<code>mac Ry,RxSF,ACCx</code> <code>msac Ry,RxSF,ACCx</code>	Multiplies two operands and adds/subtracts the product to/from an accumulator
Multiply Accumulate with Load	<code>mac Ry,Rx,<ea>y,Rw,ACCx</code> <code>msac Ry,Rx,<ea>y,Rw,ACCx</code>	Multiplies two operands and combines the product to an accumulator while loading a register with the memory operand
Load Accumulator	<code>move.l {Ry,#imm},ACCx</code>	Loads an accumulator with a 32-bit operand
Store Accumulator	<code>move.l ACCx,Rx</code>	Writes the contents of an accumulator to a CPU register
Copy Accumulator	<code>move.l ACCy,ACCx</code>	Copies a 48-bit accumulator
Load MACSR	<code>move.l {Ry,#imm},MACSR</code>	Writes a value to MACSR
Store MACSR	<code>move.l MACSR,Rx</code>	Write the contents of MACSR to a CPU register
Store MACSR to CCR	<code>move.l MACSR,CCR</code>	Write the contents of MACSR to the CCR
Load MAC Mask Reg	<code>move.l {Ry,#imm},MASK</code>	Writes a value to the MASK register
Store MAC Mask Reg	<code>move.l MASK,Rx</code>	Writes the contents of the MASK to a CPU register
Load Accumulator Extensions 01	<code>move.l {Ry,#imm},ACCext01</code>	Loads the accumulator 0,1 extension bytes with a 32-bit operand

Table 4-8. EMAC Instruction Summary (continued)

Command	Mnemonic	Description
Load Accumulator Extensions 23	<code>move.l {Ry,#imm},ACCext23</code>	Loads the accumulator 2,3 extension bytes with a 32-bit operand
Store Accumulator Extensions 01	<code>move.l ACCext01,Rx</code>	Writes the contents of accumulator 0,1 extension bytes into a CPU register
Store Accumulator Extensions 23	<code>move.l ACCext23,Rx</code>	Writes the contents of accumulator 2,3 extension bytes into a CPU register

4.3.3 EMAC Instruction Execution Times

The instruction execution times for the EMAC can be found in [Section 3.3.5.6, “EMAC Instruction Execution Times”](#).

The EMAC execution pipeline overlaps the AGEX stage of the OEP (the first stage of the EMAC pipeline is the last stage of the basic OEP). EMAC units are designed for sustained, fully-pipelined operation on accumulator load, copy, and multiply-accumulate instructions. However, instructions that store contents of the multiply-accumulate programming model can generate OEP stalls that expose the EMAC execution pipeline depth:

```
mac.w    Ry, Rx, Acc0
move.l   Acc0, Rz
```

The MOVE.L instruction that stores the accumulator to an integer register (Rz) stalls until the program-visible copy of the accumulator is available. [Figure 4-9](#) shows EMAC timing.

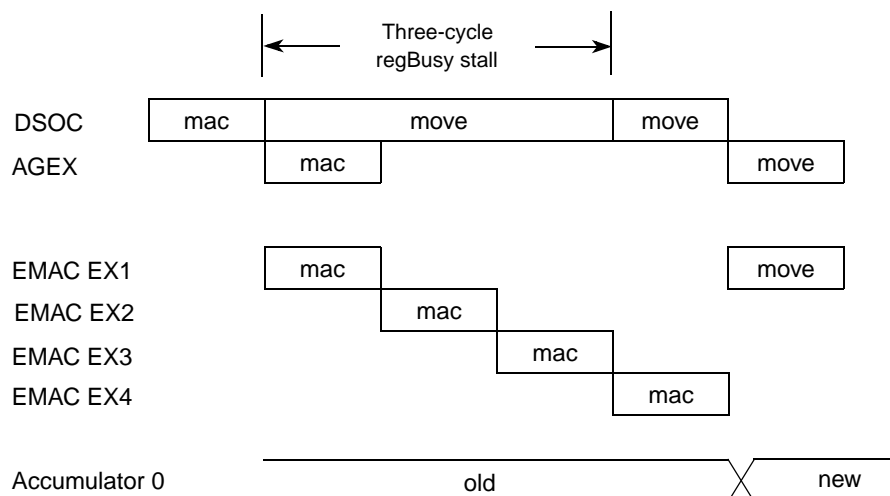


Figure 4-9. EMAC-Specific OEP Sequence Stall

In [Figure 4-9](#), the OEP stalls the store-accumulator instruction for three cycles: the EMAC pipeline depth minus 1. The minus 1 factor is needed because the OEP and EMAC pipelines overlap by a cycle, the AGEX stage. As the store-accumulator instruction reaches the AGEX stage where the operation is performed, the recently updated accumulator 0 value is available.

As with change or use stalls between accumulators and general-purpose registers, introducing intervening instructions that do not reference the busy register can reduce or eliminate sequence-related store-MAC instruction stalls. A major benefit of the EMAC is the addition of three accumulators to minimize stalls caused by exchanges between accumulator(s) and general-purpose registers.

4.3.4 Data Representation

MACSR[S/U,F/I] selects one of the following three modes, where each mode defines a unique operand type:

1. Two's complement signed integer: In this format, an N-bit operand value lies in the range $-2^{(N-1)} \leq \text{operand} \leq 2^{(N-1)} - 1$. The binary point is right of the lsb.
2. Unsigned integer: In this format, an N-bit operand value lies in the range $0 \leq \text{operand} \leq 2^N - 1$. The binary point is right of the lsb.
3. Two's complement, signed fractional: In an N-bit number, the first bit is the sign bit. The remaining bits signify the first N-1 bits after the binary point. Given an N-bit number, $a_{N-1}a_{N-2}a_{N-3}...a_2a_1a_0$, its value is given by the equation in [Equation 4-3](#).

$$\text{value} = -(1 \cdot a_{N-1}) + \sum_{i=0}^{N-2} 2^{-(i+1-N)} \cdot a_i \quad \text{Eqn. 4-3}$$

This format can represent numbers in the range $-1 \leq \text{operand} \leq 1 - 2^{(N-1)}$.

For words and longwords, the largest negative number that can be represented is -1, whose internal representation is 0x8000 and 0x8000_0000, respectively. The largest positive word is 0x7FFF or $(1 - 2^{-15})$; the most positive longword is 0x7FFF_FFFF or $(1 - 2^{-31})$.

4.3.5 MAC Opcodes

MAC opcodes are described in the *ColdFire Programmer's Reference Manual*.

Remember the following:

- Unless otherwise noted, the value of MACSR[N,Z] is based on the result of the final operation that involves the product and the accumulator.
- The overflow (V) flag is managed differently. It is set if the complete product cannot be represented as a 40-bit value (this applies to 32×32 integer operations only) or if the combination of the product with an accumulator cannot be represented in the given number of bits. The EMAC design includes an additional product/accumulation overflow bit for each accumulator that are treated as sticky indicators and are used to calculate the V bit on each MAC or MSAC instruction. See [Section 4.2.1, "MAC Status Register \(MACSR\)"](#).
- For the MAC design, the assembler syntax of the MAC (multiply and add to accumulator) and MSAC (multiply and subtract from accumulator) instructions does not include a reference to the single accumulator. For the EMAC, assemblers support this syntax and no explicit reference to an accumulator is interpreted as a reference to ACC0. Assemblers also support syntaxes where the destination accumulator is explicitly defined.

- The optional 1-bit shift of the product is specified using the notation {<<|>>} SF, where <<1 indicates a left shift and >>1 indicates a right shift. The shift is performed before the product is added to or subtracted from the accumulator. Without this operator, the product is not shifted. If the EMAC is in fractional mode (MACSR[F/I] is set), SF is ignored and no shift is performed. Because a product can overflow, the following guidelines are implemented:
 - For unsigned word and longword operations, a zero is shifted into the product on right shifts.
 - For signed, word operations, the sign bit is shifted into the product on right shifts unless the product is zero. For signed, longword operations, the sign bit is shifted into the product unless an overflow occurs or the product is zero, in which case a zero is shifted in.
 - For all left shifts, a zero is inserted into the lsb position.

The following pseudocode explains basic MAC or MSAC instruction functionality. This example is presented as a case statement covering the three basic operating modes with signed integers, unsigned integers, and signed fractionals. Throughout this example, a comma-separated list in curly brackets, {}, indicates a concatenation operation.

```
switch (MACSR[6:5])      /* MACSR[S/U, F/I] */
{
  case 0:                /* signed integers */
    if (MACSR.OMC == 0 || MACSR.PAVn == 0)
      then {
        MACSR.PAVn = 0
        /* select the input operands */
        if (sz == word)
          then {if (U/Ly == 1)
                  then operandY[31:0] = {sign-extended Ry[31], Ry[31:16]}
                  else operandY[31:0] = {sign-extended Ry[15], Ry[15:0]}
                if (U/Lx == 1)
                  then operandX[31:0] = {sign-extended Rx[31], Rx[31:16]}
                  else operandX[31:0] = {sign-extended Rx[15], Rx[15:0]}
              }
          else {operandY[31:0] = Ry[31:0]
                operandX[31:0] = Rx[31:0]
              }

          /* perform the multiply */
          product[63:0] = operandY[31:0] * operandX[31:0]

          /* check for product overflow */
          if ((product[63:39] != 0x0000_00_0) and and (product[63:39] != 0xffff_ff_1))
            then {          /* product overflow */
              MACSR.PAVn = 1
              MACSR.V = 1
              if (inst == MSAC and and MACSR.OMC == 1)
                then if (product[63] == 1)
                      then result[47:0] = 0x0000_7fff_ffff
                      else result[47:0] = 0xffff_8000_0000
                else if (MACSR.OMC == 1)
                      then /* overflowed MAC,
                           saturationMode enabled */
                           if (product[63] == 1)
                             then result[47:0] = 0xffff_8000_0000
                             else result[47:0] = 0x0000_7fff_ffff
            }
      }
}
```

```

/* sign-extend to 48 bits before performing any scaling */
product[47:40] = {8{product[39]}} /* sign-extend */

/* scale product before combining with accumulator */
switch (SF) /* 2-bit scale factor */
{
    case 0: /* no scaling specified */
        break;
    case 1: /* SF = "<< 1" */
        product[40:0] = {product[39:0], 0}
        break;
    case 2: /* reserved encoding */
        break;
    case 3: /* SF = ">> 1" */
        product[39:0] = {product[39], product[39:1]}
        break;
}

if (MACSR.PAVn == 0)
    then {if (inst == MSAC)
        then result[47:0] = ACCx[47:0] - product[47:0]
        else result[47:0] = ACCx[47:0] + product[47:0]
    }

/* check for accumulation overflow */
if (accumulationOverflow == 1)
    then {MACSR.PAVn = 1
        MACSR.V = 1
        if (MACSR.OMC == 1)
            then /* accumulation overflow,
                saturationMode enabled */
                if (result[47] == 1)
                    then result[47:0] = 0x0000_7fff_ffff
                    else result[47:0] = 0xffff_8000_0000
            }
    }

/* transfer the result to the accumulator */
ACCx[47:0] = result[47:0]
}
MACSR.V = MACSR.PAVn
MACSR.N = ACCx[47]
if (ACCx[47:0] == 0x0000_0000_0000)
    then MACSR.Z = 1
    else MACSR.Z = 0
if ((ACCx[47:31] == 0x0000_0) || (ACCx[47:31] == 0xffff_1))
    then MACSR.EV = 0
    else MACSR.EV = 1
break;

case 1,3: /* signed fractionals */
if (MACSR.OMC == 0 || MACSR.PAVn == 0)
    then {
        MACSR.PAVn = 0
        if (sz == word)
            then {if (U/Ly == 1)
                then operandY[31:0] = {Ry[31:16], 0x0000}
                else operandY[31:0] = {Ry[15:0], 0x0000}
            }
            if (U/Lx == 1)

```

```

        then operandX[31:0] = {Rx[31:16], 0x0000}
        else operandX[31:0] = {Rx[15:0], 0x0000}
    }
    else {operandY[31:0] = Ry[31:0]
        operandX[31:0] = Rx[31:0]
    }
    /* perform the multiply */
    product[63:0] = (operandY[31:0] * operandX[31:0]) << 1
    /* check for product rounding */
    if (MACSR.R/T == 1)
    then { /* perform convergent rounding */
        if (product[23:0] > 0x80_0000)
            then product[63:24] = product[63:24] + 1
        else if ((product[23:0] == 0x80_0000) and and (product[24] == 1))
            then product[63:24] = product[63:24] + 1
    }
    /* sign-extend to 48 bits and combine with accumulator */
    /* check for the -1 * -1 overflow case */
    if ((operandY[31:0] == 0x8000_0000) and and (operandX[31:0] == 0x8000_0000))
    then product[71:64] = 0x00 /* zero-fill */
    else product[71:64] = {8{product[63]}} /* sign-extend */
    if (inst == MSAC)
    then result[47:0] = ACCx[47:0] - product[71:24]
    else result[47:0] = ACCx[47:0] + product[71:24]
    /* check for accumulation overflow */
    if (accumulationOverflow == 1)
    then {MACSR.PAVn = 1
        MACSR.V = 1
        if (MACSR.OMC == 1)
        then /* accumulation overflow,
            saturationMode enabled */
            if (result[47] == 1)
            then result[47:0] = 0x007f_ffff_ff00
            else result[47:0] = 0xff80_0000_0000
        }
    /* transfer the result to the accumulator */
    ACCx[47:0] = result[47:0]
    }
    MACSR.V = MACSR.PAVn
    MACSR.N = ACCx[47]
    if (ACCx[47:0] == 0x0000_0000_0000)
    then MACSR.Z = 1
    else MACSR.Z = 0
    if ((ACCx[47:39] == 0x00_0) || (ACCx[47:39] == 0xff_1))
    then MACSR.EV = 0
    else MACSR.EV = 1
break;
case 2: /* unsigned integers */
    if (MACSR.OMC == 0 || MACSR.PAVn == 0)
    then {
        MACSR.PAVn = 0
        /* select the input operands */
        if (sz == word)
        then {if (U/Ly == 1)
            then operandY[31:0] = {0x0000, Ry[31:16]}
            else operandY[31:0] = {0x0000, Ry[15:0]}
            if (U/Lx == 1)

```

```

        then operandX[31:0] = {0x0000, Rx[31:16]}
        else operandX[31:0] = {0x0000, Rx[15:0]}
    }
    else {operandY[31:0] = Ry[31:0]
        operandX[31:0] = Rx[31:0]
    }

    /* perform the multiply */
    product[63:0] = operandY[31:0] * operandX[31:0]

    /* check for product overflow */
    if (product[63:40] != 0x0000_00)
    then {
        /* product overflow */
        MACSR.PAVn = 1
        MACSR.V = 1
        if (inst == MSAC and and MACSR.OMC == 1)
        then result[47:0] = 0x0000_0000_0000
        else if (MACSR.OMC == 1)
        then /* overflowed MAC,
            saturationMode enabled */
            result[47:0] = 0xffff_ffff_ffff
    }

    /* zero-fill to 48 bits before performing any scaling */
    product[47:40] = 0 /* zero-fill upper byte */

    /* scale product before combining with accumulator */
    switch (SF) /* 2-bit scale factor */
    {
        case 0: /* no scaling specified */
            break;
        case 1: /* SF = "<< 1" */
            product[40:0] = {product[39:0], 0}
            break;
        case 2: /* reserved encoding */
            break;
        case 3: /* SF = ">> 1" */
            product[39:0] = {0, product[39:1]}
            break;
    }

    /* combine with accumulator */
    if (MACSR.PAVn == 0)
    then {if (inst == MSAC)
        then result[47:0] = ACCx[47:0] - product[47:0]
        else result[47:0] = ACCx[47:0] + product[47:0]
    }

    /* check for accumulation overflow */
    if (accumulationOverflow == 1)
    then {MACSR.PAVn = 1
        MACSR.V = 1
        if (inst == MSAC and and MACSR.OMC == 1)
        then result[47:0] = 0x0000_0000_0000
        else if (MACSR.OMC == 1)
        then /* overflowed MAC,
            saturationMode enabled */

```

```
        result[47:0] = 0xffff_ffff_ffff

    }

    /* transfer the result to the accumulator */
    ACCx[47:0] = result[47:0]
}
MACSR.V = MACSR.PAVn
MACSR.N = ACCx[47]
if (ACCx[47:0] == 0x0000_0000_0000)
    then MACSR.Z = 1
    else MACSR.Z = 0
if (ACCx[47:32] == 0x0000)
    then MACSR.EV = 0
    else MACSR.EV = 1
break;
}
```


Chapter 5

Cache

5.1 Introduction

This chapter describes cache operation on the ColdFire processor.

5.1.1 Features

Features include the following:

- Configurable as instruction, data, or split instruction/data cache
- 8-Kbyte direct-mapped cache
- Single-cycle access on cache hits
- Physically located on the ColdFire core's high-speed local bus
- Nonblocking design to maximize performance
- Separate instruction and data 16-Byte line-fill buffers
- Configurable instruction cache miss-fetch algorithm

5.1.2 Introduction

The cache is a direct-mapped, single-cycle memory. It may be configured as an instruction cache, a write-through data cache, or a split instruction/data cache. The cache storage is organized as 512 lines, each containing 16 bytes. The memory storage consists of a 512-entry tag array (containing addresses and a valid bit), and a data array containing 8 Kbytes, organized as 2048×32 bits.

Cache configuration is controlled by bits in the cache control register (CACR), detailed later in this chapter. For the instruction or data-only configurations, only the associated instruction or data line-fill buffer is used. For the split cache configuration, one-half of the tag and storage arrays is used for an instruction cache and one-half is used for a data cache. The split cache configuration uses the instruction and the data line-fill buffers. The core's local bus is a unified bus used for instruction and data fetches. Therefore, the cache can have only one fetch, instruction or data, active at one time.

For the instruction- or data-only configurations, the cache tag and storage arrays are accessed in parallel: fetch address bits [12:4] addressing the tag array, and fetch address bits [12:2] addressing the storage array. For the split cache configuration, the cache tag and storage arrays are accessed in parallel. The msb of the tag array address is set for instruction fetches and cleared for operand fetches; fetch address bits [11:4] provide the rest of the tag array address. The tag array outputs the address mapped to the given cache location along with the valid bit for the line. This address field is compared to bits [31:13] for instruction- or data-only configurations and to bits [31:12] for a split configuration of the fetch address from the local bus to determine if a cache hit has occurred. If the desired address is mapped into the cache memory, the

output of the storage array is driven onto the ColdFire core's local data bus, thereby completing the access in a single cycle.

The tag array maintains a single valid bit per line entry. Accordingly, only entire 16-byte lines are loaded into the cache.

The cache also contains separate 16-byte instruction and data line-fill buffers that provide temporary storage for the last line fetched in response to a cache miss. With each fetch, the contents of the associated line fill buffer are examined. Thus, each fetch address examines the tag memory array and the associated line fill buffer to see if the desired address is mapped into either hardware resource. A cache hit in the memory array or the associated line-fill buffer is serviced in a single cycle. Because the line fill buffer maintains valid bits on a longword basis, hits in the buffer can be serviced immediately without waiting for the entire line to be fetched.

If the referenced address is not contained in the memory array or the associated line-fill buffer, the cache initiates the required external fetch operation. In most situations, this is a 16-byte line-sized burst reference.

The hardware implementation is a nonblocking design, meaning the ColdFire core's local bus is released after the initial access of a miss. Thus, the cache or the SRAM module can service subsequent requests while the remainder of the line is being fetched and loaded into the fill buffer.

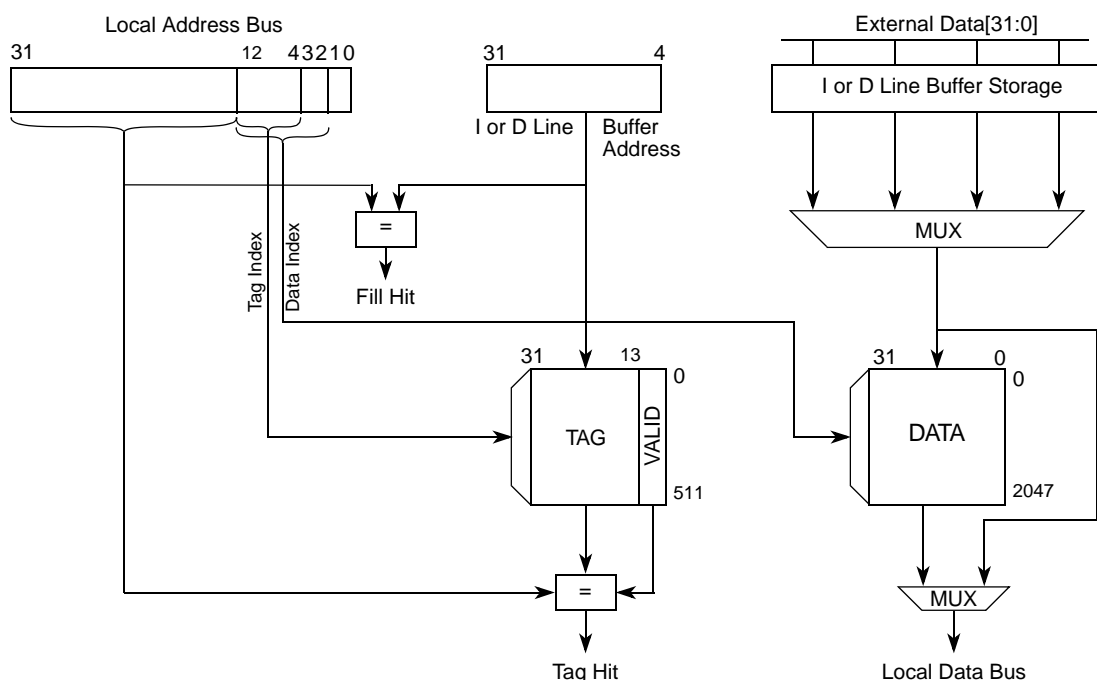


Figure 5-1. 8-Kbyte Cache Block Diagram

5.2 Memory Map/Register Definition

Three supervisor registers define the operation of the cache and local bus controller: the cache control register (CACR) and two access control registers (ACR0, ACR1). [Table 5-1](#) below shows the memory map

of these registers. The CACR and ACRs can only be accessed in supervisor mode using the MOVEC instruction with an Rc value of 0x002, 0x004 and 0x005, respectively.

Table 5-1. Cache Memory Map

BDM ¹	Register	Width (bits)	Access ²	Reset Value	Section/Page
0x002	Cache Control Register (CACR)	32	W	0x0000_0000	5.2.1/5-3
0x004	Access Control Register 0 (ACR0)	32	W	See Section	5.2.2/5-6
0x005	Access Control Register 1 (ACR1)	32	W	See Section	5.2.2/5-6

¹ The values listed in this column represent the Rc field used when accessing the core registers via the BDM port. For more information see [Chapter 26, “Debug Module.”](#)

² Readable through debug.

5.2.1 Cache Control Register (CACR)

The CACR controls the operation of the cache. The CACR provides a set of default memory access attributes used when a reference address does not map into the spaces defined by the ACRs.

The CACR is a 32-bit, write-only supervisor control register. It is accessed in the CPU address space via the MOVEC instruction with an Rc encoding of 0x002. The CACR can be read when in background debug mode (BDM). Therefore, the register diagram, [Figure 5-2](#), is shown as read/write. At system reset, the entire register is cleared.

BDM: 0x002 (CACR)

Access: Supervisor write-only
Debug read/write

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
R	CENB	0	0	CPD	CFRZ	0	0	CINV	DISI	DISD	INVI	INVD	0	0	0	0
W																
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	0	0	0	0	0	CEIB	DCM	DBWE	0	0	DWP	EUSP	0	0		
W																CLNF
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Figure 5-2. Cache Control Register (CACR)

Table 5-2. CACR Field Descriptions

Field	Description
31 CENB	Cache enable. The memory array of the cache is enabled only if CENB is asserted. This bit, along with the DISI (disable instruction caching) and DISD (disable data caching) bits, control the cache configuration. 0 Cache disabled 1 Cache enabled Table 5-3 describes cache configuration.
30–29	Reserved, must be cleared.

Table 5-2. CACR Field Descriptions (continued)

Field	Description
28 CPDI	Disable CPUSHL invalidation. When the privileged CPUSHL instruction is executed, the cache entry defined by bits [12:4] of the address is invalidated if CPDI is cleared. If CPDI is set, no operation is performed. 0 Enable invalidation 1 Disable invalidation
27 CFRZ	Cache freeze. This field allows the user to freeze the contents of the cache. When CFRZ is asserted line fetches can be initiated and loaded into the line-fill buffer, but a valid cache entry can not be overwritten. If a given cache location is invalid, the contents of the line-fill buffer can be written into the memory array while CFRZ is asserted. 0 Normal Operation 1 Freeze valid cache lines
26–25	Reserved, must be cleared.
24 CINV	Cache invalidate. The cache invalidate operation is not a function of the CENB state (this operation is independent of the cache being enabled or disabled). Setting this bit forces the cache to invalidate all, half, or none of the tag array entries depending on the state of the DISI, DISD, INVI, and INVD bits. The invalidation process requires several cycles of overhead plus 512 machine cycles to clear all tag array entries and 256 cycles to clear half of the tag array entries, with a single cache entry cleared per machine cycle. The state of this bit is always read as a zero. After a hardware reset, the cache must be invalidated before it is enabled. 0 No operation 1 Invalidate all cache locations Table 5-4 describes how to set the cache invalidate all bit.
23 DISI	Disable instruction caching. When set, this bit disables instruction caching. This bit, along with the CENB (cache enable) and DISD (disable data caching) bits, control the cache configuration. See the CENB definition for a detailed description. 0 Enable instruction caching 1 Disable instruction caching Table 5-3 describes cache configuration and Table 5-4 describes how to set the cache invalidate all bit.
22 DISD	Disable data caching. When set, this bit disables data caching. This bit, along with the CENB (cache enable) and DISI (disable instruction caching) bits, control the cache configuration. See the CENB definition for a detailed description. 0 Enable data caching 1 Disable data caching Table 5-3 describes cache configuration and Table 5-4 describes how to set the cache invalidate all bit.
21 INVI	CINV instruction cache only. This bit can not be set unless the cache configuration is split (DISI and DISD cleared). For instruction or data cache configurations this bit is a don't-care. For the split cache configuration, this bit is part of the control for the invalidate all operation. See the CINV definition for a detailed description Table 5-4 describes how to set the cache invalidate all bit.
20 INVD	CINV data cache only. This bit can not be set unless the cache configuration is split (DISI and DISD cleared). For instruction or data cache configurations this bit is a don't-care. For the split cache configuration, this bit is part of the control for the invalidate all operation. See the CINV definition for a detailed description Table 5-4 describes how to set the cache invalidate all bit.
19–11	Reserved, must be cleared.
10 CEIB	Cache enable non-cacheable instruction bursting. Setting this bit enables the line-fill buffer to be loaded with burst transfers under control of CLNF[1:0] for non-cacheable accesses. Non-cacheable accesses are never written into the memory array. See Table 5-7 . 0 Disable burst fetches on non-cacheable accesses 1 Enable burst fetches on non-cacheable accesses

Table 5-2. CACR Field Descriptions (continued)

Field	Description
9 DCM	Default cache mode. This bit defines the default cache mode. For more information on the selection of the effective memory attributes, see Section 5.3.2, “Memory Reference Attributes . 0 Caching enabled 1 Caching disabled
8 DBWE	Default buffered write enable. This bit defines the default value for enabling buffered writes. If DBWE = 0, the termination of an operand write cycle on the processor's local bus is delayed until the external bus cycle is completed. If DBWE = 1, the write cycle on the local bus is terminated immediately and the operation buffered in the bus controller. In this mode, operand write cycles are effectively decoupled between the processor's local bus and the external bus. Generally, enabled buffered writes provide higher system performance but recovery from access errors can be more difficult. For the ColdFire core, reporting access errors on operand writes is always imprecise and enabling buffered writes further decouples the write instruction and the signaling of the fault 0 Disable buffered writes 1 Enable buffered writes
7–6	Reserved, must be cleared.
5 DWP	Default write protection 0 Read and write accesses permitted 1 Only read accesses permitted
4 EUSP	Enable user stack pointer. See Section 3.2.3, “Supervisor/User Stack Pointers (A7 and OTHER_A7)” for more information on the dual stack pointer implementation. 0 Disable the processor's use of the User Stack Pointer 1 Enable the processor's use of the User Stack Pointer
3–2	Reserved, must be cleared.
1–0 CLNF	Cache line fill. These bits control the size of the memory request the cache issues to the bus controller for different initial instruction line access offsets. See Table 5-6 for external fetch size based on miss address and CLNF.

[Table 5-3](#) shows the relationship between CACR[CENB, DISI, & DISD] bits and the cache configuration.

Table 5-3. Cache Configuration as Defined by CACR

CACR [CENB]	CACR [DISI]	CACR [DISD]	Configuration	Description
0	x	x	N/A	Cache is completely disabled
1	0	0	Split Instruction/ Data Cache	4 KByte direct-mapped instruction cache (uses upper half of tag and storage arrays) and 4 KByte direct-mapped write-through data cache (uses lower half of tag and storage arrays)
1	0	1	Instruction Cache	8 KByte direct-mapped instruction cache (uses all of tag and storage arrays)
1	1	0	Data Cache	8 KByte direct-mapped write-through data cache (uses all of tag and storage arrays)

[Table 5-4](#) shows the relationship between CACR[DISI, DISD, INVI, & INVD] and setting the cache invalidate all bit (CACR[CINV]).

Table 5-4. Cache Invalidate All as Defined by CACR

CACR [DISI]	CACR [DISD]	CACR [INVI]	CACR [INVD]	Configuration	Operation
0	0	0	0	Split Instruction/ Data Cache	Invalidate all entries in 4-KByte instruction cache and 4-KByte data cache
0	0	0	1	Split Instruction/ Data Cache	Invalidate only 4 KByte data cache
0	0	1	0	Split Instruction Data Cache	Invalidate only 4 KByte instruction cache
0	0	1	1	Split Instruction/ Data Cache	No invalidate
1	0	x	x	Instruction Cache	Invalidate 8 KByte instruction cache
0	1	x	x	Data Cache	Invalidate 8 KByte data cache

5.2.2 Access Control Registers (ACR0, ACR1)

The ACRs provide a definition of memory reference attributes for two memory regions (one per ACR). This set of effective attributes is defined for every memory reference using the ACRs or the set of default attributes contained in the CACR. The ACRs are examined for every processor memory reference not mapped to the SRAM memories.

The ACRs are 32-bit, write-only supervisor control register. They are accessed in the CPU address space via the MOVEC instruction with an Rc encoding of 0x004 and 0x005. The ACRs can be read when in background debug mode (BDM). Therefore, the register diagram, Figure 5-3, is shown as read/write. At system reset, both registers are disabled with ACR_n[EN] cleared.

NOTE

Peripheral space (0xE000_0000-0xFFFF_FFFF) should not be cached. The combination of the CACR defaults and the two ACR_n registers must define the non-cacheable attribute for this address space.

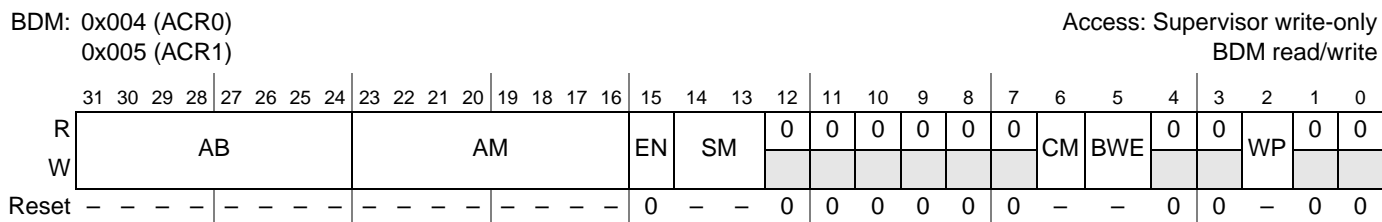
Figure 5-3. Access Control Registers (ACR_n)

Table 5-5. ACR_n Field Descriptions

Field	Description
31–24 AB	Address base. This 8-bit field is compared to address bits [31:24] from the processor's local bus under control of the ACR address mask. If the address matches, the attributes for the memory reference are sourced from the given ACR.
23–16 AM	Address mask. Masks any AB bit. If a bit in the AM field is set, the corresponding bit of the address field comparison is ignored.
15 EN	ACR Enable. Hardware reset clears this bit, disabling the ACR. 0 ACR disabled 1 ACR enabled
14–13 SM	Supervisor mode. Allows the given ACR to be applied to references based on operating privilege mode of the ColdFire processor. The field uses the ACR for user references only, supervisor references only, or all accesses. 00 Match if user mode 01 Match if supervisor mode 1x Match always—ignore user/supervisor mode
12–7	Reserved, must be cleared.
6 CM	Cache mode. 0 Caching enabled 1 Caching disabled
5 BWE	Buffered write enable. Defines the value for enabling buffered writes. If BWE is cleared, the termination of an operand write cycle on the processor's local bus is delayed until the system bus cycle is completed. Setting BWE terminates the write cycle on the local bus immediately and the operation is then buffered in the bus controller. In this mode, operand write cycles are effectively decoupled between the processor's local bus and the system bus. Generally, the enabling of buffered writes provides higher system performance but recovery from access errors may be more difficult. For the V2 ColdFire core, the reporting of access errors on operand writes is always imprecise, and enabling buffered writes simply decouples the write instruction from the signaling of the fault even more. 0 Writes are not buffered. 1 Writes are buffered.
4–3	Reserved, must be cleared.
2 WP	Write protect. Defines the write-protection attribute. If the effective memory attributes for a given access select the WP bit, an access error terminates any attempted write with this bit set. 0 Read and write accesses permitted 1 Only read accesses permitted
1–0	Reserved, must be cleared.

5.3 Functional Description

The cache is physically connected to the ColdFire core's local bus, allowing it to service all fetches from the ColdFire core and certain memory fetches initiated by the debug module. Typically, the debug module's memory references appear as supervisor data accesses but the unit can be programmed to generate user-mode accesses and/or instruction fetches. The cache processes any fetch access in the normal manner.

5.3.1 Interaction with Other Modules

Because the cache and high-speed SRAM module are connected to the ColdFire core's local data bus, certain user-defined configurations can result in simultaneous fetch processing.

If the referenced address is mapped into the SRAM module, that module services the request in a single cycle. In this case, data accessed from the cache is simply discarded and no external memory references are generated. If the address is not mapped into the SRAM space, the cache handles the request in the normal fashion.

5.3.2 Memory Reference Attributes

For every memory reference the ColdFire core or the debug module generates, a set of effective attributes is determined based on the address and the access control registers (ACRs). This set of attributes includes the cacheable/non-cacheable definition, the precise/imprecise handling of operand write, and the write-protect capability.

In particular, each address is compared to the values programmed in the ACRs. If the address matches one of the ACR values, the access attributes from that ACR are applied to the reference. If the address does not match either ACR, then the default value defined in the cache control register (CACR) is used. The specific algorithm is as follows:

```
if (address == ACR0_address including mask)
    Effective Attributes = ACR0 attributes
else if (address == ACR1_address including mask)
    Effective Attributes = ACR1 attributes
else Effective Attributes = CACR default attributes
```

5.3.3 Cache Coherency and Invalidation

The cache does not monitor data references for accesses to cached instructions. Therefore, software must maintain instruction cache coherency by invalidating the appropriate cache entries after modifying code segments if instructions are cached.

The cache invalidation can be performed in several ways. For the instruction- or data-only configurations, setting CACR[CINV] forces the entire cache to be marked as invalid. The invalidation operation requires 512 cycles because the cache sequences through the entire tag array, clearing a single location each cycle. For the split configuration, CACR[INVI] and CACR[INVD] can be used in addition to CACR[CINV] to clear the entire cache, only the instruction half, or only the data half. Any subsequent fetch accesses are postponed until the invalidation sequence is complete.

The privileged CPUSHL instruction can invalidate a single cache line. When this instruction is executed, the cache entry defined by bits [12:4] of the source address register is invalidated, provided CACR[CPDI] is cleared. For the split data/instruction cache configuration, software directly controls bit 12 that selects whether an instruction cache or data cache line is being accessed.

These invalidation operations can be initiated from the ColdFire core or the debug module.

5.3.4 Reset

A hardware reset clears the CACR and disables the cache. The contents of the tag array are not affected by the reset. Accordingly, the system startup code must explicitly perform a cache invalidation by setting CACR[CINV] before the cache can be enabled.

5.3.5 Cache Miss Fetch Algorithm/Line Fills

As discussed in [Section 5.1.2, “Introduction,”](#) the cache hardware includes a 16-byte, line-fill buffer for providing temporary storage for the last fetched line.

With the cache enabled as defined by CACR[CENB], a cacheable fetch that misses in the tag memory and the line-fill buffer generates an external fetch. For data misses, the size of the external fetch is always 16 bytes. For instruction misses, the size of the external fetch is determined by the value contained in the 2-bit CLNF field of the CACR and the miss address. [Table 5-6](#) shows the relationship between the CLNF bits, the miss address, and the size of the external fetch.

Table 5-6. Initial Fetch Offset vs. CLNF Bits

CLNF[1:0]	Longword Address Bits[3:2]			
	00	01	10	11
00	Line	Line	Line	Longword
01	Line	Line	Longword	Longword
1X	Line	Line	Line	Line

Depending on the runtime characteristics of the application and the memory response speed, overall performance may be increased by programming the CLNF bits to values 00 or 01.

For all cases of a line-sized fetch, the critical longword defined by bits [3:2] of the miss address is accessed first followed by the remaining three longwords that are accessed by incrementing the longword address in a modulo-16 fashion as shown below:

```

if miss address[3:2] = 00
    fetch sequence = 0x0, 0x4, 0x8, 0xC
if miss address[3:2] = 01
    fetch sequence = 0x4, 0x8, 0xC, 0x0
if miss address[3:2] = 10
    fetch sequence = 0x8, 0xC, 0x0, 0x4
if miss address[3:2] = 11
    fetch sequence = 0xC, 0x0, 0x4, 0x8

```

After an external fetch has been initiated and the data is loaded into the line-fill buffer, the cache maintains a special most-recently-used indicator that tracks the contents of the associated line-fill buffer versus its corresponding cache location. At the time of the miss, the hardware indicator is set, marking the line-fill buffer as most recently used. If a subsequent access occurs to the cache location defined by bits [12:4] (or bits [11:4] for split configurations of the fill buffer address), the data in the cache memory array is now most recently used, so the hardware indicator is cleared. In all cases, the indicator defines whether the contents of the line-fill buffer or the memory data array are most recently used. At the time of the next cache miss, the contents of the line-fill buffer are written into the memory array if the entire line is present, and the line-fill buffer data is most recently used compared to the memory array.

Generally, longword references are used for sequential instruction fetches. If the processor branches to an odd word address, a word-sized instruction fetch is generated.

For instruction fetches, the fill buffer can also be used as temporary storage for line-sized bursts of non-cacheable references under control of CACR[CEIB]. With this bit set, a non-cacheable instruction fetch is processed, as defined by [Table 5-7](#). For this condition, the line-fill buffer is loaded and subsequent references can hit in the buffer, but the data is never loaded into the memory array.

[Table 5-7](#) shows the relationship between CACR bits CENB and CEIB and the type of instruction fetch.

Table 5-7. Instruction Cache Operation as Defined by CACR

CACR [CENB]	CACR [CEIB]	Type of Instruction Fetch	Description
0	0	N/A	Cache is completely disabled; all instruction fetches are word or longword in size.
0	1	N/A	All instruction fetches are word or longword in size
1	X	Cacheable	Fetch size is defined by Table 5-6 and contents of the line-fill buffer can be written into the memory array
1	0	Non-cacheable	All instruction fetches are word or longword in size, and not loaded into the line-fill buffer
1	1	Non-cacheable	Instruction fetch size is defined by Table 5-6 and loaded into the line-fill buffer, but are never written into the memory array.

Chapter 6

Static RAM (SRAM)

6.1 Introduction

This chapter describes the on-chip static RAM (SRAM) implementation, including general operations, configuration, and initialization. It also provides information and examples showing how to minimize power consumption when using the SRAM.

6.1.1 Overview

The SRAM module provides a general-purpose memory block that the ColdFire processor can access in a single cycle. The location of the memory block can be specified to any 0-modulo-16K address within the 256-Mbyte address space (0x8000_0000 – 0x8FFF_FFFF). The memory is ideal for storing critical code or data structures or for use as the system stack. Because the SRAM module is physically connected to the processor's high-speed local bus, it can service processor-initiated accesses or memory-referencing commands from the debug module.

Depending on configuration information, processor references may be sent to the cache and the SRAM block simultaneously. If the reference maps into the region defined by the SRAM, the SRAM provides the data back to the processor, and the cache data is discarded. Accesses from the SRAM module are not cached.

The SRAM is dual-ported to provide access for any of the bus masters via the SRAM backdoor on the crossbar switch. The SRAM is partitioned into two physical memory arrays to allow simultaneous access to arrays by the processor core and another bus master. For more information on arbitration between multiple masters accessing the SRAM, see [Chapter 11, “System Control Module \(SCM\).”](#)

6.1.2 Features

The major features includes:

- One 16 Kbyte SRAM
- Single-cycle access
- Physically located on the processor's high-speed local bus
- Memory location programmable on any 0-modulo-16 Kbyte address
- Byte, word, and longword address capabilities

6.2 Memory Map/Register Description

The SRAM programming model shown in [Table 6-1](#) includes a description of the SRAM base address register (RAMBAR), SRAM initialization, and power management.

Table 6-1. SRAM Programming Model

Rc[11:0] ¹	Register	Width (bits)	Access	Reset Value	Written w/ MOVEC	Section/Page
Supervisor Access Only Registers						
0xC05	RAM Base Address Register (RAMBAR)	32	R/W	See Section	Yes	6.2.1/6-2

¹ The values listed in this column represent the Rc field used when accessing the core registers via the BDM port. For more information see [Chapter 26, "Debug Module."](#)

6.2.1 SRAM Base Address Register (RAMBAR)

The configuration information in the SRAM base-address register (RAMBAR) controls the operation of the SRAM module.

- The RAMBAR holds the SRAM base address. The MOVEC instruction provides write-only access to this register.
- The RAMBAR can be read or written from the debug module.
- All undefined bits in the register are reserved. These bits are ignored during writes to the RAMBAR and return zeroes when read from the debug module.
- A reset clears the RAMBAR's priority, backdoor write-protect, and valid bits, and sets the backdoor enable bit. This enables the backdoor port and invalidates the processor port to the SRAM (The RAMBAR must be initialized before the core can access the SRAM.) All other bits are unaffected.

NOTE

The only applicable address ranges for the SRAM module's base address are 0x8000_0000 – 0x8FFF_C000. The address must be 0-modulo-16 K. Set the RAMBAR register appropriately.

By default, the RAMBAR is invalid, but the backdoor is enabled. In this state, any core accesses to the SRAM are routed through the backdoor. Therefore, the SRAM is accessible by the core, but it does not have a single-cycle access time. To ensure that the core has single-cycle access to the SRAM, set the RAMBAR[V] bit.

Any access within the memory range allocated for the on-chip SRAM (0x8000_0000-0x8FFF_FFFF) hits in the SRAM even if the address is beyond the defined size for the SRAM. This creates address aliasing for the on-chip SRAM memory. For example, writes to addresses 0x8000_0000 and 0x8000_4000 modify the same memory location. System software should ensure SRAM address pointers do not exceed the SRAM size to prevent unwanted overwriting of SRAM.

The RAMBAR contains several control fields. These fields are shown in [Figure 6-1](#).

Rc[11:0]: 0x0C05 (RAMBAR)

Access: User write-only
Debug read/write

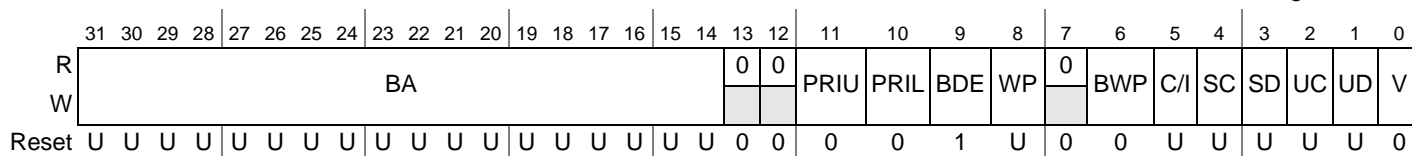


Figure 6-1. SRAM Base Address Register (RAMBAR)

Table 6-2. RAMBAR Field Descriptions

Field	Description															
31–14 BA	Base Address. Defines the 0-modulo-16K base address of the SRAM module. By programming this field, the SRAM may be located on any 16-Kbyte boundary within the processor's 256-Mbyte address space. For proper operation, the base address must be set to between 0x8000_0000 and 0x8FFF_C000.															
13–12	Reserved, must be cleared.															
11–10 PRIU PRIL	<p>Priority Bit. PRIU determines if the SRAM backdoor or CPU has priority in the upper 8K bank of memory. PRIL determines if the SRAM backdoor or CPU has priority in the lower 8K bank of memory. If a bit is set, the CPU has priority. If a bit is cleared, the SRAM backdoor has priority. Priority is determined according to the following table:</p> <table><tr><th>PRIU,PRIL</th><th>Upper Bank Priority</th><th>Lower Bank Priority</th></tr><tr><td>00</td><td>SRAM Backdoor</td><td>SRAM Backdoor</td></tr><tr><td>01</td><td>SRAM Backdoor</td><td>CPU</td></tr><tr><td>10</td><td>CPU</td><td>SRAM Backdoor</td></tr><tr><td>11</td><td>CPU</td><td>CPU</td></tr></table> <p>Note: The recommended setting (maximum performance) for the priority bits is 00.</p>	PRIU,PRIL	Upper Bank Priority	Lower Bank Priority	00	SRAM Backdoor	SRAM Backdoor	01	SRAM Backdoor	CPU	10	CPU	SRAM Backdoor	11	CPU	CPU
PRIU,PRIL	Upper Bank Priority	Lower Bank Priority														
00	SRAM Backdoor	SRAM Backdoor														
01	SRAM Backdoor	CPU														
10	CPU	SRAM Backdoor														
11	CPU	CPU														
9 BDE	<p>Backdoor Enable. Allows access by non-core bus masters via the SRAM backdoor on the crossbar switch</p> <p>0 Non-core crossbar switch master access to memory is disabled.</p> <p>1 Non-core crossbar switch master access to memory is enabled.</p>															
8 WP	<p>Write Protect. Allows only read accesses to the SRAM. When this bit is set, any attempted write access from the core generates an access error exception to the ColdFire processor core.</p> <p>0 Allows core read and write accesses to the SRAM module</p> <p>1 Allows only core read accesses to the SRAM module</p> <p>Note: This bit does not affect non-core write accesses.</p>															
7	Reserved, must be cleared.															
6 BWP	<p>Backdoor Write Protect. Allows only read accesses from the non-core bus masters. When this bit is set, any attempted write access from the non-core bus masters on the backdoor terminates the bus transfer with an access error.</p> <p>0 Allows read and write accesses to the SRAM module from non-core masters.</p> <p>1 Allows only read accesses to the SRAM module from non-core masters.</p>															

Table 6-2. RAMBAR Field Descriptions (continued)

Field	Description
5–1 C/I, SC, SD, UC, UD	<p>Address Space Masks (AS_n). These five bit fields allow types of accesses to be masked or inhibited from accessing the SRAM module. The address space mask bits are:</p> <p>C/I = CPU space/interrupt acknowledge cycle mask SC = Supervisor code address space mask SD = Supervisor data address space mask UC = User code address space mask UD = User data address space mask</p> <p>For each address space bit:</p> <p>0 An access to the SRAM module can occur for this address space 1 Disable this address space from the SRAM module. If a reference using this address space is made, it is inhibited from accessing the SRAM module and is processed like any other non-SRAM reference.</p> <p>These bits do not affect accesses by non-core bus masters using the SRAM backdoor port in any manner. These bits are useful for power management as detailed in Section 6.3.2, “Power Management.” In most applications, the C/I bit is set</p>
0 V	<p>Valid. When set, this bit enables the SRAM module; otherwise, the module is disabled. A hardware reset clears this bit.</p> <p>0 Processor accesses of the SRAM are masked 1 Processor accesses of the SRAM are enabled</p>

6.3 Initialization/Application Information

After a hardware reset, the SRAM module contents are undefined. The valid bit of the RAMBAR is cleared, disabling the processor port into the memory. RAMBAR[BDE] is set, enabling the system backdoor port into the memory. If the SRAM requires initialization with instructions or data, perform the following steps:

1. Load the RAMBAR, mapping the SRAM module to the desired location within the address space.
2. Read the source data and write it to the SRAM. Various instructions support this function, including memory-to-memory move instructions, or the MOVEM opcode. The MOVEM instruction is optimized to generate line-sized burst fetches on 0-modulo-16 addresses, so this opcode generally provides maximum performance.
3. After the data loads into the SRAM, it may be appropriate to load a revised value into the RAMBAR with a new set of attributes. These attributes consist of the write-protect and address space mask fields.

The ColdFire processor or an external debugger using the debug module can perform these initialization functions.

6.3.1 SRAM Initialization Code

The following code segment describes how to initialize the SRAM. The code sets the base address of the SRAM at 0x8000_0000 and initializes the SRAM to zeros.

```
RAMBASE      EQU 0x00000000      ;set this variable to 0x00000000
RAMVALID     EQU 0x00000001
```

```

move.l  #RAMBASE+RAMVALID,D0      ;load RAMBASE + valid bit into D0.
movec.l D0, RAMBAR                ;load RAMBAR and enable SRAM

```

The following loop initializes the entire SRAM to zero:

```

lea.l   RAMBASE,A0                ;load pointer to SRAM
move.l  #4096,D0                  ;load loop counter into D0 (SRAM size/4)

```

SRAM_INIT_LOOP:

```

clr.l   (A0)+                      ;clear 4 bytes of SRAM
clr.l   (A0)+                      ;clear 4 bytes of SRAM
clr.l   (A0)+                      ;clear 4 bytes of SRAM
clr.l   (A0)+                      ;clear 4 bytes of SRAM
subq.l  #4,D0                      ;decrement loop counter
bne.b   SRAM_INIT_LOOP             ;if done, then exit; else continue looping

```

6.3.2 Power Management

As noted previously, depending on the RAMBAR-defined configuration, instruction fetch and operand read accesses may be sent to the SRAM and cache simultaneously. If the access maps to the SRAM module, it sources the read data and the cache access is discarded. If the SRAM is used only for data operands, setting the ASn bits associated with instruction fetches can decrease power dissipation. Additionally, if the SRAM contains only instructions, masking operand accesses can reduce power dissipation. [Table 6-3](#) shows examples of typical RAMBAR settings.

Table 6-3. Typical RAMBAR Setting Examples

Data Contained in SRAM	RAMBAR[7:0]
Instruction Only	0x2B
Data Only	0x35
Instructions and Data	0x21

Chapter 7

Clock Module

7.1 Introduction

The clock module allows the device to be configured for one of several clocking methods. Clocking modes include internal phase-locked loop (PLL) clocking with an external clock reference or an external crystal reference supported by an internal crystal amplifier. The PLL can also be disabled and an external oscillator can be used to clock the device directly. The clock module contains:

- Crystal amplifier and oscillator (OSC)
- Dithering phase-locked loop (PLL)
- Status and control registers
- Control logic

NOTE

Throughout this manual, f_{sys} refers to the core frequency and $f_{\text{sys}/2}$ refers to the internal bus frequency.

Figure 7-1 is a high level representation of the clock connections. The exact functionality of the blocks is not illustrated (e.g. clocks to the SDRAMC are disabled when the device is in limp mode, and the clocks to individual modules may be disabled via the peripheral power management registers).

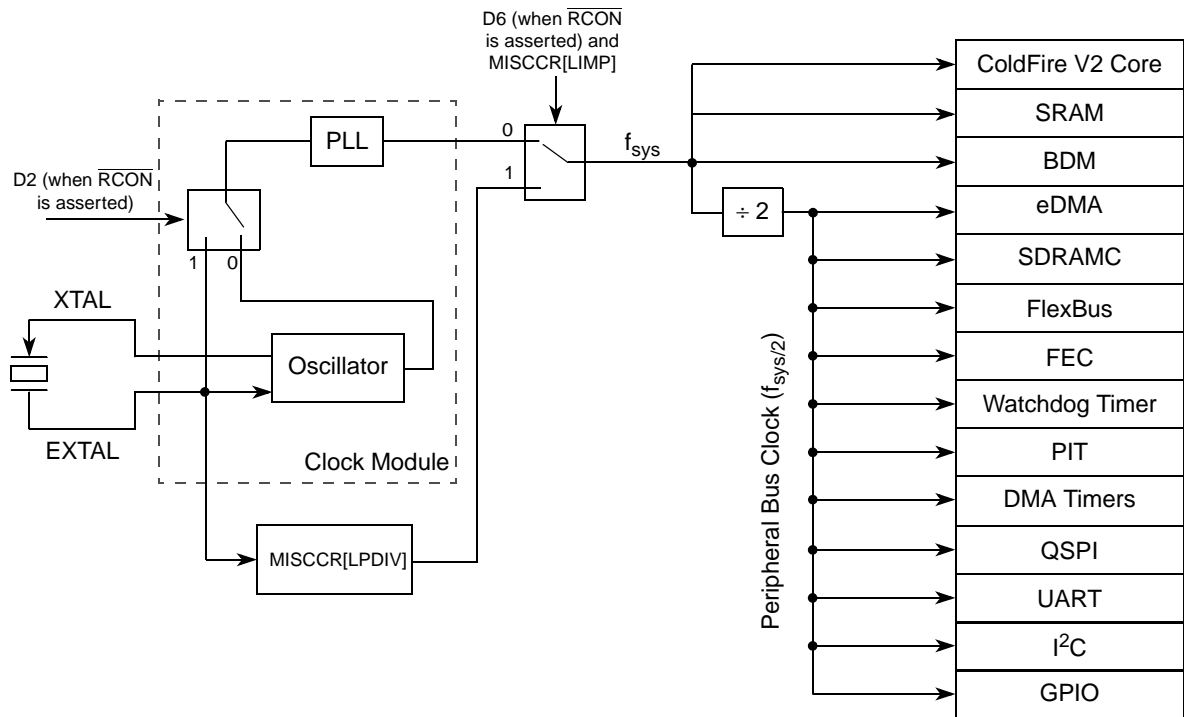


Figure 7-1. Device Clock Connections

7.1.1 Block Diagram

Figure 7-2 shows a block diagram of the clock module.

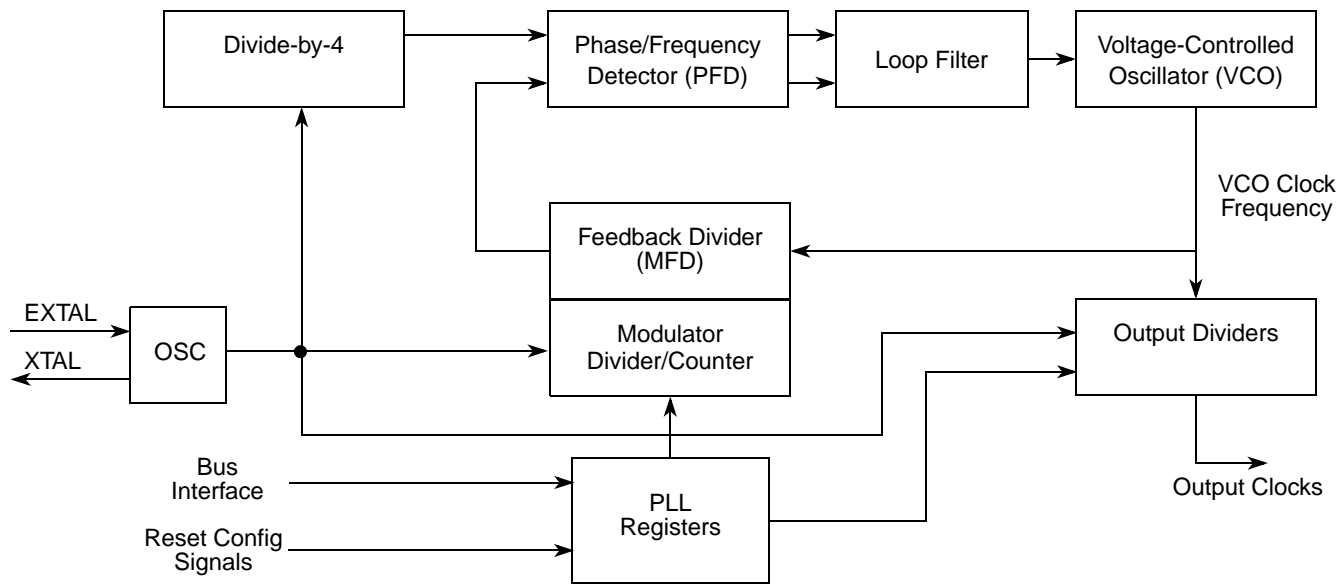


Figure 7-2. Clock Module Diagram

7.1.2 Features

Features of the clock module include the following:

- 16-MHz reference crystal oscillator
- Voltage controlled oscillator range from 350 MHz to 540 MHz, resulting in a core frequency ($f_{vco} \div 3$ (or $f_{vco} \div 4$)) of 87.5 MHz to 166.67 MHz (maximum rated for device)
- Programmable dithering
- Support for low-power modes
- Direct clocking of system by input clock, bypassing the PLL
- Loss-of-lock reset

7.1.3 Modes of Operation

The PLL operational mode must be configured during reset. The reset configuration pins must be driven to the appropriate state for the desired mode from the time RSTOUT asserts until it negates. Refer to [Chapter 9, “Chip Configuration Module \(CCM\).”](#)

The clock module can operate in normal PLL mode with crystal reference, normal PLL mode with external reference, and input clock limp mode.

7.1.3.1 Normal PLL Mode with Crystal Reference

In normal mode with a crystal reference, the PLL receives an input clock frequency from the crystal oscillator circuit and multiplies the frequency to create the PLL output clock. It can synthesize frequencies ranging from 22x to 33.75x the input frequency. The user must supply a crystal oscillator that is within the appropriate input frequency range, the crystal manufacturer’s recommended external support circuitry, and short signal route from the device to the crystal. In normal mode, the PLL can generate a dithered clock or a non-dithered clock (locked on a single frequency). The dithering deviation, dither modulation frequency, and whether the PLL is modulating or not can be programmed by writing to the PLL registers through the bus interface.

7.1.3.2 Normal PLL Mode with External Reference

Same as [Section 7.1.3.1, “Normal PLL Mode with Crystal Reference”](#) except EXTAL is driven by an external clock generator rather than a crystal oscillator. However, the input frequency range is the same as the crystal reference. To enter normal mode with external clock generator reference, the PLL configuration must be set at reset by overriding the default reset configuration. See [Chapter 9, “Chip Configuration Module \(CCM\),”](#) for details on setting the device for external reference.

7.1.3.3 Input Clock (Limp) Mode

Through the use of RCON, the device may be booted into a low-frequency limp mode, in which the PLL is bypassed and the device runs from a factor of the input clock (EXTAL). In this mode, EXTAL feeds a 5-bit programmable counter that divides the input clock by 2^n , where n is the value of the programmable counter field, MISCCR[LPDIV]. For more information on programming the divider, see [Chapter 8,](#)

“Power Management.” The programmed value of the divider may be changed without glitches or otherwise negative affects to the system.

While in this mode, the PLL is placed in bypass mode to reduce overall system power consumption. A 2:1 ratio is maintained between the core and the primary bus clock. Because they do not function at speeds as low as the minimum input clock frequency, the SDRAM controller and FEC are not functional in limp mode.

When switching from LIMP mode to normal functional mode, you must ensure that any peripheral transactions in progress (e.g. Ethernet frame reception/transmission) are allowed to complete to avoid data loss or corruption.

Limp mode may also be entered and exited from by writing to the MISCCR[LIMP] bit. This is useful because it places the PLL in a state where the multiplication factor (PFMDR) can be altered. Entering limp mode also requires a special procedure with the SDRAM module. As noted above the SDRAM controller is disabled in limp mode, so two critical steps must be followed before setting the MISCCR[LIMP] bit.

1. Code execution must be transferred to another memory resource. Primary options are whatever memory device is attached to the FlexBus boot chip select or on-chip SRAM (but not the CPU cache, as it may have to be flushed upon limp mode entrance or exit).
2. The SDRAM controller must be placed in self-refresh mode to avoid data loss while the SDRAMC is shut down.

7.1.3.4 Low-power Mode Operation

This subsection describes the operation of the clock module in low-power and halted modes of operation. Low-power modes are described in [Chapter 8, “Power Management.”](#) [Table 7-1](#) shows the clock module operation in low-power modes.

Table 7-1. Clock Module Operation in Low-power Modes

Low-power Mode	Clock Operation	Mode Exit
Wait	Clocks sent to peripheral modules only	Exit not caused by clock module, but normal clocking resumes upon mode exit
Doze	Clocks sent to peripheral modules only	Exit not caused by clock module, but normal clocking resumes upon mode exit
Stop	All system clocks disabled	Exit not caused by clock module, but clock sources are re-enabled and normal clocking resumes upon mode exit
Halted	Normal	Exit not caused by clock module

In wait and doze modes, the system clocks to the peripherals are enabled, and the clocks to the core, and SRAM are stopped. Each module can disable its clock locally at the module level.

In stop mode, all system clocks are disabled. There are several options for enabling or disabling the PLL or crystal oscillator in stop mode, compromising between stop mode current and wakeup recovery time. The PLL can be disabled in stop mode, but requires a wakeup period before it can relock. The oscillator can also be disabled during stop mode, but requires a wakeup period to restart.

When the PLL is enabled in stop mode (LPCR[STPMD] = 00), the external FB_CLK signal can support systems using FB_CLK as the clock source. See [Section 8.2.5, “Low-Power Control Register \(LPCR\),”](#) for more information about operating the PLL in stop mode.

There is also a fast wakeup option for quickly enabling the system clocks during stop recovery (LPCR[FWKUP]). This eliminates the wakeup recovery time but at the risk of sending a potentially unstable clock to the system.

7.2 Memory Map/Register Definition

The PLL module programming model consists of the following registers:

Table 7-2. PLL Memory Map

Address	Register	Width (bits)	Access	Reset Value	Section/Page
0xFC09_0000	PLL Output Divider Register (PODR)	8	R/W	0x36 ¹	7.2.1/7-5
0xFC09_0002	PLL Control Register (PCR)	8	R/W	0x00	7.2.2/7-6
0xFC09_0004	PLL Modulation Divider Register (PMDR)	8	R/W	0x00	7.2.3/7-7
0xFC09_0006	PLL Feedback Divider Register (PFDR)	8	R/W	0x42 ¹	7.2.4/7-8

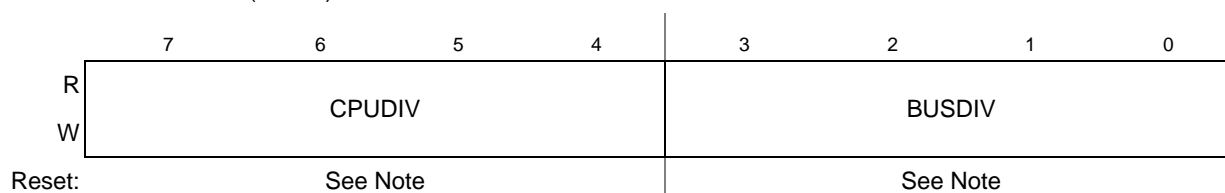
¹ With default reset configuration (\overline{RCON} is negated).

7.2.1 PLL Output Divider Register (PODR)

The PODR register controls the output divider for generating the core and bus clocks. The value of this register may be 0x48 or 0x36 and writing any other value to this register results in unpredictable behavior.

Address: 0xFC09_0000 (PODR)

Access: User read/write



Note: Default value determined by reset configuration. See [Chapter 9, “Chip Configuration Module \(CCM\),”](#) for more information. For the default reset configuration (\overline{RCON} negated), the reset value is 0x48. If \overline{RCON} and D1 is asserted at reset, the reset value of PODR is 0x36.

Figure 7-3. PLL Output Divider Register (PODR)

Table 7-3. PODR Field Descriptions

Field	Description																		
7–4 CPUDIV	Divider for generating the core frequency. See BUSDIV for a table of possible values.																		
3–0 BUSDIV	Divider for generating the internal bus frequency. <table><tr><th>Value</th><th>Core Clock</th><th>Bus Clock</th></tr><tr><td>0011</td><td>VCO/3</td><td>Reserved</td></tr><tr><td>0100</td><td>VCO/4</td><td>Reserved</td></tr><tr><td>0110</td><td>Reserved</td><td>VCO/6</td></tr><tr><td>1000</td><td>Reserved</td><td>VCO/8</td></tr><tr><td>Else</td><td>Reserved</td><td>Reserved</td></tr></table>	Value	Core Clock	Bus Clock	0011	VCO/3	Reserved	0100	VCO/4	Reserved	0110	Reserved	VCO/6	1000	Reserved	VCO/8	Else	Reserved	Reserved
Value	Core Clock	Bus Clock																	
0011	VCO/3	Reserved																	
0100	VCO/4	Reserved																	
0110	Reserved	VCO/6																	
1000	Reserved	VCO/8																	
Else	Reserved	Reserved																	

7.2.2 PLL Control Register (PCR)

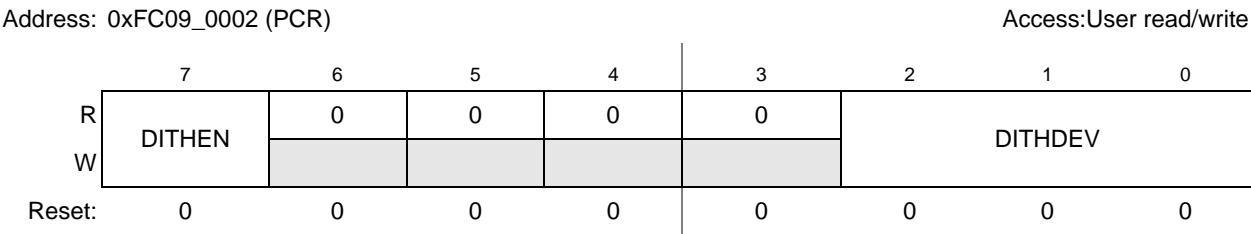


Figure 7-4. PLL Control Register (PCR)

Table 7-4. PCR Field Descriptions

Field	Description
7 DITHEN	Dithering enable bit. 0 Dithering disabled. 1 Dithering enabled.

Table 7-4. PCR Field Descriptions (continued)

Field	Description																		
6–3	Reserved, should be cleared.																		
2–0 DITHDEV	<p>Dither Deviation. The dither deviation settings are target percentages based on simulation. The actual percentages observed are slightly larger than these targets. See Section 7.3.2, “Dithering Waveform Definition” for more information.</p> <p>Deviation = -0.75% - (DITHDEV × 0.75%)</p> <table border="1"> <thead> <tr> <th>DITHDEV</th><th>Deviation</th></tr> </thead> <tbody> <tr><td>000</td><td>- 0.75%</td></tr> <tr><td>001</td><td>- 1.00%</td></tr> <tr><td>010</td><td>- 1.25%</td></tr> <tr><td>011</td><td>- 1.50%</td></tr> <tr><td>100</td><td>- 1.75%</td></tr> <tr><td>101</td><td>- 2.00%</td></tr> <tr><td>110</td><td>- 2.25%</td></tr> <tr><td>111</td><td>- 2.50%</td></tr> </tbody> </table> <p>Note: This field should only be written when dithering mode is disabled (PCR[DITHEN] = 0). Else, unpredictable PLL operation results.</p>	DITHDEV	Deviation	000	- 0.75%	001	- 1.00%	010	- 1.25%	011	- 1.50%	100	- 1.75%	101	- 2.00%	110	- 2.25%	111	- 2.50%
DITHDEV	Deviation																		
000	- 0.75%																		
001	- 1.00%																		
010	- 1.25%																		
011	- 1.50%																		
100	- 1.75%																		
101	- 2.00%																		
110	- 2.25%																		
111	- 2.50%																		

7.2.3 PLL Modulation Divider Register (PMDR)

Address: 0xFC09_0004 (PMDR)

Access: User read/write

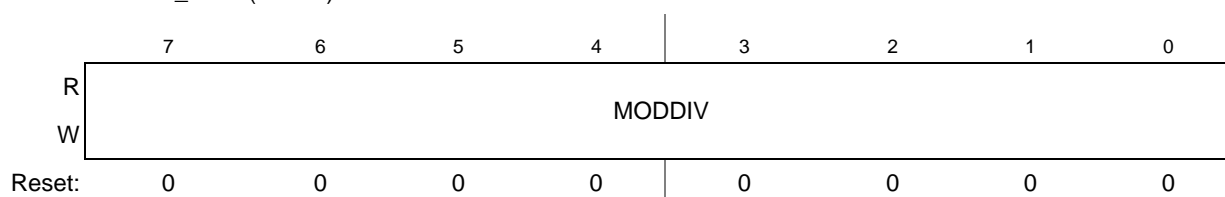
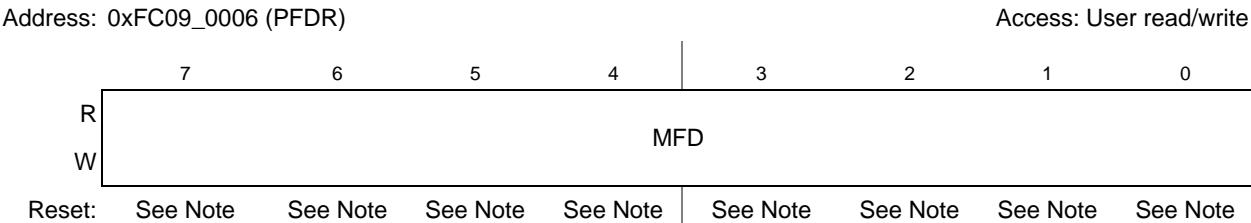


Figure 7-5. PLL Modulation Divider Register (PMDR)

Table 7-5. PMDR Field Descriptions

Field	Description
7–0 MODDIV	<p>Dither modulation divider.</p> <p>Dither Modulation Frequency = Input Frequency / (MODDIV × 32)</p> <p>A dither modulation frequency greater than 105 kHz or less than 9.95 kHz is invalid. For example, for a 16 MHz input frequency, MODDIV may be programmed between 5 (100 kHz) and 50 (10 kHz). Programming MODDIV outside the specified range results in unpredictable PLL operation.</p> <p>Note: This field should only be written when dithering mode is disabled (PCR[DITHEN] = 0). Else, unpredictable PLL operation results.</p>

7.2.4 PLL Feedback Divider Register (PFDR)



Note: Reset value determined by reset configuration. See [Chapter 9, “Chip Configuration Module \(CCM\),”](#) for more information. For the default reset configuration (\overline{RCON} negated), the reset value is 0x58. If \overline{RCON} and D1 is asserted at reset, the reset value of PFDR is 0x7D.

Figure 7-6. PLL Feedback Divider Register (PFDR)

Table 7-6. PFDR Field Descriptions

Field	Description
7–0 MFD	<p>The MFD bits control the value of the divider in the PLL feedback loop. The value specified by the MFD bits establish the multiplication factor applied to the reference frequency. See Section 7.3.3, “PLL Frequency Multiplication Factor Select” for more details.</p> <p>0x58 88 0x59 89 0x5A 90 ... 0x86 134 0x87 135 Else Reserved</p> <p>Note: The MFD bits may only be written when the device is in limp mode (MISCCR[LIMP] = 1).</p>

7.3 Functional Description

This subsection provides a functional description of the clock module.

7.3.1 PLL Dithered and Non-Dithered Operation

The PLL is capable of generating output clocks with a frequency that modulates in a triangular waveform with a specified percentage frequency deviation and a specified dither modulation frequency. This modulation of the output clock is called dithered operation. When the PLL operates at a fixed frequency, this operation is known as non-dithered operation. The selection of dithered or non-dithered operation is controlled by the PCR[DITHEN] bit. The percent frequency deviation and dither modulation frequency are also controlled by the PCR and PMDR registers, whose operation is described in [Section 7.3.2, “Dithering Waveform Definition.”](#)

After reset, dithering is disabled. After the PLL has locked (indicated by the MISCCR[PLLLOCK] bit described in [Section 8.2.6, “Miscellaneous Control Register \(MISCCR\)”](#)), the PLL may be changed from non-dithered operation to dithered operation by writing to the PCR. After the PCR[DITHEN] bit has been set, the PLL synchronizes the new value with the VCO clock domain. Then the transition from non-dithered operation to dithered operation takes place such that the PLL output clocks remain glitch-free. However, the dithering waveform and deviation percentages are not guaranteed to meet

specifications until two modulation periods have passed after the time of the write to the PCR register. During the transition the frequency of the PLL output clocks does not exceed 10% of the respective non-dithered frequency.

The PLL may also be changed from dithered operation to non-dithered operation by clearing the PCR[DITHEN] bit. After this occurs, the PLL synchronizes the new value with the VCO clock domain. Then, the transition from dithered operation to non-dithered operation takes place such that PLL output clocks remain glitch-free. However, the frequency of the PLL output clocks are not guaranteed to be completely stable until one modulation period has passed after the time of the write to the PCR. During the transition the frequency of the PLL output clocks does not exceed 10% of the respective non-dithered frequency.

Because the transition between dithered and non-dithered operation (and vice-versa) takes a period of time to change, the PCR may not be written back-to-back without waiting two modulation periods between writes.

NOTE

Failure to wait two modulation periods between writes to the PCR results in unpredictable PLL operation.

7.3.2 Dithering Waveform Definition

The dithering waveform created by the changes in the frequency of the PLL output clocks is defined by the percent frequency deviation and dither modulation frequency. The definitions of the percent frequency deviation (or dithering deviation) and the modulation period (which is the inverse of the dither modulation frequency) are shown in Figure 7-7. The dithering deviation is controlled by PCR[DITHDEV] field, while the dither modulation frequency is controlled by the PMDR[MODDIV] field.

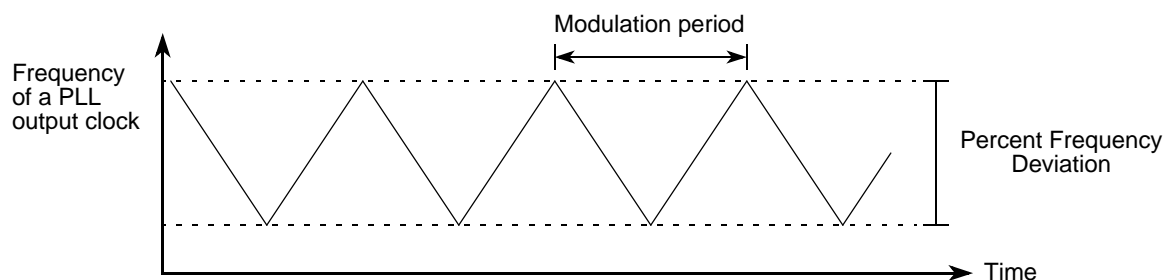


Figure 7-7. Ideal Triangular Dithering Waveform

After reset, the PCR and PMDR registers are cleared, disabling dithering. After reset has been de-asserted and the PLL has locked (indicated by the MISCCR[PLLLOCK] bit), the dithering waveform definition may be changed by writing to the PCR[DITHDEV] field and the PMDR register. However, the PCR[DITHDEV] field and PMDR register may only be written to when the PLL is in non-dithered operation (i.e. the PCR[DITHEN] bit must be cleared).

NOTE

Writing to the PCR[DITHDEV] field or the PMDR during dithering operation results in unpredictable PLL operation.

The dither deviation can be programmed to be between -0.75% of the non-dithered frequency up to -2.50% of the non-dithered frequency in steps of 0.25%.

NOTE

The dither deviation settings in the PCR[DITHDEV] field are target percentages based on simulation. The actual percentages achieved may be numerically different than the percentages listed in the specification; however, the actual percentages achieved are in proportion to each other and are stable within $\pm 10\%$ across process, voltage, and temperature conditions.

The dither modulation frequency can be programmed to be between approximately 10kHz and 100kHz. Because the dither modulation frequency is determined as a division of the input frequency, the dither modulation frequency is given by the following equation:

$$\text{Dither Modulation Frequency} = \frac{\text{Input Frequency}}{\text{PMDR}[\text{MODDIV}] \times 32} \quad \text{Eqn. 7-1}$$

NOTE

PMDR[MODDIV] field values that result in a dither modulation frequency greater than 105kHz or less than 9.95kHz are invalid and result in unpredictable PLL operation.

7.3.3 PLL Frequency Multiplication Factor Select

The frequency multiplication factor of the PLL is defined by the feedback divider in the following equation:

$$f_{\text{sys}} = f_{\text{ref}} \times \left(\frac{\text{PFDR}}{4 \times \text{PODR}[\text{CPUDIV}]} \right) \quad \text{Eqn. 7-2}$$

where f_{sys} is the core frequency. The allowable range of values for the PFDR is 88 to 135, resulting in a frequency multiplication factor range of 7.33 to 11.25 times the input reference frequency (typically 16 MHz).

The PFDR can only be modified while the device is in limp mode, which is entered by setting the MISCCR[LIMP] bit. After the PFDR register has been changed, re-enter normal mode by clearing the MISCCR[LIMP] bit. The PLL then begins to acquire lock accordingly on the new frequency.

7.3.4 System Clock Modes

The system clock source is determined during reset. By default the PLL is placed in crystal reference mode and generates a core/bus frequency of 88/44 MHz. This default mode can be overridden by asserting the RCON pin. See [Chapter 9, “Chip Configuration Module \(CCM\),”](#) for more information on overriding the default configuration during reset.

[Table 7-7](#) shows the clock-out frequency to clock-in frequency relationships for the possible system clock modes. Refer to [Section 7.1.3, “Modes of Operation”](#) for details on each mode.

Table 7-7. Clock Out and Clock In Relationships

System Clock Mode	PLL Options ¹	Cross-Reference
Normal PLL clock mode	$\overline{\text{RCON}}$ negated (default): $f_{\text{sys}} = f_{\text{ref}} \times \left(\frac{\text{PFDR}}{16} \right)$ $\overline{\text{RCON}}$ and D1 asserted: $f_{\text{sys}} = f_{\text{ref}} \times \left(\frac{\text{PFDR}}{12} \right)$	Section 7.1.3.1, “Normal PLL Mode with Crystal Reference” and Section 7.1.3.2, “Normal PLL Mode with External Reference”
Limp mode	$f_{\text{sys}} = \frac{f_{\text{ref}}}{2^{\text{MISCCR}[\text{LPDIV}]}}$	Section 7.1.3.3, “Input Clock (Limp) Mode”

¹ f_{ref} = input reference frequency = 16 MHz
 PFDR ranges from 88 to 135
 MISCCR[LPDIV] ranges from 0 to 15

7.3.5 Clock Operation During Reset

This section describes the reset operation of the PLL. Power-on reset and normal reset are described.

7.3.5.1 Power-On Reset (POR)

After V_{DDPLL} and the input clock are within specification, the PLL is held in reset for at least 10 input clock cycles to initialize the PLL. The reset configuration signals are used to select the multiply factor of the PLL and the reset state of the PLL registers. While in reset, the PLL input clock is output to the device. After $\overline{\text{RESET}}$ is de-asserted, PLL output clocks are generated; however, until the MISCCR[PLLLOCK] bit is set the PLL output clock frequencies are not stable and not within specification. The MISCCR[PLLLOCK] bit is set after $\overline{\text{RESET}}$ has negated for a minimum of 1 ms. When this bit is set, the PLL is in frequency lock.

7.3.5.2 External Reset

When $\overline{\text{RESET}}$ is asserted, the PLL input clock is output to the device and the PLL does not begin acquiring lock until $\overline{\text{RESET}}$ is negated. The MISCCR[PLLLOCK] bit is cleared and remains cleared while the PLL is acquiring lock. This bit is set after the PLL lock period of 1 ms has passed.

CAUTION

When running in an unlocked state, the clocks generated by the PLL are not guaranteed to be stable and may exceed the maximum specified frequency of the device.

Chapter 8

Power Management

8.1 Introduction

This chapter explains the low-power operation of the device.

8.1.1 Features

The following features support low-power operation:

- Four modes of operation: run, wait, doze, and stop
- Ability to shut down most peripherals independently
- Ability to shut down clocks to most peripherals independently
- Ability to run the device in low-frequency limp mode
- Ability to shut down the external FB_CLK pin

8.2 Memory Map/Register Definition

The power management programming model consists of registers from the SCM and CCM memory space, as shown below:

Table 8-1. Power Management Memory Map

Address	Register	Width (bits)	Access	Reset Value	Section/Page
Supervisor Access Only Registers¹					
0xFC04_0013	Wakeup Control Register (WCR)	8	R/W	0x00	8.2.1/8-2
0xFC04_002C	Peripheral Power Management Set Register 0 (PPMSR0)	8	W	0x00	8.2.2/8-3
0xFC04_002D	Peripheral Power Management Clear Register 0 (PPMCR0)	8	W	0x00	8.2.3/8-4
0xFC04_0030	Peripheral Power Management High Register 0 (PPMHR0)	32	R/W	0x0000_0000	8.2.4/8-4
0xFC04_0034	Peripheral Power Management Low Register 0 (PPMLR0)	32	R/W	0x0000_0000	8.2.4/8-4
0xFC0A_0007	Low-Power Control Register (LPCR)	8	R/W	0x00	8.2.5/8-6
0xFC0A_0010	Miscellaneous Control Register (MISCCR)	16	R/W	See Section	8.2.6/8-7

¹ User access to supervisor only address locations have no effect and result in a bus error

8.2.1 Wake-up Control Register

Implementation of low-power stop mode and exit from a low-power mode via an interrupt require communication between the core and logic associated with the interrupt controller. The WCR enables entry into low-power modes, and includes the setting of the interrupt level needed to exit a low-power mode.

NOTE

The setting of the low-power mode select field, LPCR[LPMD], determines which low-power mode the device enters when a STOP instruction is issued.

The following sequence of operations is generally needed to enable this functionality:

1. The WCR register is programmed, setting the ENBWCR bit and the desired interrupt priority level.
2. At the appropriate time, the processor executes the privileged STOP instruction. After the processor has stopped execution, it asserts a specific processor status (PST) encoding. Issuing the STOP instruction when the WCR[ENBWCR] bit is set causes the SCM to enter the mode specified in LPCR[LPMD].
3. The entry into a low-power mode is processed by the low-power mode control logic, and the appropriate clocks (usually those related to the high-speed processor core) are disabled.
4. After entering the low-power mode, the interrupt controller enables a combinational logic path which evaluates any unmasked interrupt requests. The device waits for an event to generate an interrupt request with a priority level greater than the value programmed in WCR[PRILVL].
5. After an appropriately high interrupt request level arrives, the interrupt controller signals its presence, and the SCM responds by asserting the request to exit low-power mode.
6. The low-power mode control logic senses the request signal and re-enables the appropriate clocks.
7. With the processor clocks enabled, the core processes the pending interrupt request.

Address: 0xFC04_0013 (WCR)

Access: Supervisor read/write

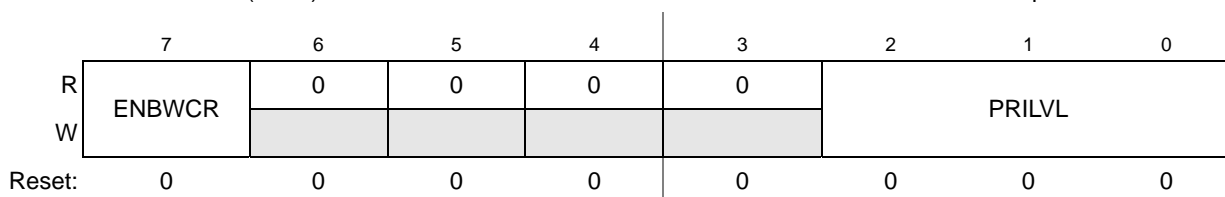


Figure 8-1. Wake-up Control Register (WCR)

Table 8-2. WCR Field Descriptions

Field	Description
7 ENBWCR	Enable low-power mode entry. The mode entered is specified in LPCR[LPMD]. 0 Low-power mode entry is disabled 1 Low-power mode entry is enabled.

Table 8-2. WCR Field Descriptions (continued)

Field	Description																
6–3	Reserved, should be cleared.																
2–0 PRILVL	Exit low-power mode interrupt priority level. This field defines the interrupt priority level needed to exit the low-power mode. <table border="1"> <thead> <tr> <th>PRILVL</th><th>Interrupt Level Needed to Exit Low-Power Mode</th></tr> </thead> <tbody> <tr> <td>000</td><td>Any interrupt request exits low-power mode</td></tr> <tr> <td>001</td><td>Interrupt request levels [2-7] exit low-power mode</td></tr> <tr> <td>010</td><td>Interrupt request levels [3-7] exit low-power mode</td></tr> <tr> <td>011</td><td>Interrupt request levels [4-7] exit low-power mode</td></tr> <tr> <td>100</td><td>Interrupt request levels [5-7] exit low-power mode</td></tr> <tr> <td>101</td><td>Interrupt request levels [6-7] exit low-power mode</td></tr> <tr> <td>11x</td><td>Interrupt request level [7] exits low-power mode</td></tr> </tbody> </table>	PRILVL	Interrupt Level Needed to Exit Low-Power Mode	000	Any interrupt request exits low-power mode	001	Interrupt request levels [2-7] exit low-power mode	010	Interrupt request levels [3-7] exit low-power mode	011	Interrupt request levels [4-7] exit low-power mode	100	Interrupt request levels [5-7] exit low-power mode	101	Interrupt request levels [6-7] exit low-power mode	11x	Interrupt request level [7] exits low-power mode
PRILVL	Interrupt Level Needed to Exit Low-Power Mode																
000	Any interrupt request exits low-power mode																
001	Interrupt request levels [2-7] exit low-power mode																
010	Interrupt request levels [3-7] exit low-power mode																
011	Interrupt request levels [4-7] exit low-power mode																
100	Interrupt request levels [5-7] exit low-power mode																
101	Interrupt request levels [6-7] exit low-power mode																
11x	Interrupt request level [7] exits low-power mode																

8.2.2 Peripheral Power Management Set Register (PPMSR0)

The PPMSR register provides a simple mechanism to set a given bit in the PPM{H,L}R registers to disable the clock for a given peripheral module without the need to perform a read-modify write on the PPMR. The data value on a register write causes the corresponding bit in the PPM{H,L}R to be set. The SAMCD bit provides a global set function forcing the entire contents of the PPMR to be set, disabling all peripheral module clocks. Reads of these registers return all zeroes.

Address: 0xFC04_002C (PPMSR0)

Access: Supervisor Write-only

	7	6	5	4	3	2	1	0
R	0	0	0	0	0	0	0	0
W		SAMCD	SMCD					
Reset:	0	0	0	0	0	0	0	0

Figure 8-2. Peripheral Power Management Set Register (PPMSR0)

Table 8-3. PPMSR0 Field Descriptions

Field	Description
7	Reserved, should be cleared.
6 SAMCD	Set all module clock disables. 0 Set only those bits specified in the SMCD field 1 Set all bits in PPMRH and PPMRL, disabling all peripheral clocks
5–0 SMCD	Set module clock disable. Set the corresponding bit in PPM{H,L}R, disabling the peripheral clock.

8.2.3 Peripheral Power Management Clear Register (PPMCR)

The PPMCR register provides a simple mechanism to clear a given bit in the PPMHR & PPMLR registers, enabling the clock for a given peripheral module without the need to perform a read-modify write on the PPMR. The data value on a register write causes the corresponding bit in the PPM{H,L}R to be clear. A value of 64 to 127 (setting the CAMCD bit) provides a global clear function forcing the entire contents of the PPMR to be clear, enabling all peripheral module clocks. Reads of these registers return all zeroes.

Address: 0xFC04_002D (PPMCR0)

Access: Supervisor Write-only

	7	6	5	4	3	2	1	0
R	0	0	0	0	0	0	0	0
W		CAMCD	CMCD					
Reset:	0	0	0	0	0	0	0	0

Figure 8-3. Peripheral Power Management Clear Register (PPMCR0)

Table 8-4. PPMCR0 Field Descriptions

Field	Description
7	Reserved, should be cleared.
6 CAMCD	Clear all module clock disables. 0 Clear only those bits specified in the CMCD field 1 Clear all bits in PPMRH and PPMLR, enabling all peripheral clocks
5–0 CMCD	Clear module clock disable. Clear the corresponding bit in PPMR{H,L}, enabling the peripheral clock.

8.2.4 Peripheral Power Management Registers (PPMHR0 & PPMLR0)

The PPMR registers provide a bit map for controlling the generation of the peripheral clocks for each decoded address space. Recall each peripheral module is mapped into 16 kByte slots within the memory map. The PPMR registers provide a unique control bit for each of these address spaces that defines whether the module clock for the given space is enabled or disabled.

Because the operation of the crossbar switch and the system control module (SCM) are fundamental to the operation of the device, the clocks for these modules cannot be disabled.

The individual bits of the PPMR can be modified using a read-modify-write to this register directly or indirectly through writes to the PPMSR and PPMCR registers to set/clear individual bits.

Address: 0xFC04_0030 (PPMHR0)

Access: Supervisor read/write

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
R	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
W																
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	0	0	0	0	0	CD42	CD41	CD40	0	0	0	CD36	CD35	CD34	CD33	CD32
W																
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Figure 8-4. Peripheral Power Management High Register (PPMHR0)

Table 8-5. PPMHR0[CDn] Assignments

Slot Number	CDn	Peripheral
32	CD32	PIT 0
33	CD33	PIT 1
34	CD34	Edge Port
35	CD35	On-chip Watchdog Timer
36	CD36	PLL
40	CD40	CCM, Reset Controller, Power Management
41	CD41	GPIO Module
42	CD42	SDRAM Controller

Address: 0xFC04_0034 (PPMLR0)

Access: Supervisor read/write

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
R					0							0	0			0
W	CD31	CD30	CD29	CD28		CD26	CD25	CD24	CD23	CD22	CD21			CD18	CD17	
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	0	0	0		0	0	0	0	0	0	0	0	0		0	0
W				CD12										CD2		
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Figure 8-5. Peripheral Power Management Low Registers (PPMLR0)

Table 8-6. PPMLR0[CDn] Assignments

Slot Number	CDn	Peripheral
2	CD2	FlexBus
12	CD12	FEC
17	CD17	eDMA Controller

Table 8-6. PPMLR0[CDn] Assignments (continued)

Slot Number	CDn	Peripheral
18	CD18	Interrupt Controller
21	CD21	IACK
22	CD22	I ² C
23	CD23	QSPI
24	CD24	UART0
25	CD25	UART1
26	CD26	UART2
28	CD28	DMA Timer 0
29	CD29	DMA Timer 1
30	CD30	DMA Timer 2
31	CD31	DMA Timer 3

Table 8-7. PPMHR & PPMLR Field Descriptions

Field	Description
CDn	Module slot <i>n</i> clock disable. 0 The clock for this module is enabled. 1 The clock for this module is disabled.

CAUTION

Extreme caution should be taken by the customer when setting PPMR[CD40] to disable clocking of the CCM, reset controller, and power management modules. This may disable logic to reset the chip, disable the external bus monitor, and other logic contained within these blocks.

8.2.5 Low-Power Control Register (LPCR)

The LPCR register controls chip operation and module operation during low-power modes.

Address: 0xFC0A_0007 (LPCR)

Access: Supervisor read/write

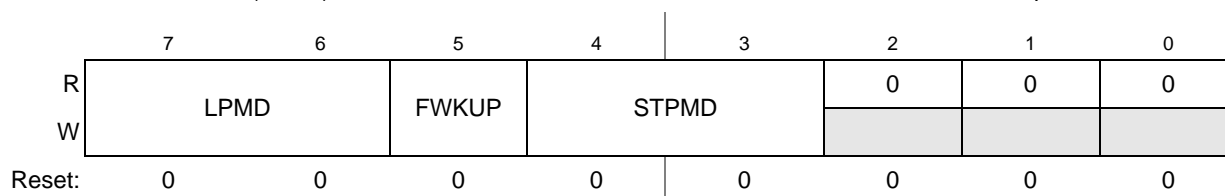


Figure 8-6. Low-Power Control Register (LPCR)

Table 8-8. LPCR Field Descriptions

Field	Description																									
7–6 LPMD	Low-power mode select. Used to select the low-power mode the chip enters after the ColdFire core executes the STOP instruction. These bits must be written prior to instruction execution for them to take effect. The LPMD bits are readable and writable in all modes. 00 Run 01 Doze 10 Wait 11 Stop Note: If LPCR[LPMD] is cleared, the device stops executing code upon issue of a STOP instruction. However, no clocks are disabled.																									
5 FWKUP	Fast wake-up. Determines whether the system clocks are enabled upon wake-up from stop mode. This bit must be written before execution of the STOP instruction for it to take effect. 0 System clocks enabled only when PLL is locked or operating normally. 1 System clocks enabled upon wake-up from stop mode, regardless of PLL lock status. Note: Setting this bit is potentially dangerous and unreliable. The system may behave unpredictably when using an unlocked clock because the clock frequency could overshoot the maximum frequency of the device. Note: If FWKUP is set before entering stop mode, it should not be cleared upon wake-up from stop mode until after the PLL has actually acquired lock. Lock status may be obtained by reading the MISCCR[PLLLOCK] bit. FWKUP is not effective in limp mode because the PLL never locks in this mode. The system clocks are always enabled upon wake-up from stop mode, regardless of the value of FWKUP.																									
4–3 STPMD	FB_CLK stop mode bits. Controls the operation of the clocks, PLL, and oscillator in stop mode as shown below. <table><tr><th>STPMD</th><th>System Clocks</th><th>FB_CLK</th><th>PLL</th><th>Oscillator</th></tr><tr><td>00</td><td>Disabled</td><td>Enabled</td><td>Enabled</td><td>Enabled</td></tr><tr><td>01</td><td>Disabled</td><td>Disabled</td><td>Enabled</td><td>Enabled</td></tr><tr><td>10</td><td>Disabled</td><td>Disabled</td><td>Disabled</td><td>Enabled</td></tr><tr><td>11</td><td>Disabled</td><td>Disabled</td><td>Disabled</td><td>Disabled</td></tr></table>	STPMD	System Clocks	FB_CLK	PLL	Oscillator	00	Disabled	Enabled	Enabled	Enabled	01	Disabled	Disabled	Enabled	Enabled	10	Disabled	Disabled	Disabled	Enabled	11	Disabled	Disabled	Disabled	Disabled
STPMD	System Clocks	FB_CLK	PLL	Oscillator																						
00	Disabled	Enabled	Enabled	Enabled																						
01	Disabled	Disabled	Enabled	Enabled																						
10	Disabled	Disabled	Disabled	Enabled																						
11	Disabled	Disabled	Disabled	Disabled																						
2–0	Reserved, should be cleared.																									

8.2.6 Miscellaneous Control Register (MISCCR)

The MISCCR provides clock source selection and configuration for internal clocks.

Address: 0xFC0A_0010 (MISCCR)

Access: Supervisor read/write

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	0	0	PLL LOCK	LIMP	0	0	0	0	0	0	0	0	LPDIV			
W																
Reset	0	0	1	See Note	0	0	0	0	0	0	0	0	0	0	0	0

Note: Reset value depends upon chosen reset configuration (RCON[RLIMP]).

Figure 8-7. Miscellaneous Control Register (MISCCR)

Table 8-9. MISCCR Field Descriptions

Field	Description
15–14	Reserved, should be cleared.
13 PLLLOCK	PLL lock status. 0 PLL is not locked. 1 PLL is locked.
12 LIMP	Limp mode enable. Selects between the PLL and the low-power clock divider as the source of all system clocks. 0 Normal operation; PLL drives all internal clocks. 1 Limp mode; low-power clock divider drivers internal clocks.
11–4	Reserved, should be cleared.
3–0 LPDIV	Low power divider. Specifies the limp mode divide value used to produce the clock for the ColdFire core, bus, and other system clocks. A 2:1 ratio is maintained between the core and the internal bus. This field is used only when LIMP is set, and ignored otherwise. Limp mode clock = Oscillator clock / 2^{LPDIV} Note: When LPDIV is 0 (divide-by-1), the internal bus clock and FB_CLK will not have a 50/50 duty cycle.

8.3 Functional Description

The functions and characteristics of the low-power modes, and how each module is affected by, or affects these modes are discussed in this section.

8.3.1 Peripheral Shut Down

All peripherals, except for the SCM and crossbar switch, may have their input clocks individually removed by software to reduce power consumption. See [Section 8.2.4, “Peripheral Power Management Registers \(PPMHR0 & PPMLR0\)”](#) for more information. A peripheral may be disabled at any time and remains disabled during any low-power mode of operation.

8.3.2 Limp mode

The device may also be booted into a low-frequency limp mode, in which the PLL is bypassed and the device runs from a factor of the input clock (EXTAL). In this mode, EXTAL feeds a 5-bit programmable counter that divides the input clock by 2^n , where n is the value of the programmable counter field, MISCCR[LPDIV]. The programmed value of the divider may be changed without glitches or otherwise negative affects to the system. While in this mode, the PLL is placed in bypass mode to reduce overall system power consumption.

Limp mode may also be entered and exited from by writing to the MISCCR[LIMP] bit.

While in this mode a 2:1 ratio is maintained between the core and the primary bus clock. Because they do not function at speeds as low as the minimum input clock frequency, the SDRAM controller, and FEC are not functional in limp mode.

8.3.3 Low-Power Modes

The system enters a low-power mode by executing a STOP instruction. The low-power mode the device actually enters (stop, wait, or doze) depends on the setting of LPCR[LPMD]. Entry into any of these modes idles the CPU with no cycles active, powers down the system, and stops all internal clocks appropriately. During stop mode, the system clock is stopped low.

A wake-up event is required to exit a low-power mode and return to run mode. Wake-up events consist of any of these conditions:

- Any type of reset
- Any valid, enabled interrupt request

Exiting from low power mode via an interrupt request requires:

- An interrupt request whose priority is higher than the value programmed in the WCR[PRILVL].
- An interrupt request whose priority is higher than the value programmed in the interrupt priority mask (I) field of the core's status register.
- An interrupt request from a source which is not masked in the interrupt controller's interrupt mask register.
- An interrupt request which has been enabled at the module of the interrupt's origin.

8.3.3.1 Run Mode

Run mode is the normal system operating mode. Current consumption in this mode is related directly to the system clock frequency.

8.3.3.2 Wait Mode

Wait mode is intended to be used to stop only the CPU and memory clocks until a wake-up event is detected. In this mode, peripherals may be programmed to continue operating and can generate interrupts, which cause the CPU to exit from wait mode.

8.3.3.3 Doze Mode

Doze mode affects the CPU in the same manner as wait mode, except that some peripherals define individual operational characteristics in doze mode. Peripherals which continue to run and have the capability of producing interrupts may cause the CPU to exit the doze mode and return to run mode. Peripherals that are stopped restart operation on exit from doze mode as defined for each peripheral.

8.3.3.4 Stop Mode

Stop mode affects the CPU in the same manner as the wait and doze modes, except that all clocks to the system are stopped and the peripherals cease operation.

Stop mode must be entered in a controlled manner to ensure that any current operation is properly terminated. When exiting stop mode, most peripherals retain their pre-stop status and resume operation.

The following subsections specify the operation of each module while in and when exiting low-power modes.

NOTE

Entering stop mode disables the SDRAMC including the refresh counter. If SDRAM is used, then code is required to ensure proper entry and exit from stop mode. See [Chapter 18, “SDRAM Controller \(SDRAMC\),”](#) for more information.

8.3.4 Peripheral Behavior in Low-Power Modes

8.3.4.1 ColdFire Core

The ColdFire core is disabled during any low-power mode. No recovery time is required when exiting any low-power mode.

8.3.4.2 Internal SRAM

The SRAM is disabled during any low-power mode. No recovery time is required when exiting any low-power mode.

8.3.4.3 Clock Module

In wait and doze modes, the clocks to the CPU and SRAM is stopped and the system clocks to the peripherals are enabled. Each module may disable the module clocks locally at the module level or the module clocks may be individually disabled by the PPMR registers (refer to [Section 8.2.4, “Peripheral Power Management Registers \(PPMHR0 & PPMLR0\)”](#)). In stop mode, all clocks to the system are stopped.

There are several options for enabling or disabling the PLL or crystal oscillator in stop mode, compromising between stop mode current and wakeup recovery time. The PLL can be disabled in stop mode, but requires a wakeup period before it can relock. The oscillator can also be disabled during stop mode, but requires a wakeup period to restart.

When the PLL is enabled in stop mode ($LPCR[STPMD] = 00$), the external FB_CLK signal can support systems using FB_CLK as the clock source. See [Section 8.2.5, “Low-Power Control Register \(LPCR\),”](#) for more information about operating the PLL in stop mode.

There is also a fast wakeup option for quickly enabling the system clocks during stop recovery ($LPCR[FWKUP]$). This eliminates the wakeup recovery time but at the risk of sending a potentially unstable clock to the system. This is also explained in [Section 8.2.5, “Low-Power Control Register \(LPCR\).”](#)

8.3.4.4 Chip Configuration Module

The chip configuration module is unaffected by entry into a low-power mode. If low-power mode is exited by a reset, chip configuration may be executed if configured to do so.

8.3.4.5 Reset Controller

A power-on reset (POR) always causes a chip reset and exit from any low-power mode.

In wait and doze modes, asserting the external $\overline{\text{RESET}}$ pin for at least four clocks causes an external reset that resets the chip and exit any low-power modes.

In stop mode, the $\overline{\text{RESET}}$ pin synchronization is disabled and asserting the external $\overline{\text{RESET}}$ pin asynchronously generates an internal reset and exit any low-power modes. Registers lose current values and must be reconfigured from reset state if needed.

If the core or on-chip watchdog timer remains enabled during wait or doze modes, then a watchdog timer timeout may generate a reset to exit these low-power modes.

When the CPU is inactive, a software reset cannot be generated to exit any low-power mode.

8.3.4.6 System Control Module (SCM)

The SCM's core watchdog timer can bring the device out of all low-power modes except stop mode. In stop mode, all clocks stop, and the core watchdog timer does not operate.

When enabled, the core watchdog can bring the device out of low-power mode in one of two ways. Depending on the setting of the CWCW[CWRI] field, a core watchdog timeout may cause a reset of the device. Other settings of the CWRI field may enable a core watchdog interrupt and upon a watchdog timeout, this interrupt can bring the device out of low-power mode. This system setup must meet the conditions specified in [Section 8.3.3, “Low-Power Modes”](#) for the core watchdog interrupt to bring the part out of low-power mode.

8.3.4.7 Cross-Bar Switch

8.3.4.8 GPIO Ports

The GPIO ports are unaffected by entry into a low-power mode. These pins may impact low-power current draw if they are configured as outputs and are sourcing current to an external load. If low-power mode is exited by a reset, the state of the I/O pins reverts to their default direction settings.

8.3.4.9 Interrupt Controllers (INTC0)

The interrupt controller is not affected by any of the low-power modes. All logic between the input sources and generating the interrupt to the processor is combinational to allow the ability to wake up the core during low-power stop mode when all system clocks are stopped.

An interrupt request causes the CPU to exit a low-power mode only if that interrupt's priority level is at or above the level programmed in the interrupt priority mask field of the CPU's status register (SR) and above the level programmed in the WCR[PRILVL]. The interrupt must also be enabled in the interrupt controller's interrupt mask register as well as at the module from which the interrupt request would originate.

8.3.4.10 Edge Port

In wait and doze modes, the edge port continues to operate normally and may be configured to generate interrupts (an edge transition or low level on an external pin) to exit the low-power modes.

In stop mode, there is no system clock available to perform the edge detect function. Thus, only the level detect logic is active (if configured) to allow any low level on the external interrupt pin to generate an interrupt (if enabled) to exit stop mode.

8.3.4.11 eDMA Controller

In wait and doze modes, the eDMA controller is capable of bringing the device out of a low-power mode by generating an interrupt upon completion of a transfer or an error condition. The completion of transfer interrupt is generated when DMA interrupts are enabled by the setting of a `EDMA_INTR[INTn]` bit, and an interrupt is generated when the `TCDn[DONE]` bit is set. The interrupt upon error condition is generated when the `EDMA_EEIR[EEIn]` bit is set, and an interrupt is generated when any of the `EDMA_ESR` bits becomes set.

The eDMA controller is stopped in stop mode and thus cannot cause an exit from this low-power mode.

8.3.4.12 FlexBus Module

In wait and doze modes, the FlexBus module continues operation but does not generate interrupts; therefore it cannot bring a device out of a low-power mode. This module is stopped in stop mode.

8.3.4.13 SDRAM Controller (SDRAMC)

SDRAM controller operation is unaffected by the wait or doze modes; however, the SDRAMC is disabled by stop mode. Because all clocks to the SDRAMC are disabled by stop mode, the SDRAMC does not generate refresh cycles.

To prevent loss of data the SDRAMC should be placed in self-refresh mode by clearing `SDCR[CKE]` and setting `SDCR[REF_EN]`. The SDRAM self-refresh mode allows the SDRAM to enter a low-power state where internal refresh operations are used to maintain the integrity of the data stored in the SDRAM.

When stop mode is exited, setting the `SDCR[CKE]` bit causes the SDRAM controller to exit the self-refresh mode and allow bus cycles to the SDRAM to resume.

NOTE

The SDRAM is inaccessible while in the self-refresh mode. Therefore, if stop mode is used the vector table and any interrupt handlers that could wake the processor should not be stored in or attempt to access SDRAM.

8.3.4.14 Fast Ethernet Controller (FEC)

In wait and doze modes, the FEC is unaffected and may generate an interrupt to exit these low-power modes. In stop mode, the FEC stops immediately and freezes operation, register values, state machines, and external pins. During this mode, the FEC clocks are shut down. Coming out of stop mode returns the FEC to operation from the state prior to stop mode entry.

8.3.4.15 On-chip Watchdog Timer

In stop mode (or in wait/doze mode, if so programmed in the WCR register), the watchdog ceases operation and freezes at the current value. When exiting these modes, the watchdog resumes operation from the stopped value. It is the responsibility of software to avoid erroneous operation.

When not stopped, the watchdog may generate a reset to exit the low-power modes.

8.3.4.16 Programmable Interrupt Timers (PIT0–3)

In stop mode (or in doze mode, if so programmed in the PCSR_{*n*} register), the programmable interrupt timer (PIT) ceases operation, and freezes at the current value. When exiting these modes, the PIT resumes operation from the stopped value. It is the responsibility of software to avoid erroneous operation.

When not stopped, the PIT may generate an interrupt to exit the low-power modes.

8.3.4.17 DMA Timers (DTIM0–3)

In wait and doze modes, the DMA timers may generate an interrupt to exit a low-power mode. This interrupt can be generated when the DMA timer is in input capture mode or reference compare mode.

In input capture mode, where the capture enable (CE) field of the timer mode register (DTMR) has a non-zero value and the DTXMR[DMAEN] is cleared, an interrupt is issued upon a captured input. In reference compare mode, where the output reference request interrupt enable (ORRI) bit of DTMR is set and the DTXMR[DMAEN] bit is cleared, an interrupt is issued when the timer counter reaches the reference value.

DMA timer operation is disabled in stop mode. Upon exiting stop mode, the timer resumes operation unless stop mode was exited by reset.

8.3.4.18 Queued Serial Peripheral Interface (QSPI)

In wait and doze modes, the QSPI module is unaffected and may generate an interrupt to exit these low-power modes.

In stop mode, the QSPI stops immediately and freezes operation, register values, state machines, and external pins. During this mode, the QSPI clocks are shut down. Coming out of stop mode returns the QSPI to operation from the state prior to stop mode entry.

8.3.4.19 UART Modules (UART0–2)

In wait and doze modes, the UARTs are unaffected and may generate an interrupt to exit these low-power modes.

In stop mode, the UARTs stop immediately and freeze their operation, register values, state machines, and external pins. During this mode, the UART clocks are shut down. Coming out of stop mode returns the UARTs to operation from the state prior to stop mode entry.

8.3.4.20 I²C Module

When the I²C Module is enabled by the setting of the I2CR[IEN] bit and when the device is not in stop mode, the I²C module is operable and may generate an interrupt to bring the device out of a low-power mode. For an interrupt to occur, the I2CR[IIE] bit must be set to enable interrupts, and the setting of the I2SR[IIF] generates the interrupt signal to the CPU and interrupt controller. The setting of I2SR[IIF] signifies the completion of one byte transfer or the reception of a calling address matching its own specified address when in slave receive mode.

In stop mode, the I²C module stops immediately and freezes operation, register values, and external pins. Upon exiting stop mode, the I²C resumes operation unless stop mode was exited by reset.

8.3.4.21 BDM

Entering halt (debug) mode via the BDM port (by asserting the external $\overline{\text{BKPT}}$ pin) causes the CPU to exit any low-power mode.

8.3.4.22 JTAG

The JTAG (Joint Test Action Group) controller logic is clocked using the TCLK input and is not affected by the system clock. The JTAG cannot generate an event to cause the CPU to exit any low-power mode. Toggling TCLK during any low-power mode increases the system current consumption.

8.3.5 Summary of Peripheral State During Low-power Modes

The functionality of each of the peripherals and CPU during the various low-power modes is summarized in [Table 8-10](#). The status of each peripheral during a given mode refers to the condition the peripheral automatically assumes when the STOP instruction is executed and the LPCR[LPMD] field is set for the particular low-power mode. Individual peripherals may be disabled by programming its dedicated control bits. The wake-up capability field refers to the ability of an interrupt or reset by that peripheral to force the CPU into run mode.

Table 8-10. CPU and Peripherals in Low-Power Modes

Module	Peripheral Status ¹ / Wake-up Procedure					
	Wait Mode		Doze Mode		Stop Mode	
ColdFire Core	Stopped	N/A	Stopped	N/A	Stopped	N/A
SRAM	Stopped	N/A	Stopped	N/A	Stopped	N/A
Clock Module	Enabled	Interrupt	Enabled	Interrupt	Program	Interrupt
Power Management	Enabled	N/A	Enabled	N/A	Stopped	N/A
Chip Configuration Module	Enabled	N/A	Enabled	N/A	Stopped	N/A
Reset Controller	Enabled	Reset	Enabled	Reset	Enabled	Reset
System Control Module	Enabled	Reset	Enabled	Reset	Stopped	N/A
GPIO Module	Enabled	N/A	Enabled	N/A	Enabled	N/A

Table 8-10. CPU and Peripherals in Low-Power Modes (continued)

Module	Peripheral Status ¹ / Wake-up Procedure					
	Wait Mode		Doze Mode		Stop Mode	
Interrupt controller	Enabled	Interrupt	Enabled	Interrupt	Enabled	Interrupt
Edge port	Enabled	Interrupt	Enabled	Interrupt	Stopped	Interrupt
eDMA Controller	Enabled	Yes	Enabled	Yes	Stopped	N/A
FlexBus Module	Enabled	N/A	Enabled	N/A	Stopped	N/A
SDRAM Controller	Enabled	N/A	Enabled	N/A	Stopped	N/A
Fast Ethernet Controller	Enabled	Interrupt	Enabled	Interrupt	Stopped	N/A
On-chip Watchdog Timer	Program	Reset	Program	Reset	Stopped	N/A
Programmable Interrupt Timers	Enabled	Interrupt	Program	Interrupt	Stopped	N/A
DMA Timers	Enabled	Interrupt	Enabled	Interrupt	Stopped	N/A
QSPI	Enabled	Interrupt	Enabled	Interrupt	Stopped	N/A
UARTs	Enabled	Interrupt	Enabled	Interrupt	Stopped	N/A
I ² C Module	Enabled	Interrupt	Enabled	Interrupt	Stopped	N/A
JTAG	Enabled	N/A	Enabled	N/A	Enabled	N/A
BDM ²	Enabled	Yes	Enabled	Yes	Enabled	Yes

¹ Program indicates that the peripheral function during the low-power mode is dependent on programmable bits in the peripheral register map.

² The BDM logic is clocked by a separate TCLK clock. Entering halt mode via the BDM port exits any lower-power mode. Upon exit from halt mode, the previous low-power mode is re-entered and changes made in halt mode remain in effect.

Chapter 9

Chip Configuration Module (CCM)

9.1 Introduction

The chip configuration module (CCM) controls the chip configuration for the device.

9.1.1 Block Diagram

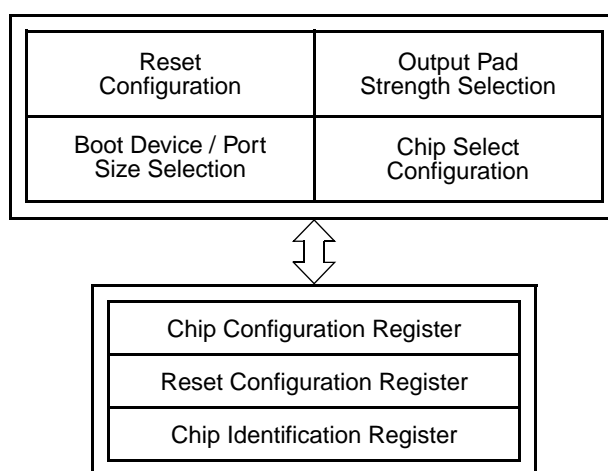


Figure 9-1. Chip Configuration Module Block Diagram

9.1.2 Features

The CCM performs the following operations:

- Selects the chip operating mode
- Selects external clock or phase-lock loop (PLL) mode with internal or external reference
- Selects output pad drive strength
- Selects boot device and data port size
- Selects bus monitor configuration
- Selects low-power configuration

9.1.3 Modes of Operation

The only chip operating mode available on this device is master mode. In master mode, the ColdFire core can access external memories and peripherals. The external bus consists of a 32-bit data bus and 24 address

lines. The available bus control signals include $\overline{R/W}$, \overline{TS} , \overline{TA} , \overline{OE} , and $\overline{BE/BWE}[3:0]$. Up to six chip selects can be programmed to select and control external devices and to provide bus cycle termination.

9.2 External Signal Descriptions

Table 9-1 provides an overview of the CCM signals.

Table 9-1. Signal Properties

Name	Function	Reset State
\overline{RCON}	Reset configuration select	Internal weak pull-up device
D[9,7:1]	Reset configuration override pins	—

9.2.1 \overline{RCON}

If the external \overline{RCON} pin is asserted during reset, then various chip functions, including the reset configuration pin functions after reset, are configured according to the levels driven onto the external data pins (see Section 9.4, “Functional Description”). The internal configuration signals are driven to reflect the levels on the external configuration pins to allow for module configuration.

9.2.2 D[9,7:1] (Reset Configuration Override)

If the external \overline{RCON} pin is asserted during reset, then the states of these data pins during reset determine the chip mode of operation, boot device, clock mode, and certain module configurations after reset.

NOTE

It is recommended that the logic levels for reset configuration on D[9,7:1] be actively driven when \overline{RCON} is used. The rest of the data bus should be allowed to float or be pulled high.

9.3 Memory Map/Register Definition

The CCM programming model consists of the registers listed in the below table.

Table 9-2. CCM Memory Map

Address	Register	Width (bits)	Access	Reset Value	Section/Page
Supervisor Access Only Registers¹					
0xFC0A_0004	Chip Configuration Register (CCR)	16	R	See Section	9.3.1/9-3
0xFC0A_0008	Reset Configuration Register (RCON)	16	R	0x0201	9.3.2/9-4
0xFC0A_000A	Chip Identification Register (CIR)	16	R	See Section	9.3.3/9-4

¹ User access to supervisor only address locations have no effect and result in a bus error.

9.3.1 Chip Configuration Register (CCR)

The CCR is a read-only register; writing to the CCR has no effect. At reset, the CCR reflects the chosen operation of certain chip functions. These functions may be set to the defaults defined by the RCON register values or may be overridden during reset configuration using the external RCON and D[15:0] pins. (See [Figure 9-3](#) for the RCON register definition.)

Address: 0xFC0A_0004 (CCR)

Access: Supervisor read-only

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	0	0	0	0	0	0	CSC	1	OSC FREQ	LIMP	LOAD	BOOTPS	OSC MODE	PLL MODE		1
W																
Reset	0	0	0	0	0	0					See Note					1

Note: Reset value depends upon chosen reset configuration. Default reset value ($\overline{\text{RCON}}$ is not asserted) is 0x012B.

Figure 9-2. Chip Configuration Register (CCR)

Table 9-3. CCR Field Descriptions

Field	Description
15–10	Reserved, should be cleared.
9 CSC	Chip select configuration field. Reflects the chosen chip select configuration. 0 A[23:22] = A[23:22] 1 A[23] = $\overline{\text{FB_CS5}}$ and A[22] = $\overline{\text{FB_CS4}}$
8	Reserved, should be set.
7 OSCFREQ	Oscillator frequency select bit. Reflects the chosen PLL multiplier for the device. However, this bit is valid only if PLLMODE is set (D1 is asserted during RCON). 0 PLL's PFDR[MFD] is set to 125, if PLLMODE is set. 1 PLL's PFDR[MFD] is set to 120, if PLLMODE is set.
6 LIMP	Limp mode bit. 0 Normal operation; PLL drives internal clocks. 1 Limp mode; low-power clock divider drives internal clocks.
5 LOAD	Pad driver load bit. Reflects the chosen pad driver strength for those pins with drive strength control and the chosen pad slew rate for those pins with slew rate control. 0 Low drive strength, low slew rate 1 High drive strength, high slew rate
4–3 BOOTPS	Boot port size field. Indicates the selection for the boot port size. 00 32 bits 01 16 bits 10 8 bits 11 32 bits
2 OSCMODE	Oscillator clock mode bit. 0 Crystal oscillator mode 1 Oscillator bypass mode
1 PLLMODE	PLL clock mode 0 88/44 MHz operation 1 166.67/83.33 MHz operation
0	Reserved, should be set.

9.3.2 Reset Configuration Register (RCON)

At reset, RCON determines the default operation of certain chip functions. All default functions defined by the RCON values can only be overridden during reset configuration (see [Section 9.4.1, “Reset Configuration”](#)) if the external $\overline{\text{RCON}}$ pin is asserted. RCON is a read-only register and contains the same fields as the CCR register. See [Table 9-3](#) for field descriptions.

Address: 0xFC0A_0008 (RCON) Access: Supervisor read-only

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	0	0	0	0	0	0	CSC	1	OSC FREQ	LIMP	LOAD	BOOTPS	OSC MODE	PLL MODE		1
W																
Reset	0	0	0	0	0	0	0	1	0	0	1	0	1	0	1	1

Figure 9-3. Reset Configuration Register (RCON)

9.3.3 Chip Identification Register (CIR)

Address: 0xFC0A_000A (CIR) Access: Supervisor read-only

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	PIN										PRN					
W																
Reset	Device Dependent										Mask Set Dependent					

Figure 9-4. Chip Identification Register (CIR)

Table 9-4. CIR Field Description

Field	Description
15–6 PIN	Part identification number. Contains a unique identification number for the device. 0x044 MCF5208 0x045 MCF5207
5–0 PRN	Part revision number. This number is increased by one for each new full-layer mask set of this part. The revision numbers are assigned in chronological order.

9.4 Functional Description

Six functions are defined within the chip configuration module:

1. Reset configuration
2. PLL mode
3. Oscillator mode
4. Boot device selection
5. Output pad strength configuration
6. Chip select configuration

These functions are described below.

9.4.1 Reset Configuration

During reset, the pins for the reset override functions are immediately configured to known states. [Table 9-5](#) shows the states of the external pins while in reset.

Table 9-5. Reset Configuration Pin States During Reset

Pin	Pin Function ¹	I/O	Output State	Input State
D[15:0]	Primary function	Input	—	Must be driven by external logic
$\overline{\text{RCON}}$	$\overline{\text{RCON}}$ function for all modes ²	Input	—	Internal weak pull-up device

¹ If the external $\overline{\text{RCON}}$ pin is not asserted during reset, pin functions are determined by the default operation mode defined in the RCON register. If the external $\overline{\text{RCON}}$ pin is asserted, pin functions are determined by the override values driven on the external data bus pins.

² During reset, the external $\overline{\text{RCON}}$ pin assumes its $\overline{\text{RCON}}$ pin function, but this pin changes to the function defined by the chip operation mode immediately after reset. See [Table 9-6](#).

If the $\overline{\text{RCON}}$ pin is not asserted during reset, the chip configuration and the reset configuration pin functions after reset are determined by the RCON register or fixed defaults, regardless of the states of the external data pins. The internal configuration signals are driven to levels specified by the RCON register's reset state for default module configuration.

If the $\overline{\text{RCON}}$ pin is asserted during reset, then various chip functions, including the reset configuration pin functions after reset, are configured according to the levels driven onto the external data pins. (See [Table 9-6](#).) The internal configuration signals are driven to reflect the levels on the external configuration pins to allow for module configuration.

NOTE

It is recommended that the logic levels for reset configuration on D[9,7:1] be actively driven when $\overline{\text{RCON}}$ is used. The rest of the data bus should be allowed to float or be pulled high.

Table 9-6. Configuration During Reset¹

Pin(s) Affected	Default Configuration	Override Pins in Reset ²	Function
None	RCON[1] = 1	D1	PLL Mode
		0	88/44 MHz operation
		1	166.67/83.33 MHz operation (default)

Table 9-6. Configuration During Reset¹ (continued)

Pin(s) Affected	Default Configuration	Override Pins in Reset ²	Function
None	RCON[2] = 0	D2	Oscillator Mode
		0	Crystal oscillator mode (default)
		1	Oscillator bypass mode
None	RCON[4:3] = 01	D[4:3]	Boot Device
		00	External with 32-bit port ³
		01	External with 16-bit port (default)
		10	External with 8-bit port
		11	External with 32-bit port
All output pins	RCON[5] = 1	D5	Output pad drive strength
		0	Low Drive Strength
		1	High Drive Strength (default)
None	RCON[6] = 0	D6	Limp Mode
		0	PLL mode (default)
		1	Limp mode
None	RCON[7] = 0	D7	PLL Multiplier Select⁴
		0	120 (default)
		1	125
A[23:22]/FB_CS[5:4]	RCON[9] = 0	D9	Chip Select Configuration
		0	A[23:22] = A[23:22]
		1	A[23:22] = FB_CS[5:4] (default)

¹ Modifying the default configurations is possible only if the external $\overline{\text{RCON}}$ pin is asserted.

² The external reset override circuitry drives the data bus pins with the override values while $\overline{\text{RSTOUT}}$ is asserted. It must stop driving the data bus pins within one FB_CLK cycle after $\overline{\text{RSTOUT}}$ is negated. To prevent contention with the external reset override circuitry, the reset override pins are forced to inputs during reset and do not become outputs until at least one FB_CLK cycle after $\overline{\text{RSTOUT}}$ is negated.

³ 32-bit port size is not available when DRAMSEL = 0. Defaults to 16-bit mode instead.

⁴ Valid only if D1 is set.

9.4.2 PLL Mode Selection

The initial device operating frequency is determined during reset configuration by the D1 pin. The default configuration with a 16 MHz input clock is 88 MHz for the core and 44 MHz for the internal bus. The user may choose to almost double these frequencies (166.67 MHz and 83.33 MHz) by placing the device in limp mode and reconfiguring the appropriate PLL registers, or asserting D1 during reset configuration.

9.4.3 Oscillator Mode Selection

Use of the internal oscillator can be selected during reset configuration via the D2 pin. By default, the oscillator is enabled and the PLL is placed in normal mode with a crystal reference. If default configuration is over-ridden and D2 is asserted, the PLL is placed in normal mode with a external reference and the internal oscillator is bypassed. After reset is exited, the oscillator mode cannot be changed. See [Chapter 7, “Clock Module”](#) for more details on the available modes.

9.4.4 Boot Device Selection

During reset configuration, the $\overline{\text{FB_CS0}}$ chip select pin is configured to select an external boot device. In this case, the V (valid) bit in the CSMR0 register is ignored, and $\overline{\text{FB_CS0}}$ is enabled after reset. $\overline{\text{FB_CS0}}$ is asserted for the initial boot fetch accessed from address 0x0000_0000 for the stack pointer and address 0x0000_0004 for the program counter (PC). It is assumed that the reset vector loaded from address 0x0000_0004 causes the core to start executing from external memory space decoded by $\overline{\text{FB_CS0}}$.

9.4.5 Output Pad Strength Configuration

Output pad strength is determined during reset configuration as shown in [Table 9-7](#). After reset is exited, the output pad strength configuration can only be changed using the GPIO module. For more information see [Chapter 13, “General Purpose I/O Module.”](#)

Table 9-7. Output Pad Driver Strength Selection¹

Optional Pin Function Selection	D5
Output pads configured for low drive strength	D5 driven low
Output pads configured for full drive strength	D5 driven high

¹ Modifying the default configurations is possible only if the external $\overline{\text{RCON}}$ pin is asserted low.

9.4.6 Chip Select Configuration

The chip select configuration ($\overline{\text{FB_CS}}[5:4]$) is selected during reset and reflected in the CCR[CSC] field. After reset is exited, the chip select configuration cannot be changed. [Table 9-6](#) shows the different chip select configurations that can be implemented during reset configuration.

Chapter 10

Reset Controller Module

10.1 Introduction

The reset controller determines the cause of reset, asserts the appropriate reset signals to the system, and keeps a history of what caused the reset.

10.1.1 Block Diagram

Figure 10-1 illustrates the reset controller and is explained in the following sections.

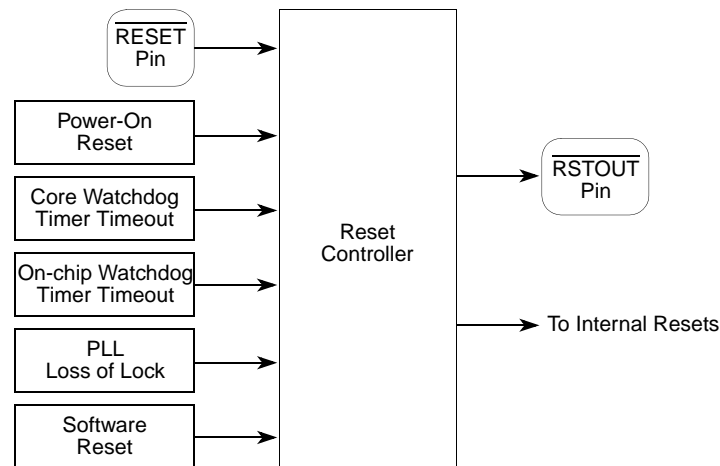


Figure 10-1. Reset Controller Block Diagram

10.1.2 Features

Module features include the following:

- Six sources of reset:
 - External
 - Power-on reset (POR)
 - Core watchdog timer
 - On-chip watchdog timer
 - Phase locked-loop (PLL) loss of lock
 - Software
- Software-assertable $\overline{\text{RSTOUT}}$ pin independent of chip reset state
- Software-readable status flags indicating the cause of the last reset

10.2 External Signal Description

Table 10-1 provides a summary of the reset controller signal properties. The signals are described in the following paragraphs.

Table 10-1. Reset Controller Signal Properties

Name	Direction	Input Hysteresis	Input Synchronization
$\overline{\text{RESET}}$	I	Y	Y ¹
$\overline{\text{RSTOUT}}$	O	—	—

¹ $\overline{\text{RESET}}$ is always synchronized except when in low-power stop mode.

10.2.1 $\overline{\text{RESET}}$

Asserting the external $\overline{\text{RESET}}$ for at least four rising FB_CLK edges causes the external reset request to be recognized and latched.

10.2.2 $\overline{\text{RSTOUT}}$

This active-low output signal is driven low when the internal reset controller module resets the chip. It may take up to six FB_CLK edges after $\overline{\text{RESET}}$ assertion for $\overline{\text{RSTOUT}}$ to assert, due to an internal synchronizer on $\overline{\text{RESET}}$. When $\overline{\text{RSTOUT}}$ is active, the user can drive override options on the data bus. See Chapter 9, “Chip Configuration Module (CCM),” for more details on these override options.

10.3 Memory Map/Register Definition

The reset controller programming model consists of these registers:

- Reset control register (RCR), which selects reset controller functions
- Reset status register (RSR), which reflects the state of the last reset source

See Table 10-2 for the memory map and the following paragraphs for a description of the registers.

Table 10-2. Reset Controller Memory Map

Address	Register	Width (bits)	Access	Reset Value	Section/Page
0xFC0A_0000	Reset Control Register (RCR)	8	R/W	0x00	10.3.1/10-2
0xFC0A_0001	Reset Status Register (RSR)	8	R	See Section	10.3.2/10-3

10.3.1 Reset Control Register (RCR)

The RCR allows software control for requesting a reset, and for independently asserting the external $\overline{\text{RSTOUT}}$ pin.

Address: 0xFC0A_0000 (RCR)

Access: User read/write

	7	6	5	4	3	2	1	0
R	SOFTRST	FRCRSTOUT	0	0	0	0	0	0
W								
Reset:	0	0	0	0	0	0	0	0

Figure 10-2. Reset Control Register (RCR)

Table 10-3. RCR Field Descriptions

Field	Description
7 SOFTRST	Allows software to request a reset. The reset caused by setting this bit clears this bit. 1 Software reset request 0 No software reset request
6 FRCRSTOUT	Allows software to assert or negate the external $\overline{\text{RSTOUT}}$ pin. 1 Assert $\overline{\text{RSTOUT}}$ pin 0 Negate $\overline{\text{RSTOUT}}$ pin CAUTION: External logic driving reset configuration data during reset needs to be considered when asserting the $\overline{\text{RSTOUT}}$ pin when setting FRCRSTOUT.

10.3.2 Reset Status Register (RSR)

The RSR contains a status bit for every reset source. When reset is entered, the cause of the reset condition is latched, along with a value of 0 for the other reset sources that were not pending at the time of the reset condition. These values are then reflected in RSR. One or more status bits may be set at the same time. The cause of any subsequent reset is also recorded in the register, overwriting status from the previous reset condition.

RSR can be read at any time. Writing to RSR has no effect.

Address: 0xFC0A_0001 (RSR)

Access: User read-only

	7	6	5	4	3	2	1	0
R	0	0	SOFT	WDR CHIP	POR	EXT	WDR CORE	LOL
W								
Reset:	0	0	Reset Dependent	Reset Dependent	Reset Dependent	Reset Dependent	Reset Dependent	Reset Dependent

Figure 10-3. Reset Status Register (RSR)

Table 10-4. RSR Field Descriptions

Field	Description
7–6	Reserved, should be cleared.
5 SOFT	Software reset flag. Indicates that the last reset was caused by software. 0 Last reset not caused by software 1 Last reset caused by software

Table 10-4. RSR Field Descriptions (continued)

Field	Description
4 WDRCHIP	On-chip watchdog timer reset flag. Indicates that the last reset was caused by the on-chip watchdog timer timeout. 0 Last reset not caused by watchdog timer timeout 1 Last reset caused by watchdog timer timeout
3 POR	Power-on reset flag. Indicates that the last reset was caused by a power-on reset. 0 Last reset not caused by power-on reset 1 Last reset caused by power-on reset
2 EXT	External reset flag. Indicates that the last reset was caused by an external device or circuitry asserting the external RESET pin. 0 Last reset not caused by external reset 1 Last reset caused by external reset
1 WDRCORE	Core watchdog timer reset flag. Indicates that the last reset was caused by the core watchdog timer timeout. 0 Last reset not caused by watchdog timer timeout 1 Last reset caused by watchdog timer timeout
0 LOL	Loss-of-lock reset flag. Indicates that the last reset state was caused by a PLL loss of lock. 0 Last reset not caused by loss of lock 1 Last reset caused by a loss of lock

10.4 Functional Description

10.4.1 Reset Sources

Table 10-5 defines the sources of reset and the signals driven by the reset controller.

Table 10-5. Reset Source Summary

Source	Type
Power on	Asynchronous
External RESET pin (not stop mode)	Synchronous
External RESET pin (during stop mode)	Asynchronous
Core Watchdog timer	Synchronous
On-chip watchdog timer	Synchronous
Loss of lock	Asynchronous
Software	Synchronous

To protect data integrity, a synchronous reset source is not acted upon by the reset control logic until the end of the current bus cycle. Reset is then asserted on the next rising edge of the system clock after the cycle is terminated. Internal byte, word, or longword writes are guaranteed to complete without data corruption when a synchronous reset occurs. External writes, including longword writes to 16-bit ports, are also guaranteed to complete.

Asynchronous reset sources usually indicate a catastrophic failure. Therefore, the reset control logic does not wait for the current bus cycle to complete. Reset is asserted immediately to the system.

10.4.1.1 Power-On Reset

At power up, the reset controller asserts $\overline{\text{RSTOUT}}$. $\overline{\text{RSTOUT}}$ continues to be asserted until V_{DD} has reached a minimum acceptable level and, if PLL clock mode is selected, until the PLL achieves phase lock. Then after approximately another 512 cycles, $\overline{\text{RSTOUT}}$ is negated and the device begins operation.

10.4.1.2 External Reset

Asserting the external $\overline{\text{RESET}}$ for at least four rising FB_CLK edges causes the external reset request to be recognized and latched. The reset controller asserts $\overline{\text{RSTOUT}}$ for approximately 512 cycles after $\overline{\text{RESET}}$ is negated and the PLL has acquired lock. The device then exits reset and begins operation.

In low-power stop mode, the system clocks are stopped. Asserting the external $\overline{\text{RESET}}$ in stop mode causes an external reset to be recognized asynchronously.

10.4.1.3 On-chip Watchdog Timer Reset

An on-chip watchdog timer timeout causes timer reset request to be recognized and latched. If the $\overline{\text{RESET}}$ pin is negated and the PLL has acquired lock, the reset controller asserts $\overline{\text{RSTOUT}}$ for approximately 512 cycles. Then the device exits reset and begins operation.

10.4.1.4 Core Watchdog Timer Reset

A core watchdog timer timeout causes timer reset request to be recognized and latched. If the $\overline{\text{RESET}}$ pin is negated and the PLL has acquired lock, the reset controller asserts $\overline{\text{RSTOUT}}$ for approximately 512 cycles. Then the device exits reset and begins operation.

10.4.1.5 Loss-of-Lock Reset

This reset condition occurs when the device is operating in PLL mode and the PLL loses lock. The reset controller asserts $\overline{\text{RSTOUT}}$ for approximately 512 cycles after the PLL has acquired lock. The device then exits reset and resumes operation.

When operating in limp mode and the PLL loses lock (e.g. when changing PLL frequencies) this reset does not occur.

10.4.1.6 Software Reset

A software reset occurs when the $\text{RCR}[\text{SOFTTRST}]$ bit is set. If the $\overline{\text{RESET}}$ is negated and the PLL has acquired lock, the reset controller asserts $\overline{\text{RSTOUT}}$ for approximately 512 cycles. Then the device exits reset and resumes operation.

10.4.2 Reset Control Flow

The reset logic control flow is shown in [Figure 10-4](#). In this figure, the control state boxes have been numbered, and these numbers are referred to (within parentheses) in the flow description that follows. All cycle counts given are approximate.

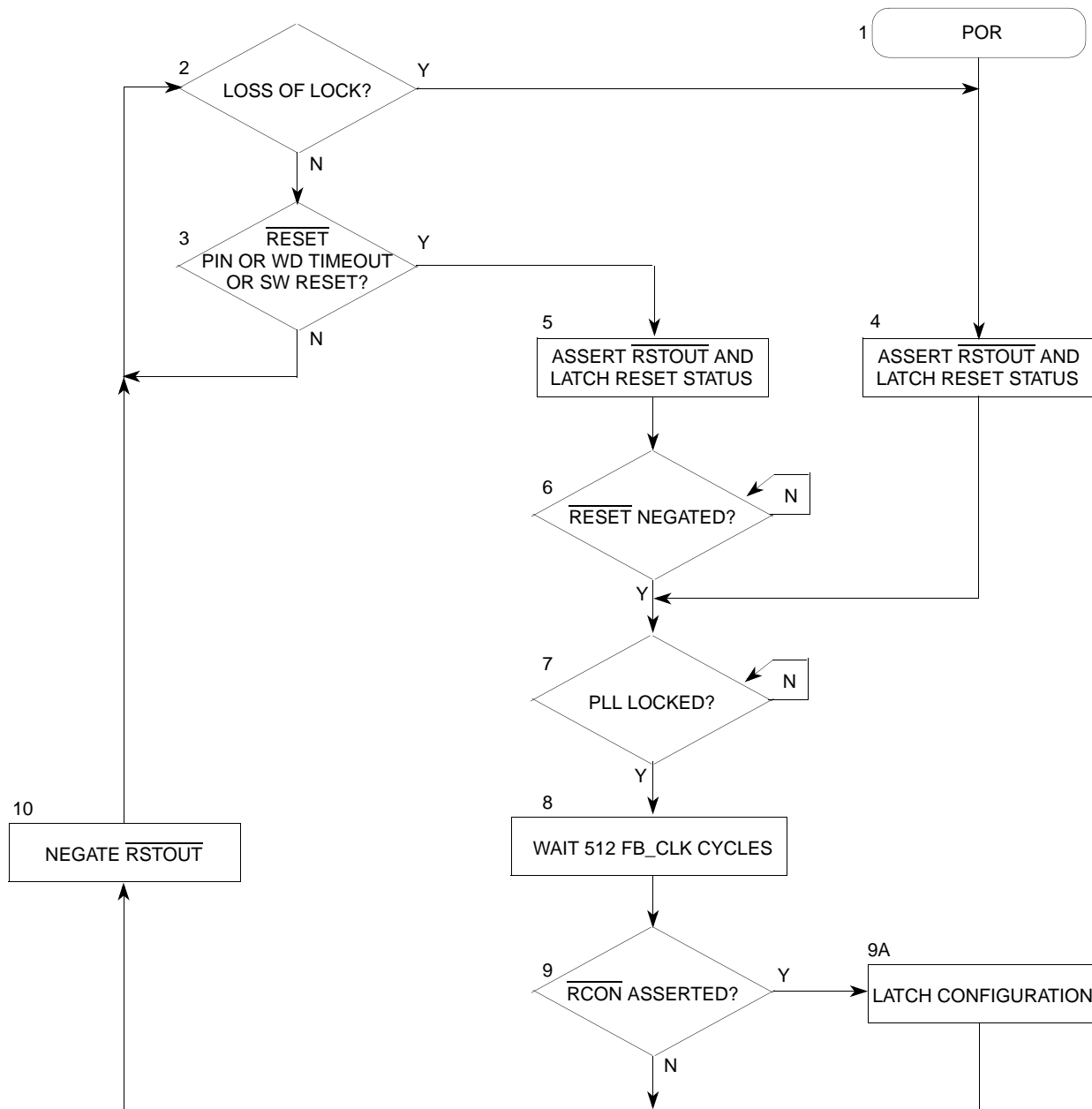


Figure 10-4. Reset Control Flow

10.4.2.1 Synchronous Reset Requests

In this discussion, the reference in parentheses refer to the state numbers in [Figure 10-4](#). All cycle counts given are approximate.

If the external $\overline{\text{RESET}}$ signal is asserted by an external device for at least four rising FB_CLK edges (3), if the watchdog timer times out, or if software requests a reset, the reset control logic latches the reset request internally. At this point the RSTOUT pin is asserted (5). The reset control logic waits until the $\overline{\text{RESET}}$ signal is negated (6) and for the PLL to attain lock (7) before waiting 512 FB_CLK cycles (8). The

reset control logic may latch the configuration according to the $\overline{\text{RCON}}$ signal level (9, 9A) before negating $\overline{\text{RSTOUT}}$ (10).

If the external $\overline{\text{RESET}}$ signal is asserted by an external device for at least four rising FB_CLK edges during the 512 count (8) or during the wait for PLL lock (7), the reset flow switches to (6) and waits for the $\overline{\text{RESET}}$ signal to be negated before continuing.

10.4.2.2 Internal Reset Request

If reset is asserted by an asynchronous internal reset source, such as loss of clock (1), the reset control logic asserts $\overline{\text{RSTOUT}}$ (4). The reset control logic waits for the PLL to attain lock (7) before waiting 512 FB_CLK cycles (8). Then the reset control logic may latch the configuration according to the $\overline{\text{RCON}}$ pin level (9, 9A) before negating $\overline{\text{RSTOUT}}$ (10).

If loss of lock occurs during the 512 count (8), the reset flow switches to (7) and waits for the PLL to lock before continuing.

10.4.2.3 Power-On Reset

When the reset sequence is initiated by power-on reset (1), the same reset sequence is followed as for the other asynchronous reset sources.

10.4.3 Concurrent Resets

This section describes the concurrent resets. As in the previous discussion references in parentheses refer to the state numbers in [Figure 10-4](#).

10.4.3.1 Reset Flow

If a power-on reset is detected during any reset sequence, the reset sequence starts immediately (1).

If the external $\overline{\text{RESET}}$ pin is asserted for at least four rising FB_CLK edges while waiting for PLL lock or the 512 cycles, the external reset is recognized. Reset processing switches to wait for the external $\overline{\text{RESET}}$ pin to negate (6).

If a loss-of-lock condition is detected during the 512 cycle wait, the reset sequence continues after a PLL lock (7).

10.4.3.2 Reset Status Flags

For a POR reset, the RSR[POR] bit is set, and all other RSR flags are cleared even if another type of reset condition is pending or concurrently asserted.

If other sources of reset are asserted after the RSR status bits have been latched (4 or 5), the device is held in reset (8) until all sources have negated and the subsequent sources are not reflected in the RSR contents.

Chapter 11

System Control Module (SCM)

11.1 Introduction

This system control module (SCM) provides several control functions, including peripheral access control, a software core watchdog timer, and generic access error information for the processor core.

11.1.1 Overview

The SCM provides programmable access protections for both masters and peripherals. It allows the privilege level of a master to be overridden, forcing it to user-mode privilege, and allows masters to be designated as trusted or untrusted. Peripherals may be programmed to require supervisor privilege level for access, may restrict access to a trusted master only, and may be write-protected.

The SCM's core watchdog timer (CWT) provides a means of preventing system lockup due to uncontrolled software loops via a special software service sequence. If periodic software servicing action does not occur, the CWT times out with a programmed response (system reset or interrupt) to allow recovery or corrective action to be taken.

NOTE

The core watchdog timer is available to provide compatibility with the watchdog timer implemented on previous ColdFire devices. However, there is a second watchdog timer available that has new features. See [Chapter 20, “Watchdog Timer Module,”](#) for more information.

Fault access reporting is also available within the SCM. The user can use these registers during the resulting interrupt service routine and perform an appropriate recovery.

11.1.2 Features

The SCM includes these distinctive features:

- Access control registers
 - Master privilege register (MPR)
 - Peripheral access control registers (PACRs)
- System control registers
 - Core watchdog control register (CWCR) for watchdog timer control
 - Core watchdog service register (CWSR) to service watchdog timer
 - SCM interrupt status register (SCMISR) to service a bus fault or watchdog interrupt
 - Bus monitor timeout register (BMT)

- Core fault reporting registers

11.2 Memory Map/Register Definition

The memory map for the SCM registers is shown in [Table 11-1](#).

Attempted accesses to reserved addresses result in a bus error, while attempted writes to read-only registers are ignored and do not terminate with an error. Unless noted otherwise, writes to the programming model must match the size of the register, e.g., an 8-bit register only supports 8-bit writes, etc. Attempted writes of a different size than the register width produce a bus error and no change to the targeted register.

Table 11-1. SCM Memory Map

Address	Register	Width (bits)	Access	Reset Value	Section/Page
0xFC00_0000	Master Privilege Register (MPR)	32	R/W	0x7777_7777	11.2.1/11-2
0xFC00_0020	Peripheral Access Control Register A (PACRA)	32	R/W	0x5444_4444	11.2.2/11-3
0xFC00_0024	Peripheral Access Control Register B (PACRB)	32	R/W	0x4444_4444	11.2.2/11-3
0xFC00_0028	Peripheral Access Control Register C (PACRC)	32	R/W	0x4444_4444	11.2.2/11-3
0xFC00_002C	Peripheral Access Control Register D (PACRD)	32	R/W	0x4444_4444	11.2.2/11-3
0xFC00_0040	Peripheral Access Control Register E (PACRE)	32	R/W	0x4444_4444	11.2.2/11-3
0xFC00_0044	Peripheral Access Control Register F (PACRF)	32	R/W	0x4444_4444	11.2.2/11-3
0xFC00_0054	Bus Monitor Timeout (BMT)	32	R/W	0x0000_0008	11.2.3/11-6
0xFC04_0013	Wakeup Control Register (WCR) ¹	8	R/W	0x00	8.2.1/8-2
0xFC04_0016	Core Watchdog Control Register (CWCR)	16	R/W	0x0000	11.2.4/11-7
0xFC04_001B	Core Watchdog Service Register (CWSR)	8	R/W	Undefined	11.2.5/11-8
0xFC04_001F	SCM Interrupt Status Register (SCMISR)	8	R/W	0x00	11.2.6/11-8
0xFC04_0070	Core Fault Address Register (CFADR)	32	R	0x0000_0000	11.2.7/11-9
0xFC04_0075	Core Fault Interrupt Enable Register (CFIER)	8	R/W	0x00	11.2.8/11-10
0xFC04_0076	Core Fault Location Register (CFLOC)	8	R	Undefined	11.2.9/11-10
0xFC04_0077	Core Fault Attributes Register (CFATR)	8	R	Undefined	11.2.10/11-10
0xFC04_007C	Core Fault Data Register (CFDTR)	32	R	Undefined	11.2.11/11-11

¹ The WCR register is described in [Chapter 8, "Power Management."](#)

11.2.1 Master Privilege Register (MPR)

The MPR specifies three 4-bit fields defining the access privilege level associated with a bus master in the device to the various peripherals listed in [Table 11-4](#). The register provides one field per bus master.

Address: 0xFC00_0000 (MPR)

Access: User read/write

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	MPROT0				MPROT1				MPROT2				0	1	1	1	0	1	1	1	0	1	1	1	0	1	1	1	0	1	1	1
W																																
Reset	0	1	1	1	0	1	1	1	0	1	1	1	0	1	1	1	0	1	1	1	0	1	1	1	0	1	1	1	0	1	1	1

Figure 11-1. Master Privilege Register (MPR)

Each master is assigned depending on its connection to the various cross-bar switch master ports.

Table 11-2. MPROT n Assignments

Cross-bar Switch Port Number	MPROT n	Master
M0	MPROT0	ColdFire Core
M1	MPROT1	eDMA Controller
M2	MPROT2	FEC

The MPROT n field is defined as shown below.

	3	2	1	0
R	0	MTR	MTW	MPL
W				

Figure 11-2. MPROT n FieldsTable 11-3. MPROT n Field Descriptions

Field	Description
3	Reserved, should be cleared.
2 MTR	Master trusted for read. Determines whether the master is trusted for read accesses. 0 This master is not trusted for read accesses. 1 This master is trusted for read accesses.
1 MTW	Master trusted for writes. Determines whether the master is trusted for write accesses. 0 This master is not trusted for write accesses. 1 This master is trusted for write accesses.
0 MPL	Master privilege level. Determines how the privilege level of the master is determined. 0 Accesses from this master are forced to user-mode. 1 Accesses from this master are not forced to user-mode.

11.2.2 Peripheral Access Control Registers (PACRx)

Each of the peripherals has a four-bit PACR n field which defines the access levels supported by the given module. Eight PACRs are grouped together to form a 32-bit PACRx register (PACRA-PACRF). At reset the SCM (PACR0) does not allow access from untrusted masters, while the other peripherals do.

Address: 0xFC00_0020 (PACRA)

Access: User read/write

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RW	PACR0				PACR1				PACR2				0	1	0	0	0	1	0	0	0	1	0	0	0	1	0	0	0	1	0	0
Reset	0	1	0	1	0	1	0	0	0	1	0	0	0	1	0	0	0	1	0	0	0	1	0	0	0	1	0	0	0	1	0	0

Figure 11-3. Peripheral Access Control Register A (PACRA)

Address: 0xFC00_0024 (PACRB)

Access: User read/write

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	0	1	0	0	0	1	0	0	0	1	0	0	0	1	0	0	PACR12				0	1	0	0	0	1	0	0	0	1	0	0
W																																
Reset	0	1	0	0	0	1	0	0	0	1	0	0	0	1	0	0	0	1	0	0	0	1	0	0	0	1	0	0	0	1	0	0

Figure 11-4. Peripheral Access Control Register B (PACRB)

Address: 0xFC00_0028 (PACRC)

Access: User read/write

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	PACR16				PACR17				PACR18				0	1	0	0	0	1	0	0	PACR21				PACR22				PACR23			
W																																
Reset	0	1	0	0	0	1	0	0	0	1	0	0	0	1	0	0	0	1	0	0	0	1	0	0	0	1	0	0	0	1	0	0

Figure 11-5. Peripheral Access Control Register C (PACRC)

Address: 0xFC00_002C (PACRD)

Access: User read/write

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	PACR24				PACR25				PACR26				0	1	0	0	PACR28				PACR29				PACR30				PACR31			
W																																
Reset	0	1	0	0	0	1	0	0	0	1	0	0	0	1	0	0	0	1	0	0	0	1	0	0	0	1	0	0	0	1	0	0

Figure 11-6. Peripheral Access Control Register D (PACRD)

Address: 0xFC00_0040 (PACRE)

Access: User read/write

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0		
R	PACR32				PACR33				PACR34				PACR35				PACR36				0	1	0	0	0	1	0	0	0	1	0	0		
W																																		
Reset	0	1	0	0	0	1	0	0	0	1	0	0	0	1	0	0	0	1	0	0	0	1	0	0	0	1	0	0	0	1	0	0		

Figure 11-7. Peripheral Access Control Register E (PACRE)

Address: 0xFC00_0044 (PACRF)

Access: User read/write

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	PACR40				PACR41				PACR42				0	1	0	0	0	1	0	0	0	1	0	0	0	1	0	0	0	1	0	0
W																																
Reset	0	1	0	0	0	1	0	0	0	1	0	0	0	1	0	0	0	1	0	0	0	1	0	0	0	1	0	0	0	1	0	0

Figure 11-8. Peripheral Access Control Register F (PACRF)

Each peripheral is assigned to its PACR_n field as shown below:

Table 11-4. PACR n Assignments

Slot Number	PACR n	Peripheral
0	PACR0	SCM (MPR & PACRs)
1	PACR1	Cross-bar switch
2	PACR2	FlexBus
12	PACR12	FEC
16	PACR16	SCM (CWT & Core Fault Registers)
17	PACR17	eDMA Controller
18	PACR18	Interrupt Controller 0
21	PACR21	Interrupt Controller IACK
22	PACR22	I ² C
23	PACR23	QSPI
24	PACR24	UART0
25	PACR25	UART1
26	PACR26	UART2
28	PACR28	DMA Timer 0
29	PACR29	DMA Timer 1
30	PACR30	DMA Timer 2
31	PACR31	DMA Timer 3
32	PACR32	PIT 0
33	PACR33	PIT 1
34	PACR34	Edge Port
35	PACR35	On-chip Watchdog Timer
36	PACR36	PLL
40	PACR40	CCM, Reset Controller, Power Management
41	PACR41	GPIO Module
42	PACR42	SDRAM Controller

The PACR n field is defined as shown below.

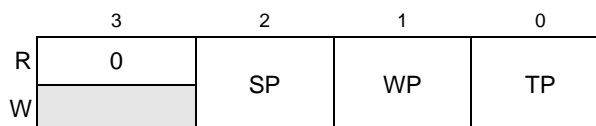
Figure 11-9. PACR n Fields

Table 11-5. PACR n Field Descriptions

Field	Description
3	Reserved, should be cleared.
2 SP	Supervisor protect. Determines whether the peripheral requires supervisor privilege level for access. 0 This peripheral does not require supervisor privilege level for accesses. 1 This peripheral requires supervisor privilege level for accesses. The master privilege level must indicate supervisor access attribute, and the MPROT n [MPL] control bit for the master must be set. If not, the access is terminated with an error response and no peripheral access is initiated.
1 WP	Write protect. Determines whether the peripheral allows write accesses 0 This peripheral allows write accesses. 1 This peripheral is write protected. If a write access is attempted, the access is terminated with an error response and no peripheral access is initiated.
0 TP	Trusted Protect. Determines whether the peripheral allows accesses from an untrusted master. 0 Accesses from an untrusted master are allowed. 1 Accesses from an untrusted master are not allowed. If an access is attempted by an untrusted master, the access is terminated with an error response and no peripheral access is initiated.

11.2.3 Bus Monitor Timeout Register (BMT)

Each AIPS controller implements a bus timeout monitor to insure that every bus cycle is properly terminated within a programmed period of time. The monitor continually checks for termination of each bus cycle and completes the cycle if there is no response when the programmed monitor cycle count is reached.

The monitor can be programmed from 8–1024 internal bus cycles under control of the BMT register. If the programmed timeout value is reached before a termination, the bus monitor completes the cycle with an error termination. Thus, the SCMISR[CFEI] bit is set, and an interrupt to the interrupt controller is generated if the CFIER[ECFEI] bit is set. At reset, the BMT is enabled with a maximum timeout value.

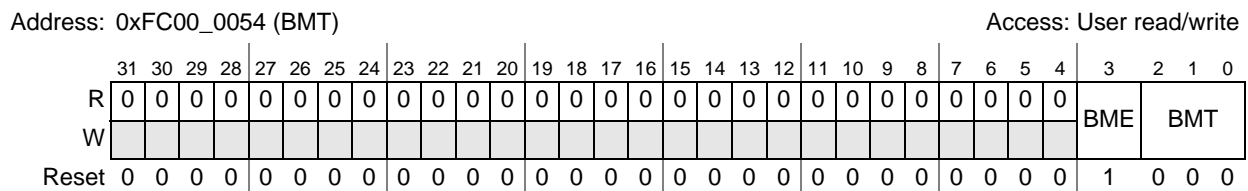


Figure 11-10. Bus Monitor Timeout Register (BMT)

Table 11-6. BMT Field Descriptions

Field	Description
31–4	Reserved, should be cleared.

Table 11-6. BMT Field Descriptions (continued)

Field	Description
3 BME	Bus monitor timeout enable. 0 BMT disabled 1 BMT enabled
2–0 BMT	Bus monitor timeout period. Indicates the timeout period in internal bus cycles for the bus monitor. 000 1024 cycles 001 512 cycles 010 256 cycles 011 128 cycles 100 64 cycles 101 32 cycles 110 16 cycles 111 8 cycles

11.2.4 Core Watchdog Control Register (CWCR)

The CWCR controls the software watchdog timer, time-out periods, and software watchdog timer interrupt. The register can be read or written at any time. At system reset, the software watchdog timer is disabled.

Address: 0xFC04_0016 (CWCR)

Access: User read/write

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	RO	0	0	0	0	0	0	CW RWH	CWE	CWRI						
W																
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Figure 11-11. Core Watchdog Control Register (CWCR)

Table 11-7. CWCR Field Descriptions

Field	Description
15 RO	Read-only control bit. 0 CWCR can be read or written. 1 CWCR is read-only. A system reset is required to clear this register. The setting of this bit is intended to prevent accidental writes of the CWCR from changing the defined core watchdog configuration.
14–9	Reserved, should be cleared.
8 CWRWH	Core watchdog run while halted. 0 Core watchdog timer stops counting if the core is halted. 1 Core watchdog timer continues to count even while the core is halted.
7 CWE	Core watchdog timer enable. 0 CWT is disabled. 1 CWT is enabled.

Table 11-7. CWCR Field Descriptions (continued)

Field	Description
6–5 CWRI	Core watchdog reset/interrupt. 00 If a time-out occurs, the CWT generates an interrupt to the core. Refer to Chapter 14, “Interrupt Controller Module,” for details on setting its priority level. 01 The first time-out generates an interrupt to the processor, and if not serviced, a second time-out generates a system reset and sets the RSR[WDRCORE] flag in the reset controller. 10 If a time-out occurs, the CWT generates a system reset and RSR[WDRCORE] in the reset controller is set. 11 The CWT functions in a “window” mode of operation. For this mode, the servicing of the CWSR must occur during the last 25% of the time-out period. Any writes to the CWSR during the first 75% of the time-out period generate an immediate system reset. Likewise, if the CWSR is not serviced during the last 25% of the time-out period, a system reset is generated. For any type of reset response, the RSR[WDRCORE] flag is set.
4–0 CWT	Core watchdog time-out period. Selects the time-out period for the CWT. At reset, this field is cleared selecting the minimum time-out period, but the CWT is disabled since CWCR[CWE] = 0 at reset. For CWCR[CWT] = n , time-out period = 2^n system clock cycles, where $n = 8–31$. If $n < 8$, then time-out period is forced to 2^8 .

11.2.5 Core Watchdog Service Register (CWSR)

The software watchdog service sequence must be performed using the CWSR as a data register to prevent a CWT time-out. The service sequence requires two writes to this data register: first a write of 0x55 followed by a write of 0xAA. Both writes must be performed in this order prior to the CWT time-out, but any number of instructions can be executed between the two writes. If the CWT has already timed out, writing to this register has no effect in negating the CWT interrupt or reset. [Figure 11-12](#) illustrates the CWSR. At system reset, the contents of CWSR are uninitialized.

NOTE

If the CWT is enabled and has not timed out, then any write of a data value other than 0x55 or 0xAA causes an immediate system reset, regardless of the value in the CWCR[CWRI] field.

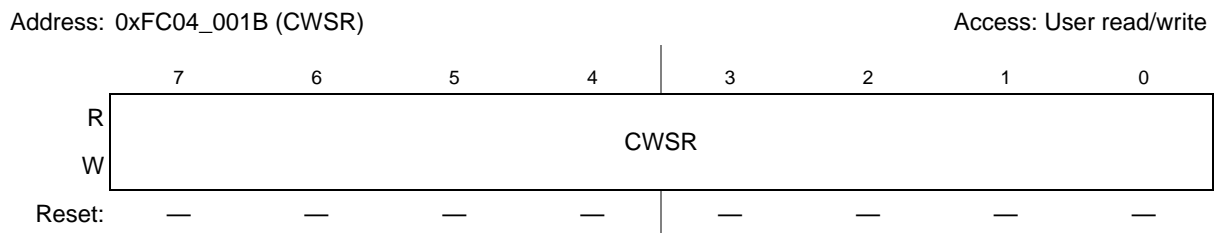


Figure 11-12. Core Watchdog Service Register (CWSR)

11.2.6 SCM Interrupt Status Register (SCMISR)

For certain values in the CWCR[CWRI] field, the CWT generates an interrupt response to a time-out. For these configurations, the SCMISR provides a program visible interrupt request from the watchdog timer. During the interrupt service routine which handles this interrupt, the source must be explicitly cleared by writing a 0x01 to the SCMISR.

The SCMISR also indicates system bus fault errors. An interrupt will only be sent to the interrupt controller when the CFIER[ECFEI] bit is set. The SCMISR[CFEI] bit flags fault errors independent of the CFIER[ECFEI] setting. Therefore, if CFEI is set prior to setting ECFEI, an interrupt is requested immediately after ECFEI is set.

Address: 0xFC04_001F (SCMISR)

Access: User read/write

	7	6	5	4	3	2	1	0
R	0	0	0	0	0	0	CFEI	CWIC
W							w1c	w1c
Reset:	0	0	0	0	0	0	0	0

Figure 11-13. SCM Interrupt Status Register (SCMISR)

Table 11-8. SCMISR Field Descriptions

Field	Description
7–2	Reserved, should be cleared.
1 CFEI	Core fault error interrupt flag. Indicates if a bus fault has occurred. 0 No bus error. 1 A bus error has occurred. The faulting address, attributes (and possibly write data) are captured in the CFADR, CFATR, and CFDTR registers. The error interrupt is only enabled if CFLOC[ECFEI] is set. The interrupt request is negated by writing a 1 to this bit. Writing a 0 has no effect. Note: This bit reports core faults regardless of the setting of CFIER[ECFEI]. Therefore, if the error interrupt is disabled and a core fault occurs, this bit is set. Then, if the error interrupt is subsequently enabled, an interrupt is immediately requested. To prevent an undesired interrupt, clear the captured error by writing one to CFEI before enabling the interrupt.
0 CWIC	Core watchdog interrupt flag. Indicates whether an CWT interrupt has occurred. 0 No CWT interrupt has occurred. 1 CWT interrupt has occurred. Writing a 1 clears this bit and negates the interrupt request. Writing a 0 has no effect.

11.2.7 Core Fault Address Register (CFADR)

The CFADR is a read-only register for indicating the address of the last core access which was terminated with an error response.

Address: 0xFC04_0070 (CFADR)

Access: User read-only

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	ADDR																															
W																																
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Figure 11-14. Core Fault Address Register (CFADR)

Table 11-9. CFADR Field Descriptions

Field	Description
31–0 ADDR	Indicates the faulting address of the last core access terminated with an error response.

11.2.8 Core Fault Interrupt Enable Register (CFIER)

The CFIER register is used to enable the system bus error interrupt. See [Chapter 14, “Interrupt Controller Module,”](#) for more information of the interrupt controller.

Address: 0xFC04_0075 (CFIER)

Access: User read/write

	7	6	5	4	3	2	1	0
R	0	0	0	0	0	0	0	ECFEI
W								
Reset:	0	0	0	0	0	0	0	0

Figure 11-15. Core Fault Interrupt Enable Register (CFIER)

Table 11-10. CFIER Field Descriptions

Field	Description
7–1	Reserved, should be cleared.
0 ECFEI	Enable core fault error interrupt. 0 Do not generate an error interrupt on a faulted system bus cycle. 1 Generate an error interrupt to the interrupt controller on a faulted system bus cycle.

11.2.9 Core Fault Location Register (CFLOC)

The read-only CFLOC register indicates the exact location within the device of the captured fault information.

Address: 0xFC04_0076 (CFLOC)

Access: User read-only

	7	6	5	4	3	2	1	0
R	LOC	0	0	0	0	0	0	0
W								
Reset:	–	0	0	0	0	0	0	0

Figure 11-16. Core Fault Location Register (CFLOC)

Table 11-11. CFLOC Field Descriptions

Field	Description
7 LOC	The location of the last captured fault. 0 Error occurred on the internal bus. 1 Error occurred within the core.
6–0	Reserved, should be cleared.

11.2.10 Core Fault Attributes Register (CFATR)

The read-only CFATR register captures the processor’s attributes of the last faulted core access to the system bus.

Address: 0xFC04_0077 (CFATR)

Access: User read-only

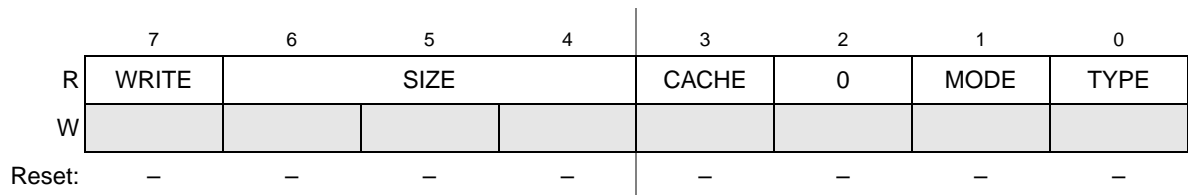


Figure 11-17. Core Fault Attributes Register (CFATR)

Table 11-12. CFATR Field Descriptions

Field	Description
7 WRITE	Indicates the direction of the last faulted core access. 0 Core read access. 1 Core write access.
6–4 SIZE	Indicates the size of the last faulted core access. 000 8-bit core access. 001 16-bit core access. 010 32-bit core access. Else Reserved.
3 CACHE	Indicates if last faulted core access was cacheable. 0 Non-cacheable 1 Cacheable
2	Reserved, should be cleared.
1 MODE	Indicates the mode the device was in during the last faulted core access. 0 User mode 1 Supervisor mode
0 TYPE	Defines the type of last faulted core access. 0 Instruction 1 Data

11.2.11 Core Fault Data Register (CFDTR)

The CFDTR is a read-only register for capturing the data associated with the last faulted processor write data access from the device's internal bus. The CFDTR is only valid for faulted internal bus write accesses, CFLOC[LOC] = 0.

Address: 0xFC04_007C (CFDTR)

Access: User read-only

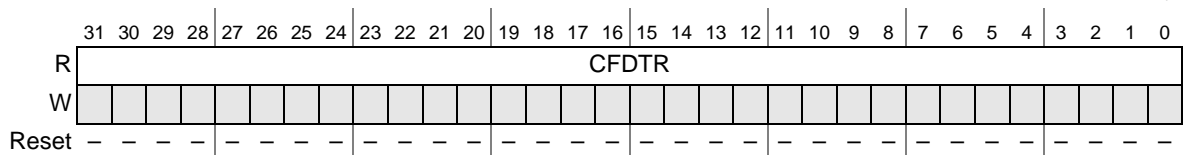


Figure 11-18. Core Fault Data Register (CFDTR)

Table 11-13. CFDTR Field Descriptions

Field	Description
31–0 CFDTR	Contains the data associated with the faulting access of the last internal bus write access. The register contains the data value taken directly from the write data bus.

11.3 Functional Description

11.3.1 Access Control

The SCM supports the traditional model of two privilege levels: supervisor and user. Typically, memory references with the supervisor attribute have total accessibility to all the resources in the system, while user mode references cannot access system control and configuration registers. In many systems, the operating system executes in supervisor mode, while application software executes in user mode.

The SCM further partitions the access control functions into two parts: one control register defines the privilege level associated with each bus master (MPR), and another set of control registers define the access levels associated with the peripheral modules (PACR_x).

Each bus transaction targeted for the peripheral space is first checked to see if its privilege rights allow access to the given memory space. If the privilege rights are correct, the access proceeds on the internal bus. If the privilege rights are insufficient for the targeted memory space, the transfer is immediately aborted and terminated with an exception, and the targeted module not accessed.

11.3.2 Core Watchdog Timer

The core watchdog timer (CWT) prevents system lockup if the software becomes trapped in a loop with no controlled exit or if a bus transaction becomes hung. The core watchdog timer can be enabled through CWCW[CWE]; it is disabled at reset. If enabled, the CWT requires the periodic execution of a core watchdog servicing sequence. If this periodic servicing action does not occur, the timer expires and, depending on the setting of CWCW[CWRI], different events may occur:

1. An interrupt may be generated to the core.
2. An immediate system reset.
3. Upon the first time-out, a watchdog timer interrupt is asserted. If this time-out condition is not serviced before a second time-out occurs, the CWT asserts a system reset. This configuration supports a more graceful response to watchdog time-outs.
4. In addition to these three basic modes of operation, the CWT also supports a windowed mode of operation. In this mode, the time-out period is divided into four equal segments and the entire service sequence of the CWT must occur during the last segment (last 25% of the time-out period). If the timer is serviced anytime (any write to the CWSR register) in the first 75% of the time-out period, an immediate system reset occurs.

To prevent the core watchdog timer from interrupting or resetting, the CWSR register must be serviced by performing the following sequence:

1. Write 0x55 to CWSR.

2. Write 0xAA to CWSR.

Both writes must occur in order before the time-out, but any number of instructions can be executed between the two writes. This allows interrupts and exceptions to occur, if necessary, between the two writes.

NOTE

If the CWT is enabled and has not timed out, then any write of a data value other than 0x55 or 0xAA will cause an immediate system reset, regardless of the value in the CWCR[CWRI] field.

The timer value is constantly compared with the time-out period specified by CWCR[CWT], and any write to the CWCR register resets the watchdog timer. In addition, there is a write-once control bit in the CWCR that sets the CWCR to read-only to prevent accidental updates to this control register from changing the desired system configuration. Once this bit, CWCR[RO], is set, a system reset is required to clear it.

For certain values in the CWCR[CWRI] field, the CWT generates an interrupt response to a time-out. For these configurations, the SCMISR register provides a program visible interrupt request from the watchdog timer. During the interrupt service routine which handles this interrupt, the source must be explicitly cleared by writing a 0x01 to the SCMISR.

11.3.3 Core Data Fault Recovery Registers

To aid in recovery from certain types of access errors, the SCM module supports a number of registers that capture access address, attribute, and data information on bus cycles terminated with an error response. These registers can then be read during the resulting exception service routine and the appropriate recovery performed.

The details on the core fault recovery registers are provided in the above sections. It is important to note these registers are used to capture fault recovery information on any processor-initiated system bus cycle that is terminated with an error.

Chapter 12

Crossbar Switch (XBS)

12.1 Overview

This section provides information on the layout, configuration, and programming of the crossbar switch. The crossbar switch connects the bus masters and bus slaves using a crossbar switch structure. This structure allows bus masters to access different bus slaves simultaneously with no interference while providing arbitration among the bus masters when they access the same slave. A variety of bus arbitration methods and attributes may be programmed on a slave by slave basis.

The MCF5208 devices have up to four masters and three slaves (4Mx3S) connected to the crossbar switch. The four masters are the ColdFire core, eDMA controller, FEC, and a reserved master for factory test. The slaves are FlexBus/SDRAM controller, SRAM controller, and the peripheral bus controller.

Figure 12-1 is a block diagram of the MCF5208 family bus architecture showing the crossbar switch configuration.

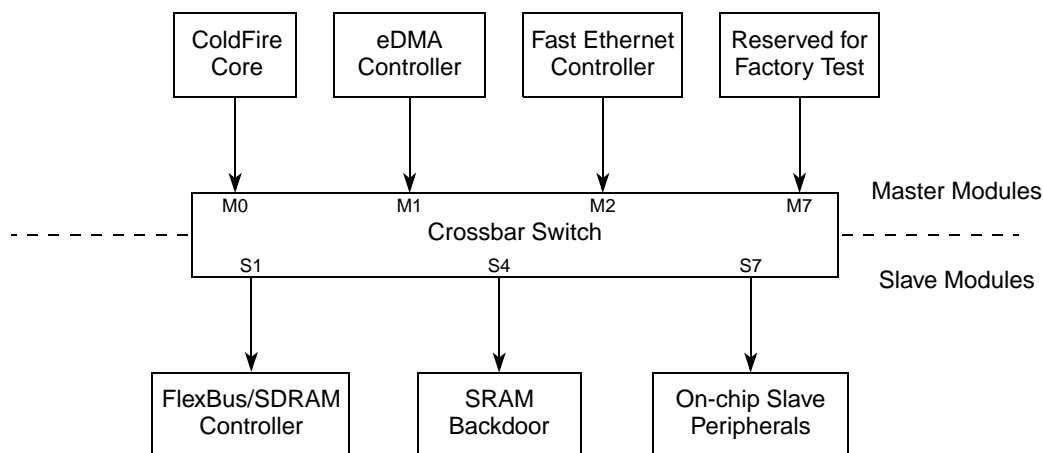


Figure 12-1. Bus Architecture Block Diagram

The modules are assigned to the numbered ports on the crossbar switch in the below table.

Table 12-1. Crossbar Switch Master/Slave Assignments

Master Modules		
Crossbar Port	Module	
Master 0 (M0)	ColdFire core	
Master 1 (M1)	eDMA controller	
Master 2 (M2)	Fast Ethernet controller	
Master 7 (M7)	Reserved for factory test	
Slave Modules		
Crossbar Port	Module	Address Range ¹
Slave 1 (S1)	Flexbus SDRAM Controller	0x0000_0000–0x3FFF_FFFF & 0xC000_0000–0xDFFF_FFFF 0x4000_0000–0x7FFF_FFFF
Slave 4 (S4)	Internal SRAM Backdoor	0x8000_0000–0x8FFF_FFFF
Slave 7 (S7)	Other on-chip slave peripherals	0xF000_0000–0xFFFF_FFFF ²

¹ Unused address spaces are reserved.

² See the various peripheral chapters for their memory maps. Any unused space by these peripherals within this memory range is reserved and must not be accessed.

NOTE

This memory map provides two disjoint regions mapped to the FlexBus controller to support glueless connections to external memories (e.g., flash and SRAM) and a second space with one (or more) unique chip-selects that can be used for non-cacheable, non-memory devices (addresses 0xC000_0000–0xDFFF_FFFF). Additionally, this mapping is easily maps into the ColdFire access control registers, which provide a coarse association between memory addresses and their attributes (e.g., cacheable, non-cacheable). For this device, one possible configuration defines the default memory attribute as non-cacheable, and one ACR then identifies cacheable addresses, e.g., ADDR[31] equals 0 identifies the cacheable space.

12.2 Features

The crossbar switch includes these distinctive features:

- Symmetric crossbar bus switch implementation
 - Allows concurrent accesses from different masters to different slaves
 - Slave arbitration attributes configured on a slave by slave basis
- 32 bits wide and supports byte, word (2 byte), longword (4 byte), and 16 byte burst transfers
- Operates at a 1-to-1 clock frequency with the bus masters

12.3 Modes of Operation

The crossbar switch supports two arbitration modes (fixed or round-robin), which may be set on a slave by slave basis. Slaves configured for fixed arbitration mode have a unique arbitration level assigned to each bus master.

In fixed priority mode, the highest priority active master accessing a particular slave is granted the master bus path to that slave. A higher priority master blocks access to a given slave from a lower priority master if the higher priority master continuously requests that slave. See [Section 12.5.1.1, “Fixed-Priority Operation.”](#)

In round-robin arbitration, active masters accessing a particular slave are initially granted the slave based on their master port number. Master priority is then modified in a wrap-around manner to give all masters fair access to the slave. See [Section 12.5.1.2, “Round-Robin Priority Operation.”](#)

12.4 Memory Map / Register Definition

Two registers reside in each slave port of the crossbar switch. Read- and write-transfers require two bus clock cycles. The registers can only be read from and written to in supervisor mode. Additionally, these registers can only be read from or written to by 32-bit accesses.

A bus error response is returned if an unimplemented location is accessed within the crossbar switch. See [Section 11.2.6, “SCM Interrupt Status Register \(SCMISR\).”](#)

The slave registers also feature a bit that, when set, prevents the registers from being written. The registers remain readable, but future write attempts have no effect on the registers and are terminated with a bus error response to the master initiating the write. The core, for example, takes a bus error interrupt.

[Table 12-2](#) shows the memory map for the crossbar switch program-visible registers.

Table 12-2. XBS Memory Map

Address	Register	Width (bits)	Access	Reset Value	Section/Page
0xFC00_4100	Priority Register Slave 1 (XBS_PRS1)	32	R/W	0x3000_0210	12.4.1/12-3
0xFC00_4110	Control Register Slave 1 (XBS_CRS1)	32	R/W	0x0000_0000	12.4.2/12-4
0xFC00_4400	Priority Register Slave 4 (XBS_PRS4)	32	R/W	0x3000_0210	12.4.1/12-3
0xFC00_4410	Control Register Slave 4 (XBS_CRS4)	32	R/W	0x0000_0000	12.4.2/12-4
0xFC00_4700	Priority Register Slave 7 (XBS_PRS7)	32	R/W	0x3000_0210	12.4.1/12-3
0xFC00_4710	Control Register Slave 7 (XBS_CRS7)	32	R/W	0x0000_0000	12.4.2/12-4

12.4.1 XBS Priority Registers (XBS_PRSn)

The priority registers (XBS_PRSn) set the priority of each master port on a per slave port basis and reside in each slave port. The priority register can be accessed only with 32-bit accesses. After the XBS_CRSn[RO] bit is set, the XBS_PRSn register can only be read; attempts to write to it have no effect on XBS_PRSn and result in a bus-error response to the master initiating the write.

Additionally, no two available master ports may be programmed with the same priority level, including reserved masters. Attempts to program two or more masters with the same priority level result in a bus-error response (see [Section 11.2.6, “SCM Interrupt Status Register \(SCMISR\)”](#)) and the XBS_PRSn is not updated.

Address: 0xFC00_4100 (XBS_PRS1)

Access: Supervisor read/write

0xFC00_4400 (XBS_PRS4)

0xFC00_4700 (XBS_PRS7)

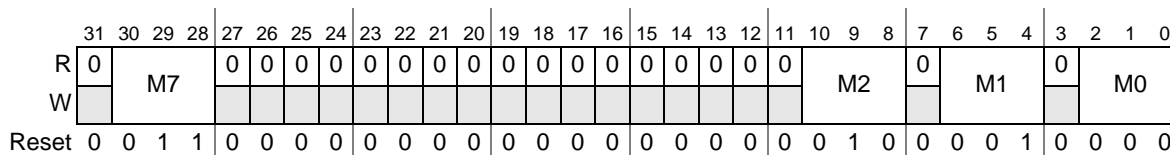
Figure 12-2. XBS Priority Registers Slave *n* (XBS_PRSn)

Table 12-3. XBS_PRSn Field Descriptions

Field	Description
31	Reserved, must be cleared.
30–28 M7	Master 7 (Factory Test) priority. Sets the arbitration priority for this port on the associated slave port. 000 This master has level 1 (highest) priority when accessing the slave port. 001 This master has level 2 priority when accessing the slave port. 010 This master has level 3 priority when accessing the slave port. 011 This master has level 4 (lowest) priority when accessing the slave port. Else Reserved
27–11	Reserved, must be cleared.
10–8 M2	Master 2 (FEC) priority. See M7 description.
7	Reserved, must be cleared.
6–4 M1	Master 1 (eDMA) priority. See M7 description.
3	Reserved, must be cleared.
2–0 M0	Master 0 (ColdFire core) priority. See M7 description.

NOTE

The possible values for the XBS_PRSn fields depend on the number of masters available on the device. Because the device contains four masters (including reserved masters), valid values are 000 to 011. Unpredictable results occur when using the reserved settings 100 to 111.

12.4.2 XBS Control Registers (XBS_CRSn)

The XBS control registers (XBS_CRSn) control several features of each slave port and must be accessed using 32-bit accesses. After XBS_CRSn[RO] is set, the XBS_CRSn can only be read; attempts to write to it have no effect and result in an error response.

Address: 0xFC00_4110 (XBS_PRS1)
 0xFC00_4410 (XBS_PRS4)
 0xFC00_4710 (XBS_PRS7)

Access: Supervisor read/write

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	RO ¹	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	ARB	0	0	PCTL	0				
W																																
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

¹ After this bit is set, only a hardware reset clears it.

Figure 12-3. XBS Control Registers Slave *n* (XBS_CRS*n*)

Table 12-4. XBS_CRS*n* Field Descriptions

Field	Description
31 RO	Read only. Forces both of the slave port's registers (XBS_CRS <i>n</i> and XBS_PRS <i>n</i>) to be read-only. After set, only a hardware reset clears it. 0 Both of the slave port's registers are writeable. 1 Both of the slave port's registers are read-only and cannot be written (attempted writes have no effect on the registers and result in a bus error response).
30–9	Reserved, must be cleared.
8 ARB	Arbitration Mode. Selects the arbitration policy for the slave port. 0 Fixed priority 1 Round robin (rotating) priority
7–6	Reserved, must be cleared.
5–4 PCTL	Parking control. Determines the slave port's parking control. The low-power park feature results in an overall power savings if the slave port is not saturated; however, this forces an extra latency clock when any master tries to access the slave port while not in use because it is not parked on any master. 00 When no master makes a request, the arbiter parks the slave port on the master port defined by the PARK bit field. 01 When no master makes a request, the arbiter parks the slave port on the last master to be in control of the slave port. 10 When no master makes a request, the slave port is not parked on a master and the arbiter drives all outputs to a constant safe state. 11 Reserved.
3	Reserved, must be cleared.
2–0 PARK	Park. Determines which master port the current slave port parks on when no masters are actively making requests and the PCTL bits are cleared. 000 Park on master port M0 (ColdFire Core) 001 Park on master port M1 (eDMA Controller) 010 Park on master port M2 (FEC) Else Reserved

12.5 Functional Description

12.5.1 Arbitration

The crossbar switch supports two arbitration schemes: a simple fixed-priority comparison algorithm and a simple round-robin fairness algorithm. The arbitration scheme is independently programmable for each slave port.

12.5.1.1 Fixed-Priority Operation

When operating in fixed-priority mode, each master is assigned a unique priority level in the XBS_PRSn (priority registers). If two masters request access to a slave port, the master with the highest priority in the selected priority register gains control over the slave port.

When a master makes a request to a slave port, the slave port checks if the new requesting master's priority level is higher than that of the master that currently has control over the slave port (unless the slave port is in a parked state). The slave port does an arbitration check at every bus transfer boundary makes certain that the proper master (if any) has control of the slave port.

If the new requesting master's priority level is higher than that of the master that currently has control of the slave port, the new requesting master is granted control over the slave port at the next clock edge. The exception to this rule is if the master that currently has control over the slave port is running a fixed length burst transfer or a locked transfer. In this case, the new requesting master must wait until the end of the burst transfer or locked transfer before it is granted control of the slave port.

If the new requesting master's priority level is lower than the master that currently has control of the slave port, the new requesting master is forced to wait until the current master runs one of the following cycles:

- An IDLE cycle
- A non-IDLE cycle to a location other than the current slave port.

12.5.1.2 Round-Robin Priority Operation

When operating in round-robin mode, each master is assigned a relative priority based on the master port number. This priority is based on how far ahead the master port number of the requesting master is to the master port number of the current bus master for this slave. Master port numbers are compared modulo the total number of bus masters, i.e. take the requesting master port number minus the current bus master's port number modulo the total number of bus masters. The master port with the highest priority based on this comparison is granted control over the slave port at the next bus transfer boundary.

After granted access to a slave port, a master may perform as many transfers as desired to that port until another master makes a request to the same slave port. The next master in line is granted access to the slave port at the next transfer boundary.

Parking may continue to be used in a round-robin mode, but does not affect the round-robin pointer unless the parked master actually performs a transfer. Handoff occurs to the next master in line after one cycle of arbitration. If the slave port is put into low-power park mode, the round-robin pointer is reset to point at master port 0, giving it the highest priority.

12.5.1.3 Priority Assignment

Each master port needs to be assigned a unique 3-bit priority level. If an attempt is made to program multiple master ports with the same priority level within the priority registers (XBS_PRS n) the crossbar switch responds with a bus error (refer to [Section 11.2.6, “SCM Interrupt Status Register \(SCMISR\)”](#)) and the registers are not updated.

12.6 Initialization/Application Information

No initialization is required by or for the crossbar switch. Hardware reset ensures all the register bits used by the crossbar switch are properly initialized to a valid state. Settings and priorities should be programmed to achieve maximum system performance.

Chapter 13

General Purpose I/O Module

13.1 Introduction

Many of the pins associated with the device may be used for several different functions. Their primary functions are to provide external interfaces to access off-chip resources. When not used for their primary function, many of the pins may be used as general-purpose digital I/O (GPIO) pins. In some cases, the pin function is set by the operating mode, and the alternate pin functions are not supported.

Each GPIO port has registers that configure, monitor, and control the port pins. [Figure 13-1](#) is a block diagram of the device ports. The GPIO functionality of the port IRQ pins is selected by the edge port module. They are shown in the below figure only for completeness.

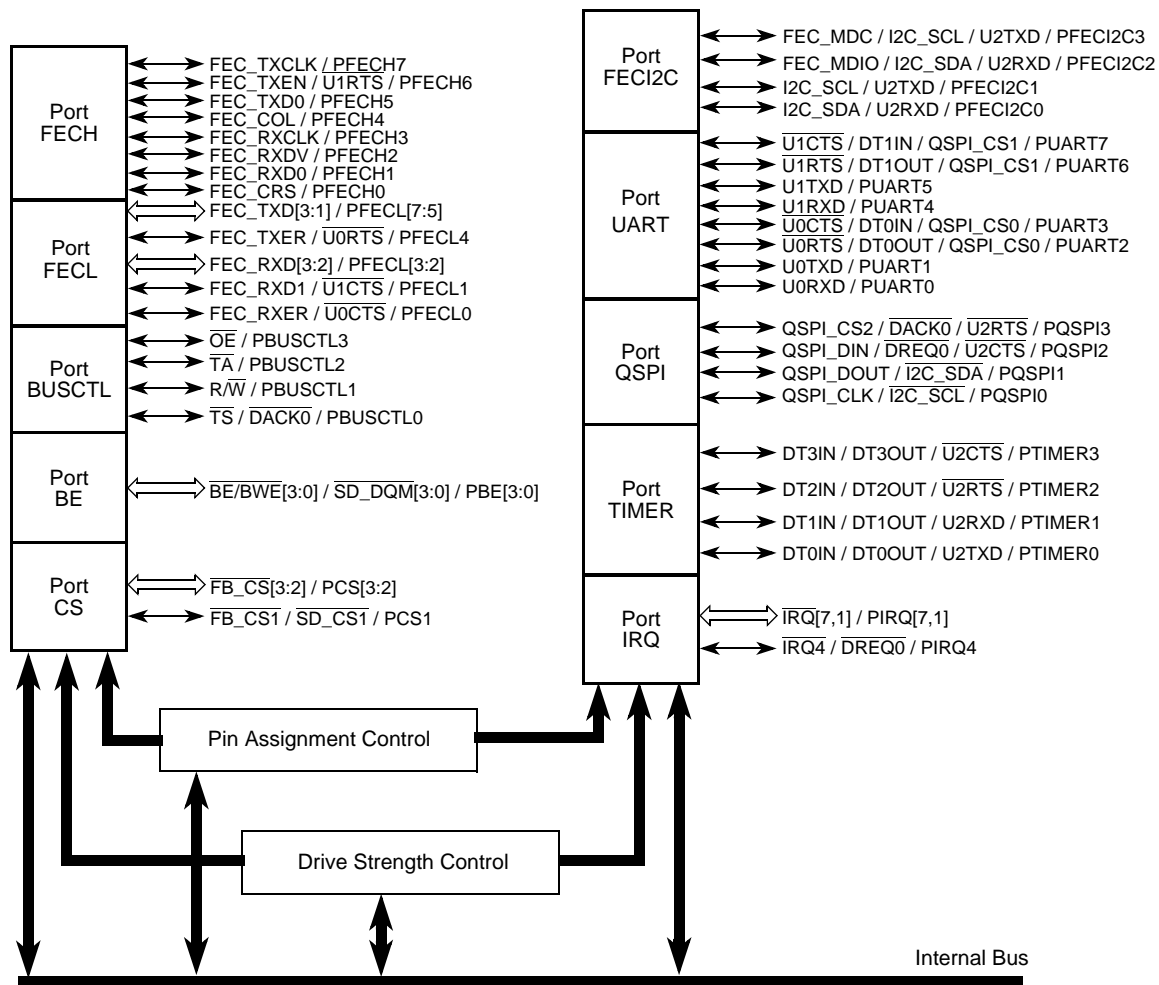


Figure 13-1. Ports Module Block Diagram

13.1.1 Overview

The GPIO module controls the configuration for various external pins, including those used for:

- External bus accesses
- External chip selection
- Ethernet data and control
- I²C serial control
- QSPI
- 32-bit DMA timers
- FEC
- UART

13.1.2 Features

The ports module includes these distinctive features:

- Control of primary function use
 - On all supported GPIO ports
 - On pins whose GPIO is not supported by ports module: $\overline{\text{IRQ4}}$
- General purpose I/O support for all ports
 - Registers for storing output pin data
 - Registers for controlling pin data direction
 - Registers for reading current pin state
 - Registers for setting and clearing output pin data registers

13.2 External Signal Description

The GPIO module controls the functionality of several external pins. These pins are listed in [Table 13-2](#) under the GPIO column.

After reset ports BUSCTL, BE and CS are configured for external memory. They are available for the user as GPIO if the corresponding registers are set appropriately. All other ports default to GPIO after reset.

NOTE

In this table and throughout this document, a single signal within a group is designated without square brackets (i.e., A23), while designations for multiple signals within a group use brackets (i.e., A[23:21]) and is meant to include all signals within the two bracketed numbers when these numbers are separated by a colon.

NOTE

The primary functionality of a pin is not necessarily its default functionality. Pins that are muxed with GPIO default to their GPIO functionality.

Table 13-1. MCF5207/8 Signal Information and Muxing

Signal Name	GPIO	Alternate 1	Alternate 2	Dir. ¹	Voltage Domain	MCF5207 144 LQFP	MCF5207 144 MAPBGA	MCF5208 160 QFP	MCF5208 196 MAPBGA
Reset									
$\overline{\text{RESET}}^2$	—	—	—	I	EVDD	82	J10	90	J14
$\overline{\text{RSTOUT}}$	—	—	—	O	EVDD	74	M12	82	N14
Clock									
EXTAL	—	—	—	I	EVDD	78	K12	86	L14
XTAL	—	—	—	O	EVDD	80	J12	88	K14
FB_CLK	—	—	—	O	SDVDD	34	L1	40	N1

Table 13-1. MCF5207/8 Signal Information and Muxing (continued)

Signal Name	GPIO	Alternate 1	Alternate 2	Dir. ¹	Voltage Domain	MCF5207 144 LQFP	MCF5207 144 MAPBGA	MCF5208 160 QFP	MCF5208 196 MAPBGA
Mode Selection									
$\overline{\text{RCON}}^2$	—	—	—	I	EVDD	144	C4	160	C3
DRAMSEL	—	—	—	I	EVDD	79	H10	87	K11
FlexBus									
A[23:22]	—	$\overline{\text{FB_CS}}[5:4]$	—	O	SDVDD	118, 117	B9, A10	126, 125	B11, A11
A[21:16]	—	—	—	O	SDVDD	116–114, 112, 108, 107	C9, A11, B10, A12, C11, B11	124, 123, 122, 120, 116, 115	B12, A12, A13, B13, B14, C13
A[15:14]	—	SD_BA[1:0] ³	—	O	SDVDD	106, 105	B12, C12	114, 113	C14, D12
A[13:11]	—	SD_A[13:11] ³	—	O	SDVDD	104–102	D11, E10, D12	112, 111, 110	D13, D14, E11
A10	—	—	—	O	SDVDD	101	C10	109	E12
A[9:0]	—	SD_A[9:0] ³	—	O	SDVDD	100–91	E11, D9, E12, F10, F11, E9, F12, G10, G12, F9	108–99	E13, E14, F11–F14, G11–G14
D[31:16]	—	SD_D[31:16] ⁴	—	I/O	SDVDD	21–28, 40–47	F1, F2, G1, G2, G4, G3, H1, H2, K3, L2, L3, K2, M3, J4, M4, K4	27–34, 46–53	J4–J1, K4–K1, M3, N3, M4, N4, P4, L5, M5, N5
D[15:0]	—	FB_D[31:16] ⁴	—	I/O	SDVDD	8–15, 51–58	B2, B1, C2, C1, D2, D1, E2, E1, L5, K5, L6, J6, M6, J7, L7, K7	16–23, 57–64	F3–F1, G4–G1, H1, N6, P6, L7, M7, N7, P7, N8, P8
$\overline{\text{BE/BWE}}[3:0]$	PBE[3:0]	$\overline{\text{SD_DQM}}[3:0]^3$	—	O	SDVDD	20, 48, 18, 50	F4, L4, E3, J5	26, 54, 24, 56	H2, P5, H4, M6
$\overline{\text{OE}}$	PBUSCTL3	—	—	O	SDVDD	60	J8	66	M8
$\overline{\text{TA}}^2$	PBUSCTL2	—	—	I	SDVDD	90	G11	98	H14
$\text{R}/\overline{\text{W}}$	PBUSCTL1	—	—	O	SDVDD	59	K6	65	L8
$\overline{\text{TS}}$	PBUSCTL0	$\overline{\text{DACK0}}$	—	O	SDVDD	4	B3	12	E3
Chip Selects									
$\overline{\text{FB_CS}}[3:2]$	PCS[3:2]	—	—	O	SDVDD	119, 120	D7, A9	—	C11, A10
$\overline{\text{FB_CS1}}$	PCS1	$\overline{\text{SD_CS1}}$	—	O	SDVDD	121	C8	127	B10

Table 13-1. MCF5207/8 Signal Information and Muxing (continued)

Signal Name	GPIO	Alternate 1	Alternate 2	Dir. ¹	Voltage Domain	MCF5207 144 LQFP	MCF5207 144 MAPBGA	MCF5208 160 QFP	MCF5208 196 MAPBGA
$\overline{\text{FB_CS0}}$	—	—	—	O	SDVDD	122	B8	128	C10
SDRAM Controller									
SD_A10	—	—	—	O	SDVDD	37	M1	43	N2
SD_CKE	—	—	—	O	SDVDD	6	C3	14	E1
SD_CLK	—	—	—	O	SDVDD	31	J1	37	L1
$\overline{\text{SD_CLK}}$	—	—	—	O	SDVDD	32	K1	38	M1
$\overline{\text{SD_CS0}}$	—	—	—	O	SDVDD	7	A1	15	F4
SD_DQS[3:2]	—	—	—	O	SDVDD	19, 49	F3, M5	25, 55	H3, L6
$\overline{\text{SD_SCAS}}$	—	—	—	O	SDVDD	38	M2	44	P2
$\overline{\text{SD_SRAS}}$	—	—	—	O	SDVDD	39	J2	45	P3
SD_SDR_DQS	—	—	—	O	SDVDD	29	H3	35	L3
$\overline{\text{SD_WE}}$	—	—	—	O	SDVDD	5	D3	13	E2
External Interrupts Port⁵									
$\overline{\text{IRQ7}}^2$	PIRQ7 ²	—	—	I	EVDD	134	A5	142	C7
$\overline{\text{IRQ4}}^2$	PIRQ4 ²	$\overline{\text{DREQ0}}^2$	—	I	EVDD	133	C6	141	D7
$\overline{\text{IRQ1}}^2$	PIRQ1 ²	—	—	I	EVDD	132	B6	140	D8
FEC									
FEC_MDC	PFECI2C3	I2C_SCL ²	U2TXD	O	EVDD	—	—	148	D6
FEC_MDIO	PFECI2C2	I2C_SDA ²	U2RXD	I/O	EVDD	—	—	147	C6
FEC_TXCLK	PFECH7	—	—	I	EVDD	—	—	157	B3
—	PFECH6	—	$\overline{\text{U1RTS}}$	O	EVDD	142	A2	—	—
FEC_TXEN	PFECH6	—	$\overline{\text{U1RTS}}$	O	EVDD	—	—	158	A2
FEC_TXD0	PFECH5	—	—	O	EVDD	—	—	3	B1
FEC_COL	PFECH4	—	—	I	EVDD	—	—	7	D3
FEC_RXCLK	PFECH3	—	—	I	EVDD	—	—	154	B4
FEC_RXDV	PFECH2	—	—	I	EVDD	—	—	153	A4
FEC_RXD0	PFECH1	—	—	I	EVDD	—	—	152	D5
FEC_CRS	PFECH0	—	—	I	EVDD	—	—	8	D2
FEC_TXD[3:1]	PFECI[7:5]	—	—	O	EVDD	—	—	6–4	C1, C2, B2
—	PFECI4	—	$\overline{\text{U0RTS}}$	O	EVDD	141	D5	—	—
FEC_TXER	PFECI4	—	$\overline{\text{U0RTS}}$	O	EVDD	—	—	156	A3

Table 13-1. MCF5207/8 Signal Information and Muxing (continued)

Signal Name	GPIO	Alternate 1	Alternate 2	Dir. ¹	Voltage Domain	MCF5207 144 LQFP	MCF5207 144 MAPBGA	MCF5208 160 QFP	MCF5208 196 MAPBGA
FEC_RXD[3:2]	PFECL[3:2]	—	—	I	EVDD	—	—	149–150	A5, B5
—	PFECL1	—	$\overline{U1CTS}$	I	EVDD	139	B4	—	—
FEC_RXD1	PFECL1	—	$\overline{U1CTS}$	I	EVDD	—	—	151	C5
—	PFECL0	—	$\overline{U0CTS}$	I	EVDD	140	E4	—	—
FEC_RXER	PFECL0	—	$\overline{U0CTS}$	I	EVDD	—	—	155	C4
Note: The MCF5207 does not contain an FEC module. However, the UART0 and UART1 control signals (as well as their GPIO signals) are available by setting the appropriate FEC GPIO port registers.									
I²C									
I2C_SDA ²	PFECI2C0 ²	U2RXD ²	—	I/O	EVDD	—	—	—	D1
I2C_SCL ²	PFECI2C1 ²	U2TXD ²	—	I/O	EVDD	—	—	—	E4
DMA									
$\overline{DACK0}$ and $\overline{DREQ0}$ do not have a dedicated bond pads. Please refer to the following pins for muxing: \overline{TS} and QSPI_CS2 for $\overline{DACK0}$, $\overline{IRQ4}$ and QSPI_DIN for $\overline{DREQ0}$.									
QSPI									
QSPI_CS2	PQSPI3	$\overline{DACK0}$	$\overline{U2RTS}$	O	EVDD	126	A8	132	D10
QSPI_CLK	PQSPI0	I2C_SCL ²	—	O	EVDD	127	C7	133	A9
QSPI_DOUT	PQSPI1	I2C_SDA ²	—	O	EVDD	128	A7	134	B9
QSPI_DIN	PQSPI2	$\overline{DREQ0}$ ²	$\overline{U2CTS}$	I	EVDD	129	B7	135	C9
Note: The QSPI_CS1 and QSPI_CS0 signals are available on the $\overline{U1CTS}$, $\overline{U1RTS}$, $\overline{U0CTS}$, or $\overline{U0RTS}$ pins for the 196 and 160-pin packages.									
UARTs									
$\overline{U1CTS}$	PUARTL7	DT1IN	QSPI_CS1	I	EVDD	—	—	136	D9
$\overline{U1RTS}$	PUARTL6	DT1OUT	QSPI_CS1	O	EVDD	—	—	137	C8
U1TXD	PUARTL5	—	—	O	EVDD	131	A6	139	A8
U1RXD	PUARTL4	—	—	I	EVDD	130	D6	138	B8
$\overline{U0CTS}$	PUARTL3	DT0IN	QSPI_CS0	I	EVDD	—	—	76	N12
$\overline{U0RTS}$	PUARTL2	DT0OUT	QSPI_CS0	O	EVDD	—	—	77	P12
U0TXD	PUARTL1	—	—	O	EVDD	71	L10	79	P13
U0RXD	PUARTL0	—	—	I	EVDD	70	M10	78	N13
Note: The UART2 signals are multiplexed on the DMA Timers, QSPI, FEC, and I2C pins. For the MCF5207 devices, the UART0 and UART1 control signals are multiplexed internally on the FEC signals.									

Table 13-1. MCF5207/8 Signal Information and Muxing (continued)

Signal Name	GPIO	Alternate 1	Alternate 2	Dir. ¹	Voltage Domain	MCF5207 144 LQFP	MCF5207 144 MAPBGA	MCF5208 160 QFP	MCF5208 196 MAPBGA
DMA Timers									
DT3IN	PTIMER3	DT3OUT	$\overline{U2CTS}$	I	EVDD	135	B5	143	B7
DT2IN	PTIMER2	DT2OUT	$\overline{U2RTS}$	I	EVDD	136	C5	144	A7
DT1IN	PTIMER1	DT1OUT	U2RXD	I	EVDD	137	A4	145	A6
DT0IN	PTIMER0	DT0OUT	U2TXD	I	EVDD	138	A3	146	B6
BDM/JTAG⁶									
JTAG_EN ⁷	—	—	—	I	EVDD	83	J11	91	J13
DSCLK	—	\overline{TRST}^2	—	I	EVDD	76	K11	84	L12
PSTCLK	—	TCLK ²	—	O	EVDD	64	M7	70	P9
\overline{BKPT}	—	TMS ²	—	I	EVDD	75	L12	83	M14
DSI	—	TDI ²	—	I	EVDD	77	H9	85	K12
DSO	—	TDO	—	O	EVDD	69	M9	75	M12
DDATA[3:0]	—	—	—	O	EVDD	—	K9, L9, M11, M8	—	P11, N11, M11, P10
PST[3:0]	—	—	—	O	EVDD	—	L11, L8, K10, K8	—	N10, M10, L10, L9
ALLPST	—	—	—	O	EVDD	67	—	73	—
Test									
TEST ⁷	—	—	—	I	EVDD	109	—	—	C12
PLL_TEST	—	—	—	I	EVDD	—	—	—	M13
Power Supplies									
EVDD	—	—	—	—	—	1, 33, 63, 66, 72, 81, 87, 125	E5–E6, F5, G8–G9, H7–H8	2, 9, 69, 72, 80, 89, 95, 131	E5–E7, F5, F6, G5, H10, J9, J10, K8–K10, K13, M9
IVDD	—	—	—	—	—	30, 68, 84, 113, 143	D4, D8, H4, H11, J9	36, 74, 92, 121, 159	J12, D4, D11, H11, L4, L11,
PLL_VDD	—	—	—	—	—	86	H12	94	H13

Table 13-1. MCF5207/8 Signal Information and Muxing (continued)

Signal Name	GPIO	Alternate 1	Alternate 2	Dir. ¹	Voltage Domain	MCF5207 144 LQFP	MCF5207 144 MAPBGA	MCF5208 160 QFP	MCF5208 196 MAPBGA
SD_VDD	—	—	—	—	—	3, 17, 35, 61, 89, 110, 123	E7–E8, F8, G5, H5–H6, J3	11, 39, 41, 67, 97, 118, 129	E8–E10, F9, F10, G10, H5, J5, J6, K5–K7, L2
VSS	—	—	—	—	—	2, 16, 36, 62, 65, 73, 88, 111, 124	D10, F6–F7, G6–G7	1, 10, 42, 68, 71, 81, 96, 117, 119, 130	A1, A14, F7–F8, G6–G9, H6–H9, J7–J8, L13, M2, N9, P1, P14
PLL_VSS	—	—	—	—	—	85	—	93	H12

¹ Refers to pin's primary function.

² Pull-up enabled internally on this signal for this mode.

³ The SDRAM functions of these signals are not programmable by the user. They are dynamically switched by the processor when accessing SDRAM memory space and are included here for completeness.

⁴ Primary functionality selected by asserting the DRAMSEL signal (SDR mode). Alternate functionality selected by negating the DRAMSEL signal (DDR mode). The GPIO module is not responsible for assigning these pins.

⁵ GPIO functionality is determined by the edge port module. The GPIO module is only responsible for assigning the alternate functions.

⁶ If JTAG_EN is asserted, these pins default to Alternate 1 (JTAG) functionality. The GPIO module is not responsible for assigning these pins.

⁷ Pull-down enabled internally on this signal for this mode.

Refer to the [Chapter 2, “Signal Descriptions,”](#) for more detailed descriptions of these pins and other pins not controlled by the ports module. The function of most of the pins (primary function, GPIO, etc.) is determined by the ports module pin assignment registers.

It should be noted from [Table 13-2](#) that there are several cases where a function is available on more than one pin. While it is possible to enable the function on more than one pin simultaneously, this type of programming should be avoided for input functions to prevent unexpected behavior. All multiple-pin functions are listed in [Table 13-2](#).

Table 13-2. Multiple-Pin Functions

Function	Direction	Associated Pins
$\overline{\text{DACK0}}$	I	QSPI_CS2, $\overline{\text{TS}}$
$\overline{\text{DREQ0}}$	I	$\overline{\text{IRQ4}}$, QSPI_DIN
I2C_SCL	I/O	I2C_SCL, QSPI_CLK, FEC_MDC
I2C_SDA	I/O	I2C_SDA, QSPI_DOUT, FEC_MDIO
$\overline{\text{U2CTS}}$	I	DT3IN, QSPI_DIN
$\overline{\text{U2RTS}}$	O	DT2IN, QSPI_CS2

Table 13-2. Multiple-Pin Functions (continued)

Function	Direction	Associated Pins
U2TXD	O	DT0IN, FEC_MDC, I2C_SCL
U2RXD	I	DT1IN, FEC_MDIO, I2C_SDA
DT0IN	I	DT0IN, $\overline{U0CTS}$
DT0OUT	O	DT0IN, $\overline{U0RTS}$
DT1IN	I	DT1IN, $\overline{U1CTS}$
DT1OUT	O	DT1IN, $\overline{U1RTS}$
QSPI_CS0	O	$\overline{U0CTS}$, $\overline{U0RTS}$
QSPI_CS1	O	$\overline{U1CTS}$, $\overline{U1RTS}$

13.3 Memory Map/Register Definition

Table 13-3 summarizes all the registers in the ports address space.

Table 13-3. GPIO Module Memory Map

Address	Register	Width (bits)	Access	Reset Value	Section/Page
Port Output Data Registers					
0xFC0A_4000	PODR_BUSCTL	8	R/W	0x0F	13.3.1/13-11
0xFC0A_4001	PODR_BE	8	R/W	0x0F	13.3.1/13-11
0xFC0A_4002	PODR_CS	8	R/W	0x0E	13.3.1/13-11
0xFC0A_4003	PODR_FECI2C	8	R/W	0x0F	13.3.1/13-11
0xFC0A_4004	PODR_QSPI	8	R/W	0x0F	13.3.1/13-11
0xFC0A_4005	PODR_TIMER	8	R/W	0x0F	13.3.1/13-11
0xFC0A_4006	PODR_UART	8	R/W	0xFF	13.3.1/13-11
0xFC0A_4007	PODR_FECH	8	R/W	0xFF	13.3.1/13-11
0xFC0A_4008	PODR_FECL	8	R/W	0xFF	13.3.1/13-11
Port Data Direction Registers					
0xFC0A_400C	PDDR_BUSCTL	8	R/W	0x00	13.3.2/13-12
0xFC0A_400D	PDDR_BE	8	R/W	0x00	13.3.2/13-12
0xFC0A_400E	PDDR_CS	8	R/W	0x00	13.3.2/13-12
0xFC0A_400F	PDDR_FECI2C	8	R/W	0x00	13.3.2/13-12
0xFC0A_4010	PDDR_QSPI	8	R/W	0x00	13.3.2/13-12
0xFC0A_4011	PDDR_TIMER	8	R/W	0x00	13.3.2/13-12
0xFC0A_4012	PDDR_UART	8	R/W	0x00	13.3.2/13-12

Table 13-3. GPIO Module Memory Map (continued)

Address	Register	Width (bits)	Access	Reset Value	Section/Page
0xFC0A_4013	PDDR_FECH	8	R/W	0x00	13.3.2/13-12
0xFC0A_4014	PDDR_FECL	8	R/W	0x00	13.3.2/13-12
Port Pin Data/Set Data Registers					
0xFC0A_401A	PPDSR_CS	8	R/W	See Section	13.3.3/13-13
0xFC0A_401B	PPDSR_FECI2C	8	R/W	See Section	13.3.3/13-13
0xFC0A_401C	PPDSR_QSPI	8	R/W	See Section	13.3.3/13-13
0xFC0A_401D	PPDSR_TIMER	8	R/W	See Section	13.3.3/13-13
0xFC0A_401E	PPDSR_UART	8	R/W	See Section	13.3.3/13-13
0xFC0A_401F	PPDSR_FECH	8	R/W	See Section	13.3.3/13-13
0xFC0A_4020	PPDSR_FECL	8	R/W	See Section	13.3.3/13-13
Port Clear Output Data Registers					
0xFC0A_4024	PCLRR_BUSCTL	8	W	0x00	13.3.4/13-15
0xFC0A_4025	PCLRR_BE	8	W	0x00	13.3.4/13-15
0xFC0A_4026	PCLRR_CS	8	W	0x00	13.3.4/13-15
0xFC0A_4027	PCLRR_FECI2C	8	W	0x00	13.3.4/13-15
0xFC0A_4028	PCLRR_QSPI	8	W	0x00	13.3.4/13-15
0xFC0A_4029	PCLRR_TIMER	8	W	0x00	13.3.4/13-15
0xFC0A_402A	PCLRR_UART	8	W	0x00	13.3.4/13-15
0xFC0A_402B	PCLRR_FECH	8	W	0x00	13.3.4/13-15
0xFC0A_402C	PCLRR_FECL	8	W	0x00	13.3.4/13-15
Pin Assignment Registers					
0xFC0A_4030	PAR_BUSCTL	8	R/W	0x1F	13.3.5.1/13-16
0xFC0A_4031	PAR_BE	8	R/W	0x0F	13.3.5.2/13-16
0xFC0A_4032	PAR_CS	8	R/W	0x0F	13.3.5.3/13-17
0xFC0A_4033	PAR_FECI2C	8	R/W	0x00	13.3.5.4/13-18
0xFC0A_4034	PAR_QSPI	8	R/W	0x00	13.3.5.5/13-18
0xFC0A_4035	PAR_TIMER	8	R/W	0x00	13.3.5.6/13-19
0xFC0A_4036	PAR_UART	8	R/W	0x0000	13.3.5.7/13-20
0xFC0A_4038	PAR_FEC	8	R/W	0x00	13.3.5.8/13-21
0xFC0A_4039	PAR_IRQ	8	R/W	0x00	13.3.5.9/13-23
Mode Select Control Registers					

Table 13-3. GPIO Module Memory Map (continued)

Address	Register	Width (bits)	Access	Reset Value	Section/Page
0xFC0A_403A	MSCR_FLEXBUS	8	R/W	0xFF	13.3.6/13-23
0xFC0A_403B	MSCR_SDRAM	8	R/W	0x3F	13.3.7/13-24
Drive Strength Control Registers					
0xFC0A_403C	DSCR_I2C	8	R/W	See Section	13.3.8.1/13-25
0xFC0A_403D	DSCR_MISC	8	R/W	See Section	13.3.8.2/13-25
0xFC0A_403E	DSCR_FEC	8	R/W	See Section	13.3.8.3/13-26
0xFC0A_403F	DSCR_UART	8	R/W	See Section	13.3.8.4/13-27
0xFC0A_4040	DSCR_QSPI	8	R/W	See Section	13.3.8.5/13-27

13.3.1 Port Output Data Registers (PODR_x)

The PODR_x registers store the data to be driven on the corresponding port pins when the pins are configured for general purpose output. The PODR_x registers are each eight bits wide, but not all ports use all eight bits. The register definitions for all ports are shown in the below figures. The PODR_x registers are read/write. At reset, all implemented bits in the PODR_x registers are set. Reserved bits always remain cleared.

Reading a PODR_x register returns the current values in the register, not the port pin values. To set bits in a PODR_x register, set the PODR_x bits, or set the corresponding bits in the PPDSR_x register. To clear bits in a PODR_x register, clear the PODR_x bits, or clear the corresponding bits in the PCLRR_x register.

Address: 0xFC0A_4000 (PODR_BUSCTL)
 0xFC0A_4001 (PODR_BE)
 0xFC0A_4003 (PODR_FECI2C)
 0xFC0A_4004 (PODR_QSPI)
 0xFC0A_4005 (PODR_TIMER)

Access: User read/write

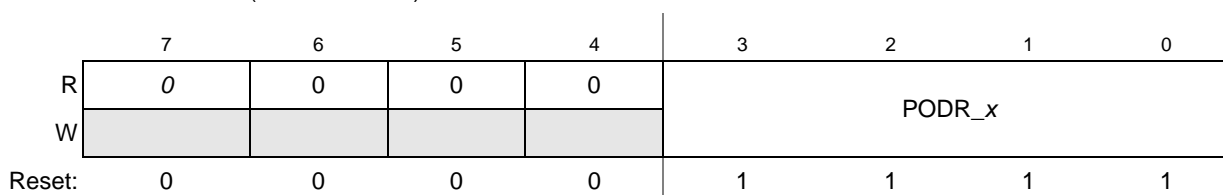


Figure 13-2. Port x Output Data Registers (PODR_x)

Address: 0xFC0A_4002 (PODR_CS)

Access: User read/write

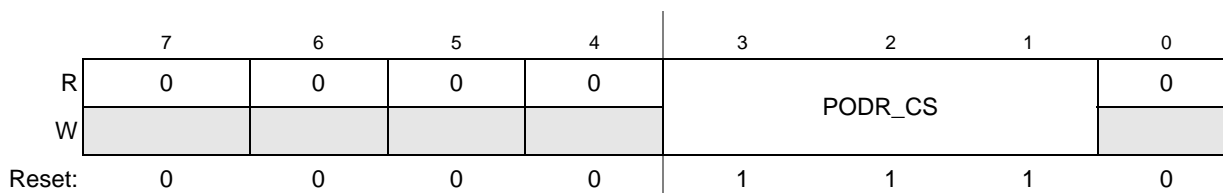


Figure 13-3. Port CS Output Data Register (PODR_CS)

Address: 0xFC0A_4006 (PODR_UART) Access: User read/write
 0xFC0A_4007 (PODR_FECH)
 0xFC0A_4008 (PODR_FECL)

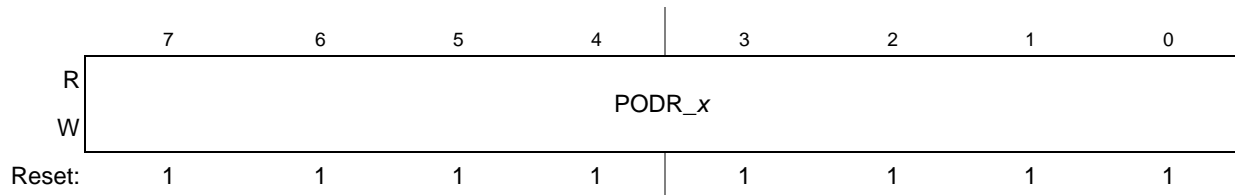


Figure 13-4. Port x Output Data Registers (PODR_x)

Table 13-4. PODR_x Field Descriptions

Field	Description
PODR_x	Port x output data bits. 0 Drives 0 when the port x pin is general purpose output 1 Drives 1 when the port x pin is general purpose output

Note: See above figures for bit field positions.

13.3.2 Port Data Direction Registers (PDDR_x)

The PDDRs control the direction of the port pin drivers when the pins are configured for GPIO. The PDDR_x registers are each eight bits wide, but not all ports use all eight bits. The register definitions for all ports are shown in the figures below.

The PDDRs are read/write. At reset, all bits in the PDDRs are cleared. Setting any bit in a PDDR_x register configures the corresponding port pin as an output. Clearing any bit in a PDDR_x register configures the corresponding pin as an input.

Address: 0xFC0A_400C (PDDR_BUSCTL) Access: User read/write
 0xFC0A_400D (PDDR_BE)
 0xFC0A_400F (PDDR_FECI2C)
 0xFC0A_4010 (PDDR_QSPI)
 0xFC0A_4011 (PDDR_TIMER)

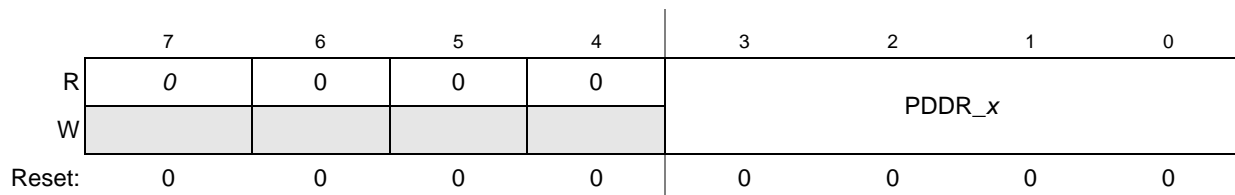


Figure 13-5. Port Data Direction Registers (PDDR_x)

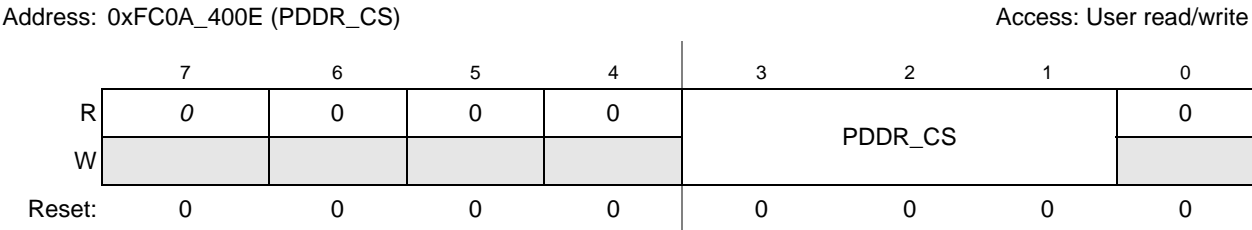


Figure 13-6. Port CS Data Direction Register (PDDR_CS)

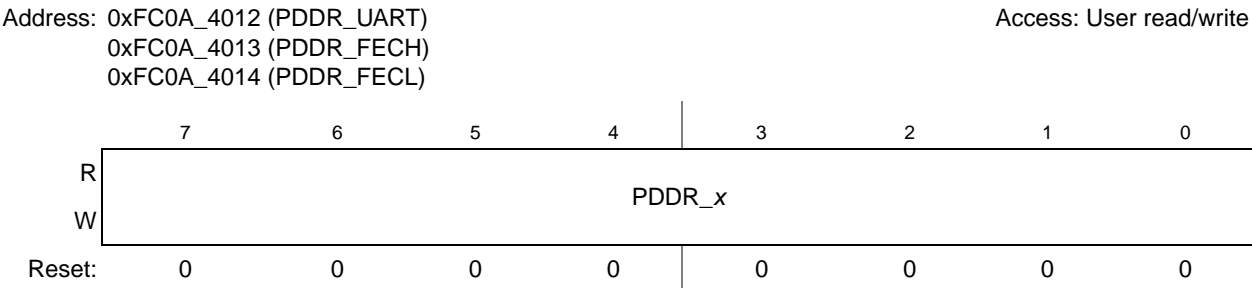


Figure 13-7. Port Data Direction Registers (PDDR_x)

Table 13-5. PDDR_x Field Descriptions

Field	Description
PDDR_x	Port x output data direction bits. 1 Port x pin configured as output 0 Port x pin configured as input

Note: See above figures for bit field positions.

13.3.3 Port Pin Data/Set Data Registers (PPDSDR_x)

The PPDSDR registers reflect the current pin states and control the setting of output pins when the pin is configured for GPIO. The PPDSDR_x registers are each eight bits wide, but not all ports use all eight bits. The register definitions for all ports are shown in the below figures.

The PPDSDR_x registers are read/write. At reset, the bits in the PPDSDR_x registers are set to the current pin states. Reading a PPDSDR_x register returns the current state of the port x pins. Setting a PPDSDR_x register sets the corresponding bits in the PODR_x register. Writing 0s has no effect.

Address: 0xFC0A_4018 (PPDSDR_BUSCTL) Access: User read/write
 0xFC0A_4019 (PPDSDR_BE)
 0xFC0A_401B (PPDSDR_FECI2C)
 0xFC0A_401C (PPDSDR_QSPI)
 0xFC0A_401D (PPDSDR_TIMER)

	7	6	5	4	3	2	1	0
R	0	0	0	0	PPDR_x			
W					PSDR_x			
Reset:	0	0	0	0	[Px3]	[Px2]	[Px1]	[Px0]

Figure 13-8. Port Pin Data/Set Data Registers (PPDSDR_x)

Address: 0xFC0A_401A (PPDSDR_CS) Access: User read/write

	7	6	5	4	3	2	1	0
R	0	0	0	0	PPDR_CS			0
W					PSDR_CS			
Reset:	0	0	0	0	[PCS3]	[PCS2]	[PCS1]	0

Figure 13-9. Port CS Pin Data/Set Data Register (PPDSDR_CS)

Address: 0xFC0A_401E (PPDSDR_UART) Access: User read/write
 0xFC0A_401F (PPDSDR_FECH)
 0xFC0A_4020 (PPDSDR_FECL)

	7	6	5	4	3	2	1	0
R	PPDR_x							
W	PSDR_x							
Reset:	[Px7]	[Px6]	[Px5]	[Px4]	[Px3]	[Px2]	[Px1]	[Px0]

Figure 13-10. Port Pin Data/Set Data Registers (PPDSDR_x)

Table 13-6. PPDSDR_x Field Descriptions

Field	Description
PPDR_x (read)	Port x pin data bits. 0 Port x pin state is 0 1 Port x pin state is 1
PSDR_x (write)	Port x set data bits. 0 No effect. 1 Set corresponding PODR_x bit.

Note: See above figures for bit field positions.

13.3.4 Port Clear Output Data Registers (PCLRR_x)

Clearing a PCLRR_x register clears the corresponding bits in the PODR_x register. Setting it has no effect. Reading the PCLRR_x register returns 0s. The PCLRR_x registers are each eight bits wide, but not all ports use all eight bits. The register definitions for all ports are shown in the figures below.

Address: 0xFC0A_4024 (PCLRR_BUSCTL)
 0xFC0A_4025 (PCLRR_BE)
 0xFC0A_4027 (PCLRR_FECI2C)
 0xFC0A_4028 (PCLRR_QSPI)
 0xFC0A_4029 (PCLRR_TIMER)

Access: User write-only

	7	6	5	4	3	2	1	0
R	0	0	0	0	0	0	0	0
W					PCLRR_x			
Reset:	0	0	0	0	0	0	0	0

Figure 13-11. Port Clear Output Data Registers (PCLRR_x)

Address: 0xFC0A_4026 (PCLRR_CS)

Access: User write-only

	7	6	5	4	3	2	1	0
R	0	0	0	0	0	0	0	0
W					PCLRR_CS			
Reset:	0	0	0	0	0	0	0	0

Figure 13-12. Port CS Clear Output Data Register (PCLRR_CS)

Address: 0xFC0A_402A (PCLRR_UART)
 0xFC0A_402B (PCLRR_FECH)
 0xFC0A_402C (PCLRR_FECL)

Access: User write-only

	7	6	5	4	3	2	1	0
R	0	0	0	0	0	0	0	0
W	PCLRR_x							
Reset:	0	0	0	0	0	0	0	0

Figure 13-13. Port Clear Output Data Registers (PCLRR_x)

Table 13-7. PCLRR_x Field Descriptions

Field	Description
PCLRR_x	Port x clear data bits. 0 Clears corresponding PODR_x bit 1 No effect

Note: See above figures for bit field positions.

13.3.5 Pin Assignment Registers (PAR_x)

The pin assignment registers control which functions are currently active on the external pins. All pin assignment registers are read/write.

13.3.5.1 External Bus Control Pin Assignment Register (PAR_BUSCTL)

The PAR_BUSCTL register controls the functions of the external bus control signal pins.

Address: 0xFC0A_4030 (PAR_BUSCTL)

Access: User read/write

	7	6	5	4	3	2	1	0
R	0	0	0	PAR_OE	PAR_TA	PAR_RWB	PAR_TS	
W								
Reset:	0	0	0	1	1	1	1	1

Figure 13-14. External Bus Control Pin Assignment Register (PAR_BUSCTL)

Table 13-8. PAR_BUSCTL Field Descriptions

Field	Description
7–5	Reserved, should be cleared.
4 PAR_OE	0 \overline{OE} pin configured for GPIO 1 \overline{OE} pin configured for external bus \overline{OE} function
3 PAR_TA	0 \overline{TA} pin configured for GPIO 1 \overline{TA} pin configured for external bus \overline{TA} function
2 PAR_RWB	0 R/\overline{W} pin configured for GPIO 1 R/\overline{W} pin configured for external bus read/write function
1–0 PAR_TS	0x \overline{TS} pin configured for GPIO 10 \overline{TS} pin configured for DMA acknowledge 0 function 11 \overline{TS} pin configured for external bus \overline{TS} function

13.3.5.2 Byte Enable Pin Assignment Register (PAR_BE)

The PAR_BE register controls the functions of the byte enable pins.

Address: 0xFC0A_4031 (PAR_BE)

Access: User read/write

	7	6	5	4	3	2	1	0
R	0	0	0	0	PAR_BE			
W								
Reset:	0	0	0	0	1	1	1	1

Figure 13-15. Byte Enable Pin Assignment Register (PAR_BE)

Table 13-9. PAR_BE Field Descriptions

Field	Description
7–4	Reserved, should be cleared.
3–0 PAR_BE	$\overline{\text{BE}}/\text{BWE}[3:0]$ pin assignment. The PAR_BE[3:0] bits configure the $\overline{\text{BE}}/\text{BWE}[3:0]$ pins for their primary function or GPIO. 0 $\overline{\text{BE}}/\text{BWE}[3:0]$ pin configured for GPIO 1 $\overline{\text{BE}}/\text{BWE}[3:0]$ pin configured for $\overline{\text{BE}}/\text{BWE}[3:0]$ function Refer to Chapter 9, “Chip Configuration Module (CCM)” for more information on reset configuration.

13.3.5.3 Chip Select Pin Assignment Register (PAR_CS)

The PAR_CS register controls the functions of the FlexBus chip select pins.

Address: 0xFC0A_4032 (PAR_CS)

Access: User read/write

	7	6	5	4	3	2	1	0
R	0	0	0	0	PAR_CS3	PAR_CS2	PAR_CS1	
W								
Reset:	0	0	0	0	1	1	1	1

Figure 13-16. Chip Select Pin Assignment Register (PAR_CS)**Table 13-10. PAR_CS Field Descriptions**

Field	Description
7–4	Reserved, should be cleared.
3 PAR_CS3	$\overline{\text{FB_CS3}}$ pin assignment. 0 $\overline{\text{FB_CS3}}$ pin configured for GPIO 1 $\overline{\text{FB_CS3}}$ pin configured for FlexBus $\overline{\text{FB_CS3}}$ function
2 PAR_CS2	$\overline{\text{FB_CS2}}$ pin assignment. 0 $\overline{\text{FB_CS2}}$ pin configured for GPIO 1 $\overline{\text{FB_CS2}}$ pin configured for FlexBus $\overline{\text{FB_CS2}}$ function
1–0 PAR_CS1	$\overline{\text{FB_CS1}}$ pin assignment. 0x $\overline{\text{FB_CS1}}$ pin configured for GPIO 10 $\overline{\text{FB_CS1}}$ pin configured for $\overline{\text{SD_CS1}}$ function 11 $\overline{\text{FB_CS1}}$ pin configured for FlexBus $\overline{\text{FB_CS1}}$ function

13.3.5.4 FEC/I2C Pin Assignment Register (PAR_FECI2C)

The PAR_FECI2C register controls the functions of the I²C and some of the FEC pins.

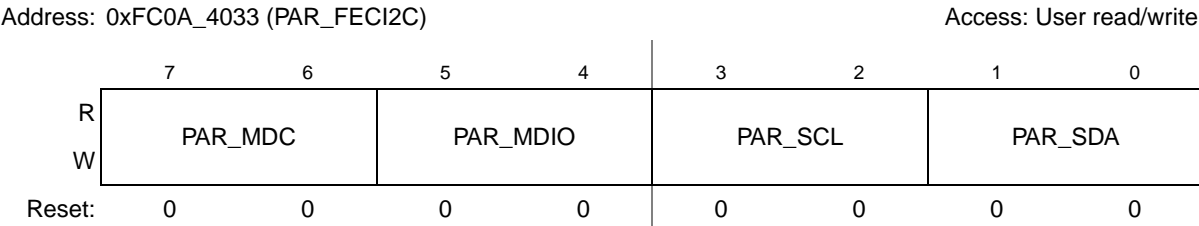


Figure 13-17. FEC/I2C Pin Assignment (PAR_FECI2C)

Table 13-11. PAR_FECI2C Field Descriptions

Field	Description																									
7–6 PAR_MDC 5–4 PAR_MDIO 3–2 PAR_SCL 1–0 PAR_SDA	<p>FEC & I²C pin assignment. These bit fields configure the FEC_MDC, FEC_MDIO, I2C_SCL, and I2C_SDA pins for one of their primary functions or GPIO.</p> <table><tr><th></th><th>PAR_MDC</th><th>PAR_MDIO</th><th>PAR_SCL</th><th>PAR_SDA</th></tr><tr><td>00</td><td>GPIO</td><td>GPIO</td><td>GPIO</td><td>GPIO</td></tr><tr><td>01</td><td>U2TXD</td><td>U2RXD</td><td>U2TXD</td><td>U2RXD</td></tr><tr><td>10</td><td>I2C_SCL</td><td>I2C_SDA</td><td>GPIO</td><td>GPIO</td></tr><tr><td>11</td><td>FEC_MDC</td><td>FEC_MDIO</td><td>I2C_SCL</td><td>I2C_SDA</td></tr></table>		PAR_MDC	PAR_MDIO	PAR_SCL	PAR_SDA	00	GPIO	GPIO	GPIO	GPIO	01	U2TXD	U2RXD	U2TXD	U2RXD	10	I2C_SCL	I2C_SDA	GPIO	GPIO	11	FEC_MDC	FEC_MDIO	I2C_SCL	I2C_SDA
	PAR_MDC	PAR_MDIO	PAR_SCL	PAR_SDA																						
00	GPIO	GPIO	GPIO	GPIO																						
01	U2TXD	U2RXD	U2TXD	U2RXD																						
10	I2C_SCL	I2C_SDA	GPIO	GPIO																						
11	FEC_MDC	FEC_MDIO	I2C_SCL	I2C_SDA																						

13.3.5.5 QSPI Pin Assignment Register (PAR_QSPI)

The PAR_QSPI register controls the functions of the QSPI pins.

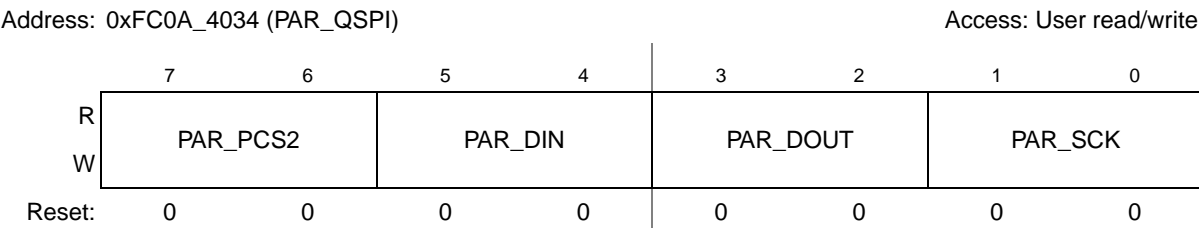


Figure 13-18. QSPI Pin Assignment (PAR_QSPI)

Table 13-12. PAR_QSPI Field Descriptions

Field	Description																									
7–6 PAR_PCS2 5–4 PAR_DIN 3–2 PAR_DOUT 1–0 PAR_SCK	QSPI pin assignment. These bit fields configure the QSPI pins for one of their primary functions or GPIO. <table><tr><th></th><th>PAR_PCS2</th><th>PAR_DIN</th><th>PAR_DOUT</th><th>PAR_SCK</th></tr><tr><td>00</td><td>GPIO</td><td>GPIO</td><td>GPIO</td><td>GPIO</td></tr><tr><td>01</td><td>U2RTS</td><td>U2CTS</td><td>GPIO</td><td>GPIO</td></tr><tr><td>10</td><td>DACK0</td><td>DREQ0</td><td>I2C_SDA</td><td>I2C_SCL</td></tr><tr><td>11</td><td>QSPI_PCS2</td><td>QSPI_DIN</td><td>QSPI_DOUT</td><td>QSPI_SCK</td></tr></table>		PAR_PCS2	PAR_DIN	PAR_DOUT	PAR_SCK	00	GPIO	GPIO	GPIO	GPIO	01	U2RTS	U2CTS	GPIO	GPIO	10	DACK0	DREQ0	I2C_SDA	I2C_SCL	11	QSPI_PCS2	QSPI_DIN	QSPI_DOUT	QSPI_SCK
	PAR_PCS2	PAR_DIN	PAR_DOUT	PAR_SCK																						
00	GPIO	GPIO	GPIO	GPIO																						
01	U2RTS	U2CTS	GPIO	GPIO																						
10	DACK0	DREQ0	I2C_SDA	I2C_SCL																						
11	QSPI_PCS2	QSPI_DIN	QSPI_DOUT	QSPI_SCK																						

13.3.5.6 Timer Pin Assignment Registers (PAR_TIMER)

The PAR_TIMER register controls the functions of the DMA timer pins.

Address: 0xFC0A_4035 (PAR_TIMER)

Access: User read/write

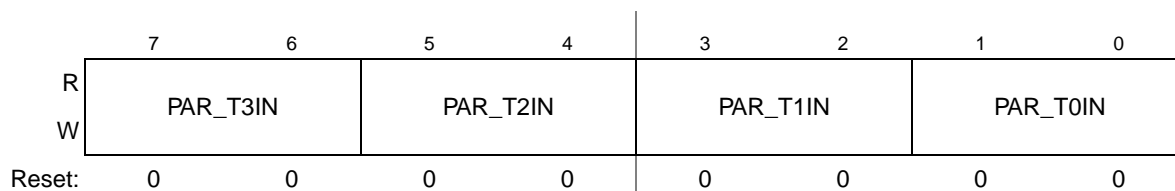


Figure 13-19. Timer Pin Assignment (PAR_TIMER)

Table 13-13. PAR_TIMER Field Descriptions

Field	Description																									
7–6 PAR_T3IN 5–4 PAR_T2IN 3–2 PAR_T1IN 1–0 PAR_T0IN	DMA Timer pin assignment. These bit fields configure the DMA Timer pins for one of their primary functions or GPIO <table><tr><td></td><td>PAR_T3IN</td><td>PAR_T2IN</td><td>PAR_T1IN</td><td>PAR_T0IN</td></tr><tr><td>00</td><td>GPIO</td><td>GPIO</td><td>GPIO</td><td>GPIO</td></tr><tr><td>01</td><td>$\overline{U2CTS}$</td><td>$\overline{U2RTS}$</td><td>U2RXD</td><td>U2TXD</td></tr><tr><td>10</td><td>T3OUT</td><td>T2OUT</td><td>T1OUT</td><td>T0OUT</td></tr><tr><td>11</td><td>T3IN</td><td>T2IN</td><td>T1IN</td><td>T0IN</td></tr></table>		PAR_T3IN	PAR_T2IN	PAR_T1IN	PAR_T0IN	00	GPIO	GPIO	GPIO	GPIO	01	$\overline{U2CTS}$	$\overline{U2RTS}$	U2RXD	U2TXD	10	T3OUT	T2OUT	T1OUT	T0OUT	11	T3IN	T2IN	T1IN	T0IN
	PAR_T3IN	PAR_T2IN	PAR_T1IN	PAR_T0IN																						
00	GPIO	GPIO	GPIO	GPIO																						
01	$\overline{U2CTS}$	$\overline{U2RTS}$	U2RXD	U2TXD																						
10	T3OUT	T2OUT	T1OUT	T0OUT																						
11	T3IN	T2IN	T1IN	T0IN																						

13.3.5.7 UART Pin Assignment Register (PAR_UART)

The PAR_UART register controls the functions of the UART pins.

Address: 0xFC0A_4036 (PAR_UART)

Access: User read/write

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	0	0	0	0	PAR_U1CTS		PAR_U1RTS		PAR_U1TXD	PAR_U1RXD	PAR_U0CTS		PAR_U0RTS		PAR_U0TXD	PAR_U0RXD
W																
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Figure 13-20. UART Pin Assignment (PAR_UART)

Table 13-14. PAR_UART Field Descriptions

Field	Description															
15–12	Reserved, should be cleared.															
11–10 PAR_U1CTS 9–8 PAR_U1RTS 7–6 PAR_U1RXD 5–4 PAR_U1TXD	UART1 control pin assignment. These bit fields configure the UART1 control pins for one of their primary functions or GPIO. <table><tr><td></td><td>PAR_U1CTS</td><td>PAR_U1RTS</td></tr><tr><td>00</td><td>GPIO</td><td>GPIO</td></tr><tr><td>01</td><td>QSPI_PCS1</td><td>QSPI_PCS1</td></tr><tr><td>10</td><td>T1IN</td><td>T1OUT</td></tr><tr><td>11</td><td>$\overline{\text{U1CTS}}$</td><td>$\overline{\text{U1RTS}}$</td></tr></table>		PAR_U1CTS	PAR_U1RTS	00	GPIO	GPIO	01	QSPI_PCS1	QSPI_PCS1	10	T1IN	T1OUT	11	$\overline{\text{U1CTS}}$	$\overline{\text{U1RTS}}$
	PAR_U1CTS	PAR_U1RTS														
00	GPIO	GPIO														
01	QSPI_PCS1	QSPI_PCS1														
10	T1IN	T1OUT														
11	$\overline{\text{U1CTS}}$	$\overline{\text{U1RTS}}$														
7 PAR_U1TXD	U1TXD pin assignment. 0 U1TXD pin configured for GPIO 1 U1TXD pin configured for UART1 TXD function															
6 PAR_U1RXD	U1RXD pin assignment. 0 U1RXD pin configured for GPIO 1 U1RXD pin configured for UART1 RXD function															
5–4 PAR_U0CTS 3–2 PAR_U0RTS	UART0 control pin assignment. These bit fields configure the UART0 control pins for one of their primary functions or GPIO. <table><tr><td></td><td>PAR_U0CTS</td><td>PAR_U0RTS</td></tr><tr><td>00</td><td>GPIO</td><td>GPIO</td></tr><tr><td>01</td><td>QSPI_PCS0</td><td>QSPI_PCS0</td></tr><tr><td>10</td><td>T0IN</td><td>T0OUT</td></tr><tr><td>11</td><td>$\overline{\text{U0CTS}}$</td><td>$\overline{\text{U0RTS}}$</td></tr></table>		PAR_U0CTS	PAR_U0RTS	00	GPIO	GPIO	01	QSPI_PCS0	QSPI_PCS0	10	T0IN	T0OUT	11	$\overline{\text{U0CTS}}$	$\overline{\text{U0RTS}}$
	PAR_U0CTS	PAR_U0RTS														
00	GPIO	GPIO														
01	QSPI_PCS0	QSPI_PCS0														
10	T0IN	T0OUT														
11	$\overline{\text{U0CTS}}$	$\overline{\text{U0RTS}}$														

Table 13-14. PAR_UART Field Descriptions (continued)

Field	Description
1 PAR_U0TXD	U0TXD pin assignment. 0 U0TXD pin configured for GPIO 1 U0TXD pin configured for UART0 TXD function
0 PAR_U0RXD	U0RXD pin assignment. 0 U0RXD pin configured for GPIO 1 U0RXD pin configured for UART0 RXD function

13.3.5.8 FEC Pin Assignment Register (PAR_FEC)

The PAR_FEC register controls the functions of the FEC pins.

Address: 0xFC0A_4038 (PAR_FEC)

Access: User read/write

	7	6	5	4	3	2	1	0
R	0	0	0	0	PAR_FEC_7W		PAR_FEC_MII	
W								
Reset:	0	0	0	0	0	0	0	0

Figure 13-21. FEC Pin Assignment (PAR_FEC)

Table 13-15. PAR_FEC Field Descriptions

Field	Description
7–4	Reserved, should be cleared.

Table 13-15. PAR_FEC Field Descriptions (continued)

Field	Description																																																							
3–2 PAR_FEC_7W	<p>FEC 7-wire pin assignment. These bit fields configure the FEC_COL, FEC_RXCLK, FEC_RXDV, FEC_RXD0, FEC_TXCLK, FEC_TXD0, and FEC_TXEN pins for one of their primary functions or GPIO.</p> <table><tr><th></th><th>FEC_COL</th><th>FEC_RXCLK</th><th>FEC_RXDV</th><th>FEC_RXD0</th><th>FEC_TXCLK</th><th>FEC_TXD0</th><th>FEC_TXEN</th></tr><tr><td>00</td><td>GPIO</td><td>GPIO</td><td>GPIO</td><td>GPIO</td><td>GPIO</td><td>GPIO</td><td>GPIO</td></tr><tr><td>01</td><td>GPIO</td><td>GPIO</td><td>GPIO</td><td>GPIO</td><td>GPIO</td><td>GPIO</td><td>U1RTS</td></tr><tr><td>10</td><td>GPIO</td><td>GPIO</td><td>GPIO</td><td>GPIO</td><td>GPIO</td><td>GPIO</td><td>GPIO</td></tr><tr><td>11</td><td>FEC_COL</td><td>FEC_RXCLK</td><td>FEC_RXDV</td><td>FEC_RXD0</td><td>FEC_TXCLK</td><td>FEC_TXD0</td><td>FEC_TXEN</td></tr></table> <p>Note: The MCF5207 devices do not contain an FEC module. However, the U1RTS signal can be selected by the appropriate setting in PAR_FEC_7W. See Table 13-1 for the location of this pin on the device.</p>		FEC_COL	FEC_RXCLK	FEC_RXDV	FEC_RXD0	FEC_TXCLK	FEC_TXD0	FEC_TXEN	00	GPIO	GPIO	GPIO	GPIO	GPIO	GPIO	GPIO	01	GPIO	GPIO	GPIO	GPIO	GPIO	GPIO	U1RTS	10	GPIO	GPIO	GPIO	GPIO	GPIO	GPIO	GPIO	11	FEC_COL	FEC_RXCLK	FEC_RXDV	FEC_RXD0	FEC_TXCLK	FEC_TXD0	FEC_TXEN															
	FEC_COL	FEC_RXCLK	FEC_RXDV	FEC_RXD0	FEC_TXCLK	FEC_TXD0	FEC_TXEN																																																	
00	GPIO	GPIO	GPIO	GPIO	GPIO	GPIO	GPIO																																																	
01	GPIO	GPIO	GPIO	GPIO	GPIO	GPIO	U1RTS																																																	
10	GPIO	GPIO	GPIO	GPIO	GPIO	GPIO	GPIO																																																	
11	FEC_COL	FEC_RXCLK	FEC_RXDV	FEC_RXD0	FEC_TXCLK	FEC_TXD0	FEC_TXEN																																																	
1–0 PAR_FEC_MII	<p>FEC MII pin assignment. These bit fields configure the FEC_CRS, FEC_RXD3, FEC_RXD2, FEC_RXD1, FEC_RXER, FEC_TXD3, FEC_TXD2, FEC_TXD1 and FEC_TXER pins for one of their primary functions or GPIO.</p> <table><tr><th></th><th>FEC_RXD3</th><th>FEC_RXD2</th><th>FEC_RXD1</th><th>FEC_RXER</th><th>FEC_CRS</th></tr><tr><td>00</td><td>GPIO</td><td>GPIO</td><td>GPIO</td><td>GPIO</td><td>GPIO</td></tr><tr><td>01</td><td>GPIO</td><td>GPIO</td><td>U1CTS</td><td>U0CTS</td><td>GPIO</td></tr><tr><td>10</td><td>GPIO</td><td>GPIO</td><td>GPIO</td><td>GPIO</td><td>GPIO</td></tr><tr><td>11</td><td>FEC_RXD3</td><td>FEC_RXD2</td><td>FEC_RXD1</td><td>FEC_RXER</td><td>FEC_CRS</td></tr></table> <table><tr><th></th><th>FEC_TXD3</th><th>FEC_TXD2</th><th>FEC_TXD1</th><th>FEC_TXER</th></tr><tr><td>00</td><td>GPIO</td><td>GPIO</td><td>GPIO</td><td>GPIO</td></tr><tr><td>01</td><td>GPIO</td><td>GPIO</td><td>GPIO</td><td>U0RTS</td></tr><tr><td>10</td><td>GPIO</td><td>GPIO</td><td>GPIO</td><td>GPIO</td></tr><tr><td>11</td><td>FEC_TXD3</td><td>FEC_TXD2</td><td>FEC_TXD1</td><td>FEC_TXER</td></tr></table> <p>Note: The MCF5207 devices do not contain an FEC module. However, the U0RTS, U0CTS, and U1CTS signals can be selected by the appropriate setting in PAR_FEC_MII. See Table 13-1 for the location of these pins on the device.</p>		FEC_RXD3	FEC_RXD2	FEC_RXD1	FEC_RXER	FEC_CRS	00	GPIO	GPIO	GPIO	GPIO	GPIO	01	GPIO	GPIO	U1CTS	U0CTS	GPIO	10	GPIO	GPIO	GPIO	GPIO	GPIO	11	FEC_RXD3	FEC_RXD2	FEC_RXD1	FEC_RXER	FEC_CRS		FEC_TXD3	FEC_TXD2	FEC_TXD1	FEC_TXER	00	GPIO	GPIO	GPIO	GPIO	01	GPIO	GPIO	GPIO	U0RTS	10	GPIO	GPIO	GPIO	GPIO	11	FEC_TXD3	FEC_TXD2	FEC_TXD1	FEC_TXER
	FEC_RXD3	FEC_RXD2	FEC_RXD1	FEC_RXER	FEC_CRS																																																			
00	GPIO	GPIO	GPIO	GPIO	GPIO																																																			
01	GPIO	GPIO	U1CTS	U0CTS	GPIO																																																			
10	GPIO	GPIO	GPIO	GPIO	GPIO																																																			
11	FEC_RXD3	FEC_RXD2	FEC_RXD1	FEC_RXER	FEC_CRS																																																			
	FEC_TXD3	FEC_TXD2	FEC_TXD1	FEC_TXER																																																				
00	GPIO	GPIO	GPIO	GPIO																																																				
01	GPIO	GPIO	GPIO	U0RTS																																																				
10	GPIO	GPIO	GPIO	GPIO																																																				
11	FEC_TXD3	FEC_TXD2	FEC_TXD1	FEC_TXER																																																				

13.3.5.9 IRQ Pin Assignment Register (PAR_IRQ)

The PAR_IRQ register controls the functions of the $\overline{\text{IRQ4}}$ pin.

Address: 0xFC0A_4039 (PAR_IRQ)

Access: User read/write

	7	6	5	4	3	2	1	0
R	0	0	0	0	0	0	0	PAR_IRQ4
W								
Reset:	0	0	0	0	0	0	0	0

Figure 13-22. IRQ Pin Assignment (PAR_IRQ)

Table 13-16. PAR_IRQ Field Descriptions

Field	Description
7–1	Reserved, should be cleared.
0 PAR_IRQ4	$\overline{\text{IRQ4}}$ pin assignment. 0 $\overline{\text{IRQ4}}$ pin configured for $\overline{\text{IRQ4}}$ function (if IRQ4 is enabled in the Edge Port module) or GPIO (if IRQ4 is disabled in the Edge Port module). 1 $\overline{\text{IRQ4}}$ pin configured for $\overline{\text{DREQ0}}$ function.

13.3.6 FlexBus Mode Select Control Register (MSCR_FLEXBUS)

The MSCR_FLEXBUS register controls the output mode selects of the following FlexBus pins: FB_A[23:0], D[31:0], $\overline{\text{BE/BWE}}$ [3:0], $\overline{\text{OE}}$, R/ $\overline{\text{W}}$, FB_CS[5:0], $\overline{\text{TA}}$ and $\overline{\text{TS}}$.

Address: 0xFC0A_403A (MSCR_FLEXBUS)

Access: User read/write

	7	6	5	4	3	2	1	0
R	MSCR_FBCLK		MSCR_DUPPER		MSCR_DLOWER		MSCR_ADDRCTL	
W								
Reset:	1	1	1	1	1	1	1	1

Figure 13-23. FlexBus Mode Select Control Register (MSCR_FLEXBUS)

Table 13-17. MSCR_FLEXBUS Field Descriptions

Field	Description
7–6 MSCR_FBCLK	FB_CLK mode select control. These bit fields control the strength of the FlexBus clock pin. 00 Half strength 1.8V low power/mobile DDR. 01 Open drain. 10 Full strength 1.8V low power/mobile DDR. 11 2.5V DDR1 or 3.3V CMOS with roughly equal rise and fall delays.
5–4 MSCR_DUPPER	FB_D[31:16] mode select control. These bit fields control the strength of the FlexBus upper data pins. 00 Half strength 1.8V low power/mobile DDR. 01 Open drain. 10 Full strength 1.8V low power/mobile DDR. 11 2.5V DDR1 or 3.3V CMOS with roughly equal rise and fall delays.

Table 13-17. MSCR_FLEXBUS Field Descriptions (continued)

Field	Description
3–2 MSCR_ DLOWER	FB_D[15:0] mode select control. These bit fields control the strength of the FlexBus lower data pins. 00 Half strength 1.8V low power/mobile DDR. 01 Open drain. 10 Full strength 1.8V low power/mobile DDR. 11 2.5V DDR1 or 3.3V CMOS with roughly equal rise and fall delays.
1–0 MSCR_ ADDRCTL	FB_A[23:0], $\overline{\text{BE}}$ / $\overline{\text{BWE}}$ [3:0], $\overline{\text{OE}}$, $\overline{\text{R/W}}$, $\overline{\text{FB_CS}}$ [5:0], $\overline{\text{TA}}$, and $\overline{\text{TS}}$ mode select control. These bit fields control the strength of the FlexBus address and control pins. 00 Half strength 1.8V low power/mobile DDR. 01 Open drain. 10 Full strength 1.8V low power/mobile DDR. 11 2.5V DDR1 or 3.3V CMOS with roughly equal rise and fall delays.

13.3.7 SDRAM Mode Select Control Register (MSCR_SDRAM)

The MSCR_SDRAM register controls the output mode selects of the following dedicated SDRAM pins: $\overline{\text{SD_A10}}$, $\overline{\text{SD_CAS}}$, $\overline{\text{SD_CKE}}$, $\overline{\text{SD_CLK}}$, $\overline{\text{SD_CLK}}$, $\overline{\text{SD_CS0}}$, $\overline{\text{SD_DQS}}$ [3:2], $\overline{\text{SD_RAS}}$, $\overline{\text{SD_SDRDQS}}$, and $\overline{\text{SD_WE}}$.

Address: 0xFC0A_403B (MSCR_SDRAM)

Access: User read/write

	7	6	5	4	3	2	1	0
R	0	0	MSCR_SDCLKB		MSCR_SDCLK		MSCR_SDRAM	
W								
Reset:	0	0	1	1	1	1	1	1

Figure 13-24. SDRAM Mode Select Control Register (MSCR_SDRAM)

Table 13-18. MSCR_SDRAM Field Descriptions

Field	Description
7–6	Reserved, should be cleared
5–4 MSCR_ SDCLKB	$\overline{\text{SD_CLK}}$ mode select control. These bit fields control the strength of the FlexBus upper data pins. 00 Half strength 1.8V Mobile DDR. 01 Open drain. 10 Full strength 1.8V Mobile DDR. 11 2.5V DDR1 or 3.3V CMOS with roughly equal rise and fall delays.
3–2 MSCR_ SDCLK	$\overline{\text{SD_CLK}}$ mode select control. These bit fields control the strength of the FlexBus lower data pins. 00 Half strength 1.8V Mobile DDR. 01 Open drain. 10 Full strength 1.8V Mobile DDR. 11 2.5V DDR1 or 3.3V CMOS with roughly equal rise and fall delays.
1–0 MSCR_ SDRAM	$\overline{\text{SD_A10}}$, $\overline{\text{SD_CAS}}$, $\overline{\text{SD_CKE}}$, $\overline{\text{SD_CS0}}$, $\overline{\text{SD_DQS}}$ [3:2], $\overline{\text{SD_RAS}}$, $\overline{\text{SD_SDRDQS}}$, $\overline{\text{SD_WE}}$ mode select control. These bit fields control the strength of the FlexBus address and control pins. 00 Half strength 1.8V Mobile DDR. 01 Open drain. 10 Full strength 1.8V Mobile DDR. 11 2.5V DDR1 or 3.3V CMOS with roughly equal rise and fall delays.

13.3.8 Drive Strength Control Registers (DSCR_x)

The drive strength control registers set the output pin drive strengths. All drive strength control registers are read/write.

13.3.8.1 I²C Drive Strength Control Register (DSCR_I2C)

The DSCR_I2C register controls the output drive strengths of the I2C_SDA and I2C_SCL pins.

Address: 0xFC0A_403C (DSCR_I2C)

Access: User read/write

	7	6	5	4	3	2	1	0
R	0	0	0	0	0	0	I2C_DSE	
W								
Reset:	0	0	0	0	0	0	See Note	1

Note: Reset state is 0 when $\overline{RCON} = 1$, and is value of D[5] when $\overline{RCON} = 0$.

Figure 13-25. I²C Drive Strength Control Register (DSCR_I2C)

Table 13-19. DSCR_I2C Field Descriptions

Field	Description
7–2	Reserved, should be cleared
1–0 I2C_DSE	I ² C drive strength control. This bit field controls the drive strength of the I2C_SDA and I2C_SCL pins. 00 10pF 01 20pF 10 30pF 11 50pF

13.3.8.2 Miscellaneous Drive Strength Control Register (DSCR_MISC)

The DSCR_MISC register controls the output drive strengths of the following pins: PSTCLK, PST[3:0], DDATA[3:0], ALLPST, DSO, DT3IN, DT2IN, DT1IN, DT0IN, and \overline{RSTOUT} .

Address: 0xFC0A_403D (DSCR_MISC)

Access: User read/write

	7	6	5	4	3	2	1	0
R	0	0	DEBUG_DSE		RSTOUT_DSE		TIMER_DSE	
W								
Reset:	0	0	1	1	See Note	1	See Note	1

Note: Reset state is 0 when $\overline{RCON} = 1$, and is value of D[5] when $\overline{RCON} = 0$.

Figure 13-26. Miscellaneous Drive Strength Control Register (DSCR_MISC)

Table 13-20. DSCR_MISC Field Descriptions

Field	Description
7–6	Reserved, should be cleared
5–4 DEBUG_ DSE	Debug drive strength control. This bit field controls the drive strength of the PST[3:0], DDATA[3:0], ALLPST, and DSO pins. 00 10pF 01 20pF 10 30pF 11 50pF
3–2 RSTOUT_ DSE	$\overline{\text{RSTOUT}}$ drive strength control. This bit field controls the drive strength of the $\overline{\text{RSTOUT}}$ pin. 00 10pF 01 20pF 10 30pF 11 50pF
1–0 TIMER_ DSE	Timer drive strength control. This bit field controls the drive strength of the DT3IN, DT2IN, DT1IN, and DT0IN pins. 00 10pF 01 20pF 10 30pF 11 50pF

13.3.8.3 FEC Drive Strength Control Register (DSCR_FEC)

The DSCR_FEC register controls the output drive strengths of the FEC_MDC and FEC_MDIO pins.

Address: 0xFC0A_403E (DSCR_FEC)

Access: User read/write

	7	6	5	4	3	2	1	0
R	0	0	0	0	0	0	FEC_DSE	
W								
Reset:	0	0	0	0	0	0	See Note	1

Note: Reset state is 0 when $\overline{\text{RCON}} = 1$, and is value of D[5] when $\overline{\text{RCON}} = 0$.

Figure 13-27. FEC Drive Strength Control Register (DSCR_FEC)**Table 13-21. DSCR_FEC Field Descriptions**

Field	Description
7–2	Reserved, should be cleared
1–0 FEC_ DSE	FEC drive strength control. This bit field controls the drive strength of the FEC_MDC and FEC_MDIO pins. 00 10pF 01 20pF 10 30pF 11 50pF

13.3.8.4 UART/IRQ Drive Strength Control Register (DSCR_UART)

The DSCR_UART register controls the output drive strengths of the UART1, UART0, and IRQ pins.

Address: 0xFC0A_403F (DSCR_UART)

Access: User read/write

	7	6	5	4	3	2	1	0
R	0	0	UART1_DSE		UART0_DSE		IRQ_DSE	
W								
Reset:	0	0	See Note		See Note		See Note	
			1		1		1	

Note: Reset state is 0 when $\overline{\text{RCON}} = 1$, and is value of D[5] when $\overline{\text{RCON}} = 0$.

Figure 13-28. UART/IRQ Drive Strength Control Register (DSCR_UART)

Table 13-22. DSCR_UART Field Descriptions

Field	Description
7–6	Reserved, should be cleared
5–4 UART1_DSE	UART1 drive strength control. This bit field controls the drive strength of the U1RXD, U1TXD, $\overline{\text{U1CTS}}$, and $\overline{\text{U1RTS}}$ pins. 00 10pF 01 20pF 10 30pF 11 50pF
3–2 UART0_DSE	UART0 drive strength control. This bit field controls the drive strength of the U0RXD, U0TXD, $\overline{\text{U0CTS}}$, and $\overline{\text{U0RTS}}$ pins. 00 10pF 01 20pF 10 30pF 11 50pF
1–0 IRQ_DSE	IRQ drive strength control. This bit field controls the drive strength of the IRQ[7:1] pins. 00 10pF 01 20pF 10 30pF 11 50pF

13.3.8.5 QSPI Drive Strength Control Register (DSCR_QSPI)

The DSCR_QSPI register controls the output drive strengths of the QSPI_PCS2, QSPI_SCK, QSPI_DIN, and QSPI_DOUT pins.

Address: 0xFC0A_4040 (DSCR_QSPI)

Access: User read/write

	7	6	5	4	3	2	1	0
R	0	0	0	0	0	0	QSPI_DSE	
W								
Reset:	0	0	0	0	0	0	See Note	1

Note: Reset state is 0 when $\overline{RCON} = 1$, and is value of D[5] when $\overline{RCON} = 0$.

Figure 13-29. QSPI Drive Strength Control Register (DSCR_QSPI)

Table 13-23. DSCR_QSPI Field Descriptions

Field	Description
7–2	Reserved, should be cleared
1–0 QSPI_DSE	QSPI drive strength control. This bit field controls the drive strength of the QSPI_PCS2, QSPI_SCK, QSPI_DIN, QSPI_DOUT pins. 00 10pF 01 20pF 10 30pF 11 50pF

13.4 Functional Description

13.4.1 Overview

Initial pin function is determined during reset configuration. The pin assignment registers allow the user to select among various primary functions and general purpose I/O after reset. Most pins are configured as GPIO by default. The notable exceptions to this are external bus control pins, address/data pins, and chip select pins. These pins are configured for their primary functions after reset.

Every GPIO pin is individually configurable as an input or an output via a data direction register (PDDR_x). Every GPIO port has an output data register (PODR_x) and a pin data register (PPDSDR_x) to monitor and control the state of its pins. Data written to a PODR_x register is stored and then driven to the corresponding port *x* pins configured as outputs.

Reading a PODR_x register returns the current state of the register regardless of the state of the corresponding pins. Reading a PPDSDR_x register returns the current state of the corresponding pins when configured as general purpose I/O, regardless of whether the pins are inputs or outputs.

Every GPIO port has a PPDSDR_x register and a clear register (PCLRR_x) for setting or clearing individual bits in the PODR_x register. Initial pin output drive strength is determined during reset configuration. The DSCR_x registers allow the pin drive strengths to be configured on a per-function basis after reset.

13.4.2 Port Digital I/O Timing

Input data on all pins configured as general purpose input is synchronized to the rising edge of the bus clock, FB_CLK, as shown in [Figure 13-30](#).

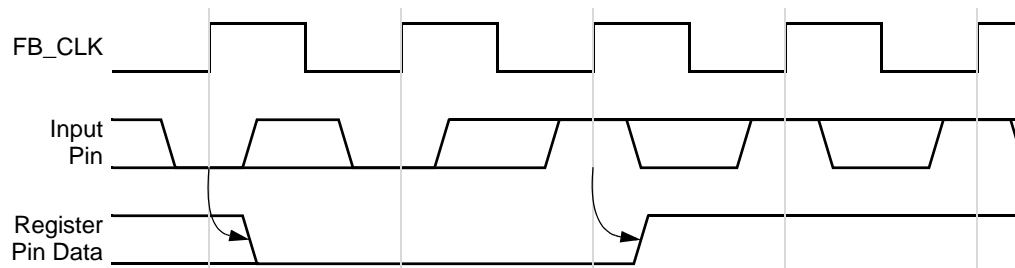


Figure 13-30. General Purpose Input Timing

Data written to the **PODR_x** register of any pin configured as a general purpose output is immediately driven to its respective pin, as shown in [Figure 13-31](#).

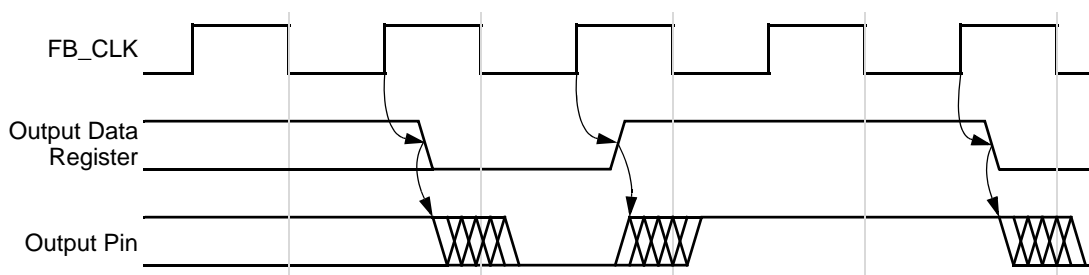


Figure 13-31. General Purpose Output Timing

13.5 Initialization/Application Information

The initialization for the ports module is done during reset configuration. All registers are reset to a predetermined state. Refer to [Section 13.3, “Memory Map/Register Definition,”](#) for more details on reset and initialization.

Chapter 14

Interrupt Controller Module

14.1 Introduction

This section details the functionality of the interrupt controller (INTC). The general features of the interrupt controller block include:

- 64 fully-programmable interrupt sources. Not all possible interrupt source locations are used on this device.
- Each of the sources has a unique interrupt control register (ICR n) to define the software-assigned levels.
- Unique vector number for each interrupt source.
- Ability to mask any individual interrupt source, plus global mask-all capability.
- Supports hardware and software interrupt acknowledge cycles.
- Wake-up signal from low-power stop modes.

The 64, fully-programmable interrupt sources for the interrupt controller manage the complete set of interrupt sources from all of the modules on the device. This section describes how the interrupt sources are mapped to the interrupt controller logic and how interrupts are serviced.

14.1.1 68 K/ColdFire Interrupt Architecture Overview

Before continuing with the specifics of the interrupt controller, a brief review of the interrupt architecture of the 68K/ColdFire family is appropriate.

The interrupt architecture of ColdFire is exactly the same as the M68000 family, where there is a 3-bit encoded interrupt priority level sent from the interrupt controller to the core, providing 7 levels of interrupt requests. Level 7 represents the highest priority interrupt level, while level 1 is the lowest priority. The processor samples for active interrupt requests once-per-instruction by comparing the encoded priority level against a 3-bit interrupt mask value (I) contained in bits 10:8 of the machine's status register (SR). If the priority level is greater than the SR[I] field at the sample point, the processor suspends normal instruction execution and initiates interrupt exception processing. Level 7 interrupts are treated as non-maskable and edge-sensitive within the processor, while levels 1-6 are treated as level-sensitive and may be masked depending on the value of the SR[I] field. For correct operation, the ColdFire device requires that, after asserted, the interrupt source remain asserted until explicitly disabled by the interrupt service routine.

During the interrupt exception processing, the CPU enters supervisor mode, disables trace mode, and then fetches an 8-bit vector from the interrupt controller. This byte-sized operand fetch is known as the interrupt acknowledge (IACK) cycle with the ColdFire implementation using a special memory-mapped address

space within the interrupt controller. The fetched data provides an index into the exception vector table that contains 256 addresses, each pointing to the beginning of a specific exception service routine. In particular, vectors 64 - 255 of the exception vector table are reserved for user interrupt service routines. The first 64 exception vectors are reserved for the processor to manage reset, error conditions (access, address), arithmetic faults, system calls, etc. After the interrupt vector number has been retrieved, the processor continues by creating a stack frame in memory. For ColdFire, all exception stack frames are 2 longwords in length, and contain 32 bits of vector and status register data, along with the 32-bit program counter value of the instruction that was interrupted (see [Section 3.3.3.1, “Exception Stack Frame Definition,”](#) for more information on the stack frame format). After the exception stack frame is stored in memory, the processor accesses the 32-bit pointer from the exception vector table using the vector number as the offset, and then jumps to that address to begin execution of the service routine. After the status register is stored in the exception stack frame, the SR[I] mask field is set to the level of the interrupt being acknowledged, effectively masking that level and all lower values while in the service routine.

The processing of the interrupt acknowledge cycle is fundamentally different than previous 68K/ColdFire cores. In this approach, all IACK cycles are directly managed by the interrupt controller, so the requesting peripheral device is not accessed during the IACK. As a result, the interrupt request must be explicitly cleared in the peripheral during the interrupt service routine. For more information, see [Section 14.3.1.3, “Interrupt Vector Determination.”](#)

ColdFire processors guarantee that the first instruction of the service routine is executed before sampling for interrupts is resumed. By making this initial instruction a load of the SR, interrupts can be safely disabled, if required.

For more information on exception processing, see the *ColdFire Programmer's Reference Manual* at <http://www.freescale.com/coldfire>.

14.2 Memory Map/Register Definition

The register programming model for the interrupt controller is memory-mapped to a 256-byte space. In the following discussion, there are a number of program-visible registers greater than 32 bits in size. For these control fields, the physical register is partitioned into two 32-bit values: a register high (the upper longword) and a register low (the lower longword). The nomenclature <reg_name>H and <reg_name>L is used to reference these values.

The registers and their locations are defined in [Table 14-2](#). The base addresses for the interrupt controller is listed below.

Table 14-1. Interrupt Controller Base Addresses

Interrupt Controller Number	Base Address
INTC	0xFC04_8000

Table 14-2. Interrupt Controller Memory Map

Address	Register	Width (bits)	Access	Reset Value	Section/ Page
Interrupt Controller 0					
0xFC04_8000	Interrupt Pending Register High (IPRH)	32	R	0x0000_0000	14.2.1/14-3
0xFC04_8004	Interrupt Pending Register Low (IPRL)	32	R	0x0000_0000	14.2.1/14-3
0xFC04_8008	Interrupt Mask Register High (IMRH)	32	R/W	0xFFFF_FFFF	14.2.2/14-4
0xFC04_800C	Interrupt Mask Register Low (IMRL)	32	R/W	0xFFFF_FFFF	14.2.2/14-4
0xFC04_8010	Interrupt Force Register High (INTFRCH)	32	R/W	0x0000_0000	14.2.3/14-6
0xFC04_8014	Interrupt Force Register Low (INTFRCL)	32	R/W	0x0000_0000	14.2.3/14-6
0xFC04_801A	Interrupt Configuration Register (ICONFIG)	16	R/W	0x0000	14.2.4/14-6
0xFC04_801C	Set Interrupt Mask (SIMR)	8	W	0x00	14.2.5/14-7
0xFC04_801D	Clear Interrupt Mask (CIMR)	8	W	0x00	14.2.6/14-8
0xFC04_801E	Current Level Mask (CLMASK)	8	R/W	0x0F	14.2.7/14-8
0xFC04_801F	Saved Level Mask (SLMASK)	8	R/W	0x0F	14.2.8/14-9
0xFC04_8040 + n ($n=0:63$)	Interrupt Control Registers (ICR n)	8	R/W	0x00	14.2.9/14-10
0xFC04_80E0	Software Interrupt Acknowledge (SWIACK)	8	R	0x00	14.2.10/14-12
0xFC04_80E0 + $4n$ ($n=1:7$)	Level n Interrupt Acknowledge Registers (L n IACK)	8	R	0x18	14.2.10/14-12

14.2.1 Interrupt Pending Registers (IPRH, IPRL)

The IPRH and IPRL registers, [Figure 14-1](#) and [Figure 14-2](#), are each 32 bits in size, and provide a bit map for each interrupt request to indicate if there is an active request (1 equals active request, 0 equals no request) for the given source. The interrupt mask register state does not affect the IPR. The IPR is cleared by reset and is a read-only register, so any attempted write to this register is ignored.

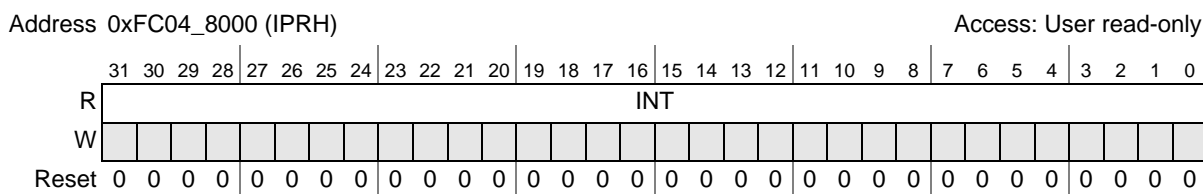


Figure 14-1. Interrupt Pending Register High (IPRH)

Table 14-3. IPRH Field Descriptions

Field	Description
31–0 INT	Interrupt pending. Each bit corresponds to an interrupt source. The corresponding IMRH n bit determines whether an interrupt condition can generate an interrupt. At every system clock, the IPRH samples the signal generated by the interrupting source. The corresponding IPRH bit reflects the state of the interrupt signal even if the corresponding IMRH n bit is set. 0 The corresponding interrupt source does not have an interrupt pending 1 The corresponding interrupt source has an interrupt pending

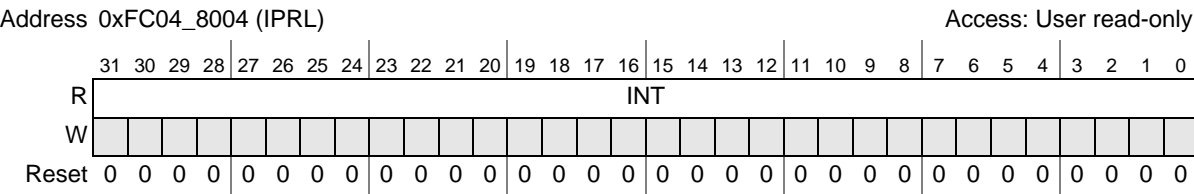


Figure 14-2. Interrupt Pending Register Low (IPRL)

Table 14-4. IPRL Field Descriptions

Field	Description
31–0 INT	Interrupt Pending. Each bit corresponds to an interrupt source. The corresponding IMRL n bit determines whether an interrupt condition can generate an interrupt. At every system clock, the IPRL samples the signal generated by the interrupting source. The corresponding IPRL bit reflects the state of the interrupt signal even if the corresponding IMRL bit is set. 0 The corresponding interrupt source does not have an interrupt pending 1 The corresponding interrupt source has an interrupt pending

14.2.2 Interrupt Mask Register (IMRH, IMRL)

The IMRH and IMRL registers are each 32 bits in size and provide a bit map for each interrupt to allow the request to be disabled (1 equals disable the request, 0 equals enable the request). The IMRL register is used for masking interrupt sources 0 to 31, while the IMRH register is used for masking interrupts 32 to 63. The IMR is set to all ones by reset, disabling all interrupt requests. The IMR can be read and written.

NOTE

A spurious interrupt may occur if an interrupt source is being masked in the interrupt controller mask register (IMR) or a module's interrupt mask register while the interrupt mask in the status register (SR[I]) is set to a value lower than the interrupt's level. This is because by the time the status register acknowledges this interrupt, the interrupt has been masked. A spurious interrupt is generated because the CPU cannot determine the interrupt source. To avoid this situation for interrupts sources with levels 1-6, first write a higher level interrupt mask to the status register, before setting the mask in the IMR or the module's interrupt mask register. After the mask is set, return the interrupt mask in the status register to its previous value. Because level 7 interrupts cannot be disabled in the status register prior to masking, use of the IMR or module interrupt mask registers to disable level 7 interrupts is not recommended.

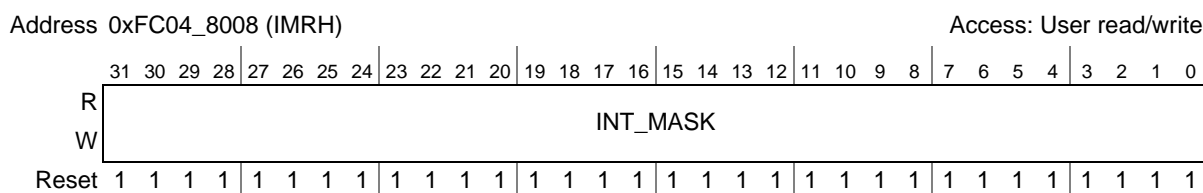


Figure 14-3. Interrupt Mask Register High (IMRH)

Table 14-5. IMRH Field Descriptions

Field	Description
31–0 INT_MASK	Interrupt mask. Each bit corresponds to an interrupt source. The corresponding IMRH bit determines whether an interrupt condition can generate an interrupt. The corresponding IPRH bit reflects the state of the interrupt signal even if the corresponding IMRH bit is set. 0 The corresponding interrupt source is not masked 1 The corresponding interrupt source is masked

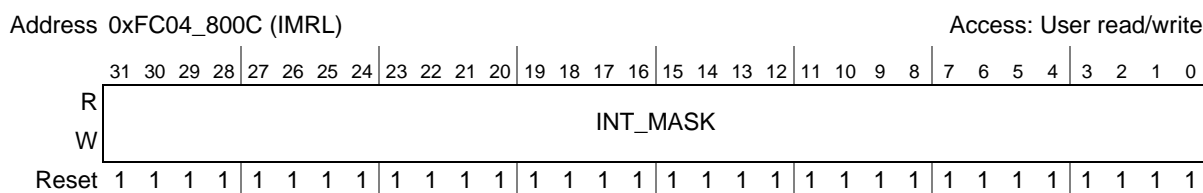


Figure 14-4. Interrupt Mask Register Low (IMRL)

Table 14-6. IMRL Field Descriptions

Field	Description
31–0 INT_MASK	Interrupt mask. Each bit corresponds to an interrupt source. The corresponding IMRL bit determines whether an interrupt condition can generate an interrupt. The corresponding IPRL bit reflects the state of the interrupt signal even if the corresponding IMRL bit is set. 0 The corresponding interrupt source is not masked 1 The corresponding interrupt source is masked

14.2.3 Interrupt Force Registers (INTFRCH, INTFRCL)

The INTFRCH and INTFRCL registers are each 32 bits in size and provide a mechanism to allow software generation of interrupts for each possible source for functional or debug purposes. The system design may reserve one or more sources to allow software to self-schedule interrupts by forcing one or more of these bits (set to force request, clear to negate request) in the appropriate INTFRC register. The INTFRCL register forces interrupts for sources 0 to 31, while the INTFRCH register forces interrupts for sources 32 to 63. The assertion of an interrupt request via the interrupt force register is not affected by the interrupt mask register. The INTFRC registers are cleared by reset.

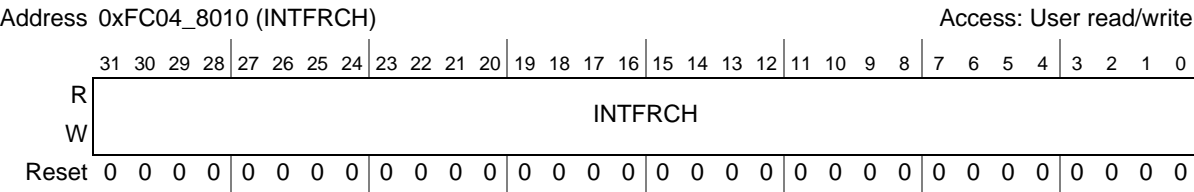


Figure 14-5. Interrupt Force Register High (INTFRCH)

Table 14-7. INTFRCH Field Descriptions

Field	Description
31–0 INTFRCH	Interrupt force. Allows software generation of interrupts for each possible source for functional or debug purposes. 0 No interrupt forced on the corresponding interrupt source 1 Force an interrupt on the corresponding source

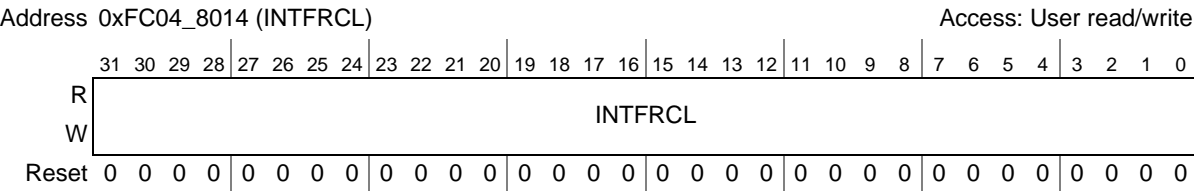


Figure 14-6. Interrupt Force Register Low (INTFRCL)

Table 14-8. INTFRCL Field Descriptions

Field	Description
31–0 INTFRCL	Interrupt force. Allows software generation of interrupts for each possible source for functional or debug purposes. 0 No interrupt forced on corresponding interrupt source 1 Force an interrupt on the corresponding source

14.2.4 Interrupt Configuration Register (ICONFIG)

This 16-bit register defines the operating configuration for the interrupt controller module.

Address: 0xFC04_801A (ICONFIG)

Access: User read/write

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	ELVLPRI							0	0	0	EMASK	0	0	0	0	0
W																
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Figure 14-7. Interrupt Configuration Register (ICONFIG)

Table 14-9. ICONFIG Field Descriptions

Field	Description
15–9 ELVLPRI	Enable core's priority elevation on priority levels. Each ELVLPRI[7:1] bit corresponds to the available priority levels 1 – 7. If set, the assertion of the corresponding level- <i>n</i> request to the core causes the processor's bus master priority to be temporarily elevated in the device's crossbar switch arbitration logic. The processor's bus master arbitration priority remains elevated until the level- <i>n</i> request is negated. If round-robin arbitration is enabled, this bit has no effect. If cleared, the assertion of a level- <i>n</i> request does not affect the processor's bus master priority.
8–6	Reserved, must be cleared.
5 EMASK	If set, the interrupt controller automatically loads the level of an interrupt request into the CLMASK (current level mask) when the acknowledge is performed. At the exact same cycle, the value of the current interrupt level mask is saved in the SLMASK (saved level mask) register. This feature can be used to support software-managed nested interrupts, and is intended to complement the interrupt masking functions supported in the ColdFire processor. The value of SLMASK register should be read from the interrupt controller and saved in the interrupt stack frame in memory, and restored near the service routine's exit. If cleared, the INTC does not perform any automatic masking of interrupt levels. The state of this bit does not affect the ColdFire processor's interrupt masking logic in any manner.
4–0	Reserved, must be cleared.

14.2.5 Set Interrupt Mask Register (SIMR)

The SIMR register provides a simple mechanism to set a given bit in the IMR registers to mask the corresponding interrupt request. The value written to the SIMR field causes the corresponding bit in the IMR register to be set. The SIMR[SALL] bit provides a global set function, forcing the entire contents of IMR to be set, thus masking all interrupts. Reads of this register return all zeroes. This register is provided so interrupt service routines can easily mask the given interrupt request without the need to perform a read-modify-write sequence on the IMR register.

Address: 0xFC04_801C (SIMR)

Access: User write-only

	7	6	5	4	3	2	1	0
R	0	0	0	0	0	0	0	0
W	SALL		SIMR					
Reset:	0	0	0	0	0	0	0	0

Figure 14-8. Set Interrupt Mask Register (SIMR)

Table 14-10. SIMR Field Descriptions

Field	Description
7	Reserved, must be cleared.
6 SALL	Set all bits in the IMR register, masking all interrupt requests. 0 Only set those bits specified in the SIMR field. 1 Set all bits in IMR register. The SIMR field is ignored.
5–0 SIMR	Set the corresponding bit in the IMR register, masking the interrupt request.

14.2.6 Clear Interrupt Mask Register (CIMR)

The CIMR register provides a simple mechanism to clear a given bit in the IMR registers to enable the corresponding interrupt request. The value written to the CIMR field causes the corresponding bit in the IMR register to be cleared. The CIMR[CALL] bit provides a global clear function, forcing the entire contents of IMR to be cleared, thus enabling all interrupts. Reads of this register return all zeroes. This register is provided so interrupt service routines can easily enable the given interrupt request without the need to perform a read-modify-write sequence on the IMR register.

In the event of a simultaneous write to the CIMR and SIMR, the SIMR has priority and the resulting function would be a set of the interrupt mask register.

Address: 0xFC04_801D (CIMR)

Access: User write-only

	7	6	5	4	3	2	1	0
R	0	0	0	0	0	0	0	0
W		CALL	CIMR					
Reset:	0	0	0	0	0	0	0	0

Figure 14-9. Clear Interrupt Mask Register (CIMR)

Table 14-11. CIMR Field Descriptions

Field	Description
7	Reserved, must be cleared.
6 CALL	Clear all bits in the IMR register, enabling all interrupt requests. 0 Only set those bits specified in the CIMR field. 1 Clear all bits in IMR register. The CIMR field is ignored.
5–0 CIMR	Clear the corresponding bit in the IMR register, enabling the interrupt request.

14.2.7 Current Level Mask Register (CLMASK)

The CLMASK register is provided so the interrupt controller can optionally automatically manage masking of interrupt requests based on the programmed priority level. If enabled by ICONFIG[EMASK] bit being set, an interrupt acknowledge read cycle returns a vector number identifying the physical request source, and the CLMASK register is loaded with the level number associated with the request. After the

CLMASK register is updated, then all interrupt requests with level numbers equal to or less than this value are masked by the controller and are not allowed to cause the assertion of the interrupt signal to the processor core. As the CLMASK register is updated during the IACK cycle read, the former value is saved in the SLMASK register.

Typically, after a level-*n* interrupt request is managed, the service routine restores the saved level mask value into the current level mask register to re-enable the lower priority requests. In addition, an interrupt service routine can explicitly load this register with a lower priority value to query for any pending interrupts via software interrupt acknowledge cycles.

Address: 0xFC04_801E (CLMASK)

Access: User read/write

	7	6	5	4	3	2	1	0
R	0	0	0	0	CLMASK			
W								
Reset:	0	0	0	0	1	1	1	1

Figure 14-10. Current Level Mask Register (CLMASK)

Table 14-12. CLMASK Field Descriptions

Field	Description
7–4	Reserved, must be cleared.
3–0 CLMASK	Current level mask. Defines the level mask, where only interrupt levels greater than the current value are processed by the controller 0000 Level 1 – 7 requests are processed. 0001 Level 2 – 7 requests are processed. 0010 Level 3 – 7 requests are processed. 0011 Level 4 – 7 requests are processed. 0100 Level 5 – 7 requests are processed. 0101 Level 6 – 7 requests are processed. 0110 Level 7 requests are processed. 0111 All requests are masked. 1000 – 1110 Reserved. 1111 Level 1 – 7 requests are processed.

14.2.8 Saved Level Mask Register (SLMASK)

The SLMASK register is provided so the interrupt controller can optionally automatically manage masking of interrupt requests based on the programmed priority level. If enabled by ICONFIG[EMASK] bit being set, an interrupt acknowledge read cycle returns a vector number identifying the physical request source, and the CLMASK register is loaded with the level number associated with the request. After the CLMASK register is updated, then all interrupt requests with level numbers equal to or less than this value are masked by the controller and are not allowed to cause the assertion of the interrupt signal to the processor core. As the CLMASK register is updated during the IACK cycle read, the former value is saved in the SLMASK register.

Typically, after a level-*n* interrupt request is managed, the service routine restores the saved level mask value into the current level mask register to re-enable the lower priority requests.

Address: 0xFC04_801F (SLMASK)

Access: User read/write

	7	6	5	4	3	2	1	0
R	0	0	0	0	SLMASK			
W								
Reset:	0	0	0	0	1	1	1	1

Figure 14-11. Saved Level Mask Register (SLMASK)

Table 14-13. SLMASK Field Descriptions

Field	Description
7–4	Reserved, must be cleared.
3–0 SLMASK	Saved level mask. Defines the saved level mask. See the CLMASK field definition for more information on the specific values.

14.2.9 Interrupt Control Register (ICR_n, (n = 00, 01, 02, ..., 63))

Each ICR register specifies the interrupt level (1–7) for the corresponding interrupt source. These registers are cleared by reset and should be programmed with the appropriate levels before interrupts are enabled.

When multiple interrupt requests are programmed to the same level number, they are processed in a descending request number order. As an example, if requests 63, 62, 2, and 1 are programmed to a common level, request 63 is processed first, then request 62, then request 2, and finally request 1.

This definition allows software maximum flexibility in grouping interrupt request sources within any given priority level. The priority level in the ICRs directly corresponds to the interrupt level supported by the ColdFire processor.

Address: 0xFC04_8040 – 7F (ICR00 – ICR63)

Access: User read/write

	7	6	5	4	3	2	1	0
R	0	0	0	0	0	LEVEL		
W								
Reset:	0	0	0	0	0	0	0	0

Figure 14-12. Interrupt Control Registers (ICR_n)Table 14-14. ICR_n Field Descriptions

Field	Description
7–3	Reserved, must be cleared.
2–0 LEVEL	Interrupt level. Indicates the interrupt level assigned to each interrupt input. A level of 0 effectively disables the interrupt request, while a level 7 interrupt is given the highest priority. If interrupt masking is enabled (ICONFIG[EMASK] = 1), the acknowledgement of a level- <i>n</i> request forces the controller to automatically mask all interrupt requests of level- <i>n</i> and lower.

14.2.9.1 Interrupt Sources

Table 14-15 list the interrupt sources for each interrupt request line for INTC.

Table 14-15. Interrupt Source Assignment For INTC

Source	Module	Flag	Source Description	Flag Clearing Mechanism
0	Not Used			
1	EPORT	EPFR[EPF1]	Edge port flag 1	Write 1 to EPF1
2		EPFR[EPF4]	Edge port flag 4	Write 1 to EPF4
3		EPFR[EPF7]	Edge port flag 7	Write 1 to EPF7
4	PIT0	PCSR0[PIF]	PIT interrupt flag	Write 1 to PIF or write PMR
5	PIT1	PCSR0[PIF]	PIT interrupt flag	Write 1 to PIF or write PMR
6	Not Used			
7	Not Used			
8	DMA	EDMA_INTR[INT00]	DMA Channel 0 transfer complete	Write EDMA_CINTR[CINT] = 0
9		EDMA_INTR[INT01]	DMA Channel 1 transfer complete	Write EDMA_CINTR[CINT] = 1
10		EDMA_INTR[INT02]	DMA Channel 2 transfer complete	Write EDMA_CINTR[CINT] = 2
11		EDMA_INTR[INT03]	DMA Channel 3 transfer complete	Write EDMA_CINTR[CINT] = 3
12		EDMA_INTR[INT04]	DMA Channel 4 transfer complete	Write EDMA_CINTR[CINT] = 4
13		EDMA_INTR[INT05]	DMA Channel 5 transfer complete	Write EDMA_CINTR[CINT] = 5
14		EDMA_INTR[INT06]	DMA Channel 6 transfer complete	Write EDMA_CINTR[CINT] = 6
15		EDMA_INTR[INT07]	DMA Channel 7 transfer complete	Write EDMA_CINTR[CINT] = 7
16		EDMA_INTR[INT08]	DMA Channel 8 transfer complete	Write EDMA_CINTR[CINT] = 8
17		EDMA_INTR[INT09]	DMA Channel 9 transfer complete	Write EDMA_CINTR[CINT] = 9
18		EDMA_INTR[INT10]	DMA Channel 10 transfer complete	Write EDMA_CINTR[CINT] = 10
19		EDMA_INTR[INT11]	DMA Channel 11 transfer complete	Write EDMA_CINTR[CINT] = 11
20		EDMA_INTR[INT12]	DMA Channel 12 transfer complete	Write EDMA_CINTR[CINT] = 12
21		EDMA_INTR[INT13]	DMA Channel 13 transfer complete	Write EDMA_CINTR[CINT] = 13
22		EDMA_INTR[INT14]	DMA Channel 14 transfer complete	Write EDMA_CINTR[CINT] = 14
23		EDMA_INTR[INT15]	DMA Channel 15 transfer complete	Write EDMA_CINTR[CINT] = 15
24		EDMA_ERR[ERR n]	DMA Error Interrupt	Write EDMA_CERR[CERR] = n
25	SCM	SCMIR[CWIC]	Core Watchdog Timeout	Write 1 to SCMISR[CWIC]
26	UART0	UISR0 register	UART0 Interrupt Request	Automatically cleared
27	UART1	UISR1 register	UART1 Interrupt Request	Automatically cleared
28	UART2	UISR2 register	UART2 Interrupt Request	Automatically cleared
29	Not Used			

Table 14-15. Interrupt Source Assignment For INTC (continued)

Source	Module	Flag	Source Description	Flag Clearing Mechanism
30	I ² C	I2SR[IIF]	I ² C Interrupt	Write 0 to I2SR[IIF]
31	QSPI	QIR register	QSPI interrupt	Write 1 to appropriate QIR bit
32	DTIM0	DTER0 register	DMA Timer 0 interrupt	Write 1 to appropriate DTER0 bit
33	DTIM1	DTER1 register	DMA Timer 1 interrupt	Write 1 to appropriate DTER1 bit
34	DTIM2	DTER2 register	DMA Timer 2 interrupt	Write 1 to appropriate DTER2 bit
35	DTIM3	DTER3 register	DMA Timer 3 interrupt	Write 1 to appropriate DTER3 bit
36	FEC	EIR[TXF]	Transmit frame interrupt	Write EIR[TXF] = 1
37		EIR[TXB]	Transmit buffer interrupt	Write EIR[TXB] = 1
38		EIR[UN]	Transmit FIFO underrun	Write EIR[UN] = 1
39		EIR[RL]	Collision retry limit	Write EIR[RL] = 1
40		EIR[RXF]	Receive frame interrupt	Write EIR[RXF] = 1
41		EIR[RXB]	Receive buffer interrupt	Write EIR[RXB] = 1
42		EIR[MII]	MII interrupt	Write EIR[MII] = 1
43		EIR[LC]	Late collision	Write EIR[LC] = 1
44		EIR[HBERR]	Heartbeat error	Write EIR[HBERR] = 1
45		EIR[GRA]	Graceful stop complete	Write EIR[GRA] = 1
46		EIR[EBERR]	Ethernet bus error	Write EIR[EBERR] = 1
47		EIR[BABT]	Babbling transmit error	Write EIR[BABT] = 1
48		EIR[BABR]	Babbling receive error	Write EIR[BABR] = 1
49–61	Not Used			
62	SCM	SCMISR[CFEI]	Bus error interrupt	Write SCMISR[CFEI] = 1
63	Not Used			

14.2.10 Software and Level 1 – 7 IACK Registers (SWIACK, L1IACK – L7IACK)

The eight IACK registers can be explicitly addressed via the CPU, or implicitly addressed via a processor-generated interrupt acknowledge cycle during exception processing. In either case, the interrupt controller's actions are very similar.

First, consider an IACK cycle to a specific level: a level-*n* IACK. When this type of IACK arrives in the interrupt controller, the controller examines all the currently-active level *n* interrupt requests, determines the highest priority within the level, and then responds with the unique vector number corresponding to that specific interrupt source. The vector number is supplied as the data for the byte-sized IACK read cycle. In addition to providing the vector number, the interrupt controller also loads the level into the CLMASK register, where it may be retrieved later.

This interrupt controller design also supports the concept of a software IACK. A software IACK allows an interrupt service routine to determine if there are other pending interrupts so that the overhead associated with interrupt exception processing (including machine state save/restore functions) can be minimized. In general, the software IACK is performed near the end of an interrupt service routine, and if there are additional active interrupt sources, the current interrupt service routine (ISR) passes control to the appropriate service routine, but without taking another interrupt exception.

When the interrupt controller receives a software IACK read, it returns the vector number associated with the highest unmasked interrupt source for that interrupt controller. If there are no active sources, the interrupt controller returns an all-zero vector as the operand for the SWIACK register. A read from the L_n IACK registers when there are no active requests returns a value of 24 (0x18), signaling a spurious interrupt.

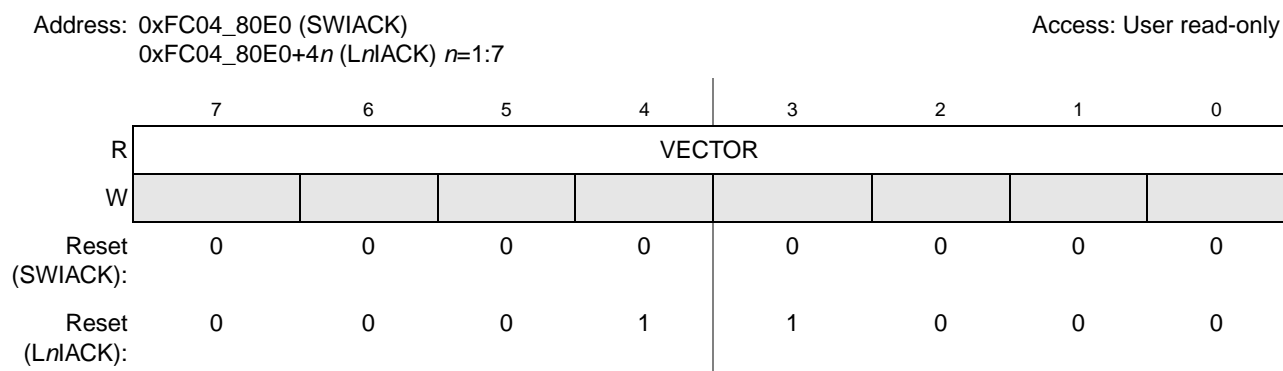


Figure 14-13. Software and Level n IACK Registers (SWIACK $_n$, L1IACK $_n$ – L7IACK $_n$)

Table 14-16. SWIACK $_n$ and L_n IACK $_n$ Field Descriptions

Field	Description
7–0 VECTOR	Vector number. A read from the SWIACK register returns the vector number associated with the highest priority pending interrupt source. A read from one of the L_n IACK registers returns the highest priority unmasked interrupt source within the level. A write to any IACK register causes an error termination.

14.3 Functional Description

14.3.1 Interrupt Controller Theory of Operation

To support the interrupt architecture of the 68K/ColdFire programming model, the 64 interrupt sources are organized as 7 levels, with an arbitrary number of requests programmed to each level. The priority structure within a single interrupt level depends on the interrupt source number assignments (see [Section 14.2.9.1, “Interrupt Sources”](#)). The higher numbered interrupt source has priority over the lower numbered interrupt source. See the below table for an example.

Table 14-17. Example Interrupt Priority Within a Level

Interrupt Source	ICR[2:0]	Priority
40	011	Highest
22	011	
8	011	
2	011	Lowest

The level is fully programmable for all sources. The 3-bit level is defined in the interrupt control register (ICR_{*n*}).

The operation of the interrupt controller can be broadly partitioned into three activities:

- Recognition
- Prioritization
- Vector determination during IACK

14.3.1.1 Interrupt Recognition

The interrupt controller continuously examines the request sources (IPR) and the interrupt mask register (IMR) to determine if there are active requests. This is the recognition phase. The interrupt force register (INTFRC) also factors into the generation of an active request.

14.3.1.2 Interrupt Prioritization

As an active request is detected, it is translated into the programmed interrupt level. Next, the appropriate level masking is performed if this feature is enabled. The level of the active request must be greater than the current mask level before it is signaled in the processor. The resulting unmasked decoded priority level is driven out of the interrupt controller to the processor core during this prioritization phase.

14.3.1.3 Interrupt Vector Determination

After the core has sampled for pending interrupts and begun interrupt exception processing, it generates an interrupt acknowledge cycle (IACK). The IACK transfer is treated as a memory-mapped byte read by the processor, and routed to the appropriate interrupt controller. Next, the interrupt controller extracts the level being acknowledged from address bits[4:2], and then determines the highest unmasked level for the type of interrupt being acknowledged, and returns the 8-bit interrupt vector for that request to complete the cycle. The 8-bit interrupt vector is formed using the following algorithm:

For INTC, $\text{vector_number} = 64 + \text{interrupt source number}$

Recall vector_numbers 0-63 are reserved for the ColdFire processor and its internal exceptions. Thus, the following mapping of bit positions to vector numbers applies for INTC:

```
if interrupt source 0 is active and acknowledged, then vector_number = 64
if interrupt source 1 is active and acknowledged, then vector_number = 65
if interrupt source 2 is active and acknowledged, then vector_number = 66
...
```

if interrupt source 63 is active and acknowledged, then vector_number = 127

The net effect is a fixed mapping between the bit position within the source to the actual interrupt vector number.

If there is no active interrupt source for the given level, a special spurious interrupt vector (vector_number equals 24) is returned and it is the responsibility of the service routine to manage this error situation.

This protocol implies the interrupting peripheral is not accessed during the acknowledge cycle because the interrupt controller completely services the acknowledge. This means the interrupt source must be explicitly disabled in the interrupt service routine. This design provides unique vector capability for all interrupt requests, regardless of the complexity of the peripheral device.

In some applications, it is expected that the hardware masking of interrupt levels by the interrupt controller is enabled. This masking capability can be used with the processor's masking logic to form a dual-mask capability. In this operation mode, the IACK read cycle also causes the current interrupt level mask to be saved in the SLMASK register, and the new level being acknowledged loaded into the CLMASK register. This operation then automatically masks the new level (and all lower levels) while in the service routine. Generally, as the service routine completes execution, and the initiating request source has been negated, the saved mask level is restored into the current mask level to re-enable the lower priority levels.

Finally, the vector number returned during the IACK cycle provides the association with the request and the physical interrupt signal. The CLMASK and SLMASK registers are all loaded (if properly enabled) during the interrupt acknowledge read cycle.

14.3.2 Low-Power Wake-up Operation

The system control module (SCM) contains an 8-bit low-power control register (LPCR) to control the low-power stop mode. This register must be explicitly programmed by software to enter low-power mode. It also contains a wake-up control register (WCR) sets the priority level of the interrupt necessary to bring the device out of the specified low-power mode. Refer to [Chapter 8, “Power Management,”](#) for definitions of the LPCR and WCR registers, as well as more information on low-power modes.

Each interrupt controller provides a special combinatorial logic path to provide a special wake-up signal to exit from the low-power stop mode. This special mode of operation works as follows:

1. The WCR register is programmed, setting the ENBWCR bit and the desired interrupt priority level.
2. At the appropriate time, the processor executes the privileged STOP instruction. After the processor has stopped execution, it asserts a specific processor status (PST) encoding. Issuing the STOP instruction when the WCR[ENBWCR] bit is set causes the SCM to enter the mode specified in LPCR[LPMD].
3. The entry into a low-power mode is processed by the low-power mode control logic, and the appropriate clocks (usually those related to the high-speed processor core) are disabled.
4. After entering the low-power mode, the interrupt controller enables a combinatorial logic path which evaluates any unmasked interrupt requests. The device waits for an event to generate a level 7 interrupt request or an interrupt request with a priority level greater than the value programmed in WCR[PRILVL].

5. After an appropriately high interrupt request level arrives, the interrupt controller signals its presence, and the SCM responds by asserting the request to exit low-power mode.
6. The low-power mode control logic senses the request signal and re-enables the appropriate clocks.
7. With the processor clocks enabled, the core processes the pending interrupt request.

For more information, see ”.

14.4 Initialization/Application Information

The interrupt controller’s reset state has all requests masked via the IMR. Before any interrupt requests are enabled, the following steps must be taken:

1. Set the ICONFIG register to the desired system configuration.
2. Program the ICR_n registers with the appropriate interrupt levels.
3. The reset value for the level mask registers (CLMASK and SLMASK) is 0xF (no levels masked). Typically, these registers do not need to be modified before interrupts are enabled.
4. Load the appropriate interrupt vector tables and interrupt service routines into memory.
5. Enable the interrupt requests, by clearing the appropriate bits in the IMR and lowering the interrupt mask level in the core’s status register (SR[I]) to an appropriate level.

14.4.1 Interrupt Service Routines

This section focuses on the interaction of the interrupt masking functionality with the service routine. Figure 14-14 presents a timing diagram showing various phases during the execution of an interrupt service routine with the controller level masking functionality enabled. The time scale in this diagram is not meant to be accurate.

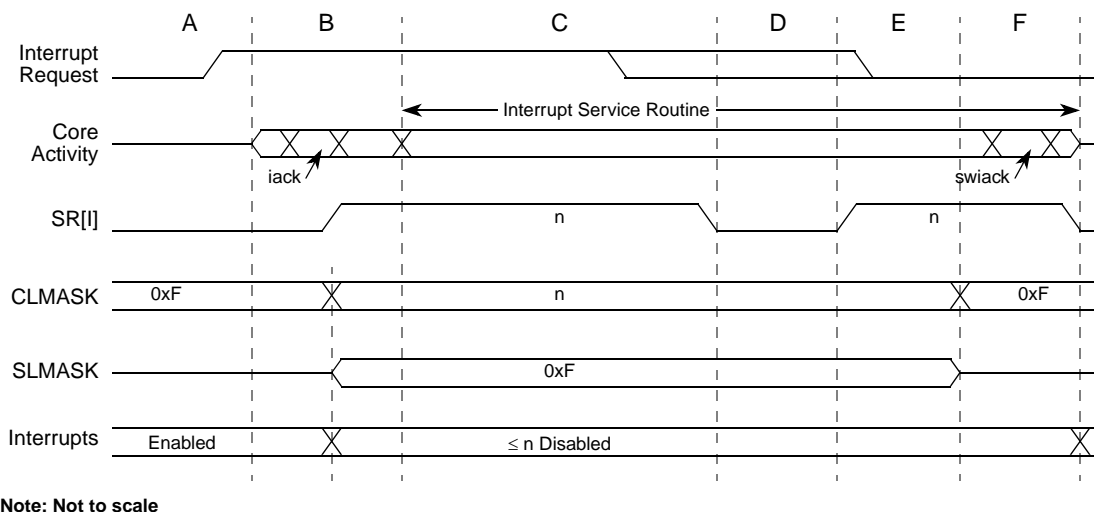


Figure 14-14. Interrupt Service Routine and Masking

Consider the events depicted in each segment (A – F) of the above diagram.

In A, an interrupt request is asserted, which is then signalled to the core.

As B begins, the interrupt request is recognized, and the core begins interrupt exception processing. During the core's exception processing, the IACK cycle performs and the interrupt controller returns the appropriate vector number. As the interrupt acknowledge read performs, the vector number returns to the core. The contents of the CLMASK register load into the SLMASK register, and the CLMASK register updates to the level of the acknowledge interrupt. Additionally, the processor raises the interrupt mask in the status register (SR[I]) to match the level of the acknowledged request. At the end of the core's exception processing, control passes to the interrupt service routine (ISR), shown as the beginning of segment C.

During C, the initial portion of the ISR executes. Near the end of this segment, the ISR accesses the peripheral to negate the interrupt request source. At the conclusion of segment C, the SR[I] field can be lowered to re-enable interrupts with a priority greater than the original request.

The bulk of the interrupt service routine executes in segment D, with interrupts enabled. Near the end of the service routine, the SR[I] field is again raised to the original acknowledged level, preparing to perform the context switch.

At the end of segment E, the original value in the saved level mask (SLMASK) is restored in the current level mask (CLMASK). Optionally, the service routine can directly load the CLMASK register with any value with pending interrupt requests of certain levels need to be examined.

In segment F, the interrupt service routine completes execution. During this period of time, it is possible to access the interrupt controller with a software IACK to see if there are any pending properly-enabled requests. Checking for any pending interrupt requests at this time provides ability to initiate processing of another interrupt without the need to return from the original and incur the overhead of another interrupt exception.

At the conclusion of segment G, the processor core returns to the original interrupted task or a different task ready to execute.

Obviously, there are many variations to the managing of the SR[I] and the CLMASK values to create a flexible, responsive system for managing interrupt requests within the device.

Chapter 15

Edge Port Module (EPORT)

15.1 Introduction

The edge port module (EPORT) has eight interrupt pins, $\overline{\text{IRQ}}7 - \overline{\text{IRQ}}0$. Each pin can be configured individually as a level-sensitive interrupt pin, an edge-detecting interrupt pin (rising edge, falling edge, or both), or a general-purpose input/output (I/O) pin.

NOTE

Not all EPORT signals may be output from the device. See [Chapter 2, “Signal Descriptions,”](#) to determine which signals are available.

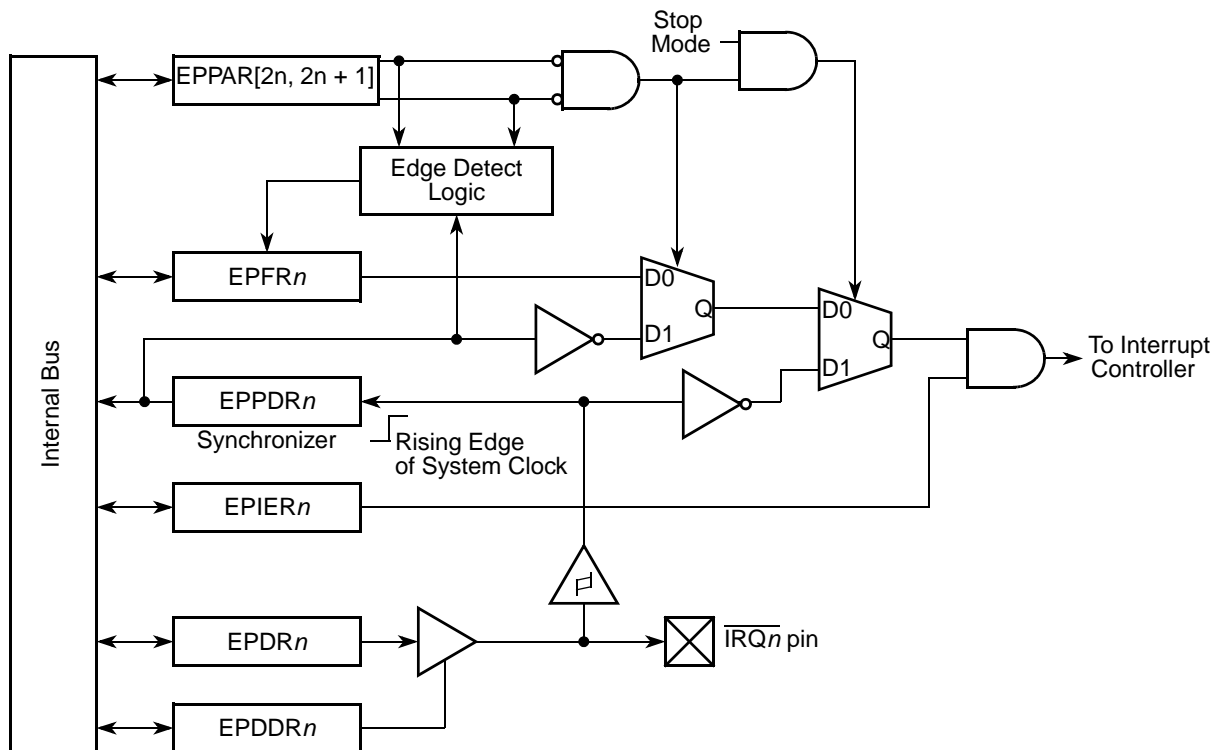


Figure 15-1. EPORT Block Diagram

NOTE

The GPIO module must be configured to enable the peripheral function of the appropriate pins (refer to [Chapter 13, “General Purpose I/O Module”](#)) prior to configuring the edge-port module.

15.2 Low-Power Mode Operation

This section describes the operation of the EPORT module in low-power modes. For more information on low-power modes, see [Chapter 8, “Power Management”](#). [Table 15-1](#) shows EPORT-module operation in low-power modes and describes how this module may exit each mode.

NOTE

The wakeup control register (WCR) in the system control module specifies the interrupt level at or above what is needed to bring the device out of a low-power mode.

Table 15-1. Edge Port Module Operation in Low-Power Modes

Low-power Mode	EPORT Operation	Mode Exit
Wait	Normal	Any \overline{IRQn} interrupt at or above level in WCR
Doze	Normal	Any \overline{IRQn} interrupt at or above level in WCR
Stop	Level-sensing only	Any \overline{IRQn} interrupt set for level-sensing at or above level in WCR. See note below.

In wait and doze modes, the EPORT module continues to operate as it does in run mode. It may be configured to exit the low-power modes by generating an interrupt request on a selected edge or a low level on an external pin. In stop mode, no clocks are available to perform the edge-detect function. Only the level-detect logic is active (if configured) to allow any low level on the external interrupt pin to generate an interrupt (if enabled) to exit stop mode.

NOTE

In stop mode, the input pin synchronizer is bypassed for the level-detect logic because no clocks are available.

15.3 Interrupt/GPIO Pin Descriptions

All EPORT pins default to general-purpose input pins at reset. The pin value is synchronized to the rising edge of FB_CLK when read from the EPORT pin data register (EPPDR). The values used in the edge/level detect logic are also synchronized to the rising edge of FB_CLK. These pins use Schmitt-triggered input buffers with built-in hysteresis designed to decrease the probability of generating false, edge-triggered interrupts for slow rising and falling input signals.

When a pin is configured as an output, it is driven to a state whose level is determined by the corresponding bit in the EPORT data register (EPDR). All bits in the EPDR are set at reset.

15.4 Memory Map/Register Definition

This subsection describes the memory map and register structure. Refer to [Table 15-2](#) for a description of the EPORT memory map.

NOTE

Longword accesses to any of the edge-port registers result in a bus error.
Only byte and word accesses are allowed.

Table 15-2. Edge Port Module Memory Map

Address	Register	Width (bits)	Access	Reset Value	Section/Page
Supervisor Access Only Registers¹					
0xFC08_8000	EPORT Pin Assignment Register (EPPAR)	16	R/W	0x0000	15.4.1/15-3
0xFC08_8002	EPORT Data Direction Register (EPDDR)	8	R/W	0x00	15.4.2/15-4
0xFC08_8003	EPORT Interrupt Enable Register (EPIER)	8	R/W	0x00	15.4.3/15-5
Supervisor/User Access Registers					
0xFC08_8004	EPORT Data Register (EPDR)	8	R/W	0xFF	15.4.4/15-5
0xFC08_8005	EPORT Pin Data Register (EPPDR)	8	R	See Section	15.4.5/15-5
0xFC08_8006	EPORT Flag Register (EPFR)	8	R/W	0x00	15.4.6/15-6

¹ User access to supervisor-only address locations have no effect and result in a bus error.

15.4.1 EPORT Pin Assignment Register (EPPAR)

The EPORT pin assignment register (EPPAR) controls the function of each pin individually.

: 0xFC08_8000 (EPPAR)												Access: Supervisor read/write																				
	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0																
R	EPPA7				EPPA6				EPPA5				EPPA4				EPPA3				EPPA2				EPPA1				EPPA0			
W																																
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0				

Figure 15-2. EPORT Pin Assignment Register (EPPAR)

Table 15-3. EPPAR Field Descriptions

Field	Description
15–0 EPPAn	<p>EPORT pin assignment select fields. The read/write EPPAn fields configure EPORT pins for level detection and rising and/or falling edge detection.</p> <p>Pins configured as level-sensitive are active-low (logic 0 on the external pin represents a valid interrupt request). Level-sensitive interrupt inputs are not latched. To guarantee that a level-sensitive interrupt request is acknowledged, the interrupt source must keep the signal asserted until acknowledged by software. Level sensitivity must be selected to bring the device out of stop mode with an \overline{IRQn} interrupt.</p> <p>Pins configured as edge-triggered are latched and need not remain asserted for interrupt generation. A pin configured for edge detection can trigger an interrupt regardless of its configuration as input or output.</p> <p>Interrupt requests generated in the EPORT module can be masked by the interrupt controller module. EPPAR functionality is independent of the selected pin direction.</p> <p>Reset clears the EPPAn fields.</p> <p>00 Pin \overline{IRQn} level-sensitive 01 Pin \overline{IRQn} rising edge triggered 10 Pin \overline{IRQn} falling edge triggered 11 Pin \overline{IRQn} falling edge and rising edge triggered</p>

15.4.2 EPORT Data Direction Register (EPDDR)

The EPORT data direction register (EPDDR) controls the direction of each one of the pins individually.

Address: 0xFC08_8002 (EPDDR)

Access: Supervisor read/write

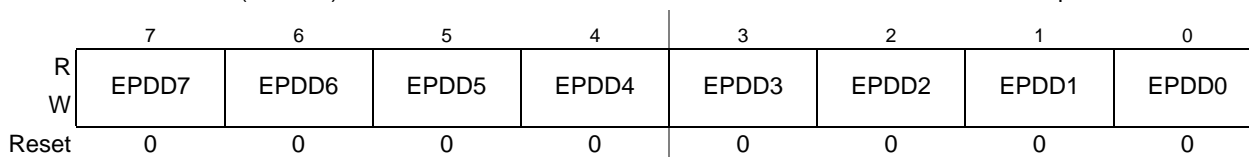


Figure 15-3. EPORT Data Direction Register (EPDDR)

Table 15-4. EPDDR Field Descriptions

Field	Description
7–0 EPDDn	<p>Setting any bit in the EPDDR configures the corresponding pin as an output. Clearing any bit in EPDDR configures the corresponding pin as an input. Pin direction is independent of the level/edge detection configuration. Reset clears EPDD7–EPDD0.</p> <p>To use an EPORT pin as an external interrupt request source, its corresponding bit in EPDDR must be clear.</p> <p>Software can generate interrupt requests by programming the EPORT data register when the EPDDR selects output.</p> <p>0 Corresponding EPORT pin configured as input 1 Corresponding EPORT pin configured as output</p>

15.4.3 Edge Port Interrupt Enable Register (EPIER)

The EPORT interrupt enable register (EPIER) enables interrupt requests for each pin individually.

Address: 0xFC08_8003 (EPIER)

Access: User read/write

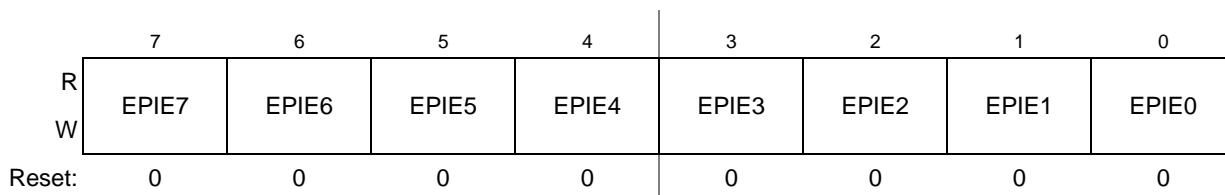


Figure 15-4. EPORT Port Interrupt Enable Register (EPIER)

Table 15-5. EPIER Field Descriptions

Field	Description
7–0 EPIEn	<p>Edge port interrupt enable bits enable EPORT interrupt requests. If a bit in EPIER is set, EPORT generates an interrupt request when:</p> <ul style="list-style-type: none"> The corresponding bit in the EPORT flag register (EPFR) is set or later becomes set. The corresponding pin level is low and the pin is configured for level-sensitive operation. <p>Clearing a bit in EPIER negates any interrupt request from the corresponding EPORT pin. Reset clears EPIE7 – EPIE0.</p> <p>0 Interrupt requests from corresponding EPORT pin disabled 1 Interrupt requests from corresponding EPORT pin enabled</p>

15.4.4 Edge Port Data Register (EPDR)

The EPORT data register (EPDR) holds the data to be driven to the pins.

Address: 0xFC08_8004 (EPDR)

Access: User read/write

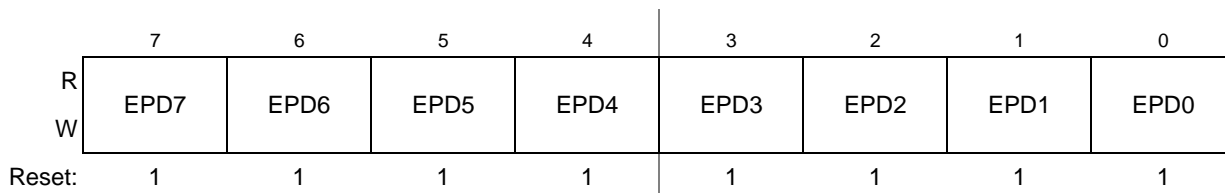


Figure 15-5. EPORT Port Data Register (EPDR)

Table 15-6. EPDR Field Descriptions

Field	Description
7–0 EPDn	<p>Edge port data bits. An internal register stores data written to EPDR; if any pin of the port is configured as an output, the bit stored for that pin is driven onto the pin. Reading EPDR returns the data stored in the register. Reset sets EPD7 – EPD0.</p>

15.4.5 Edge Port Pin Data Register (EPPDR)

The EPORT pin data register (EPPDR) reflects the current state of the pins.

Address: 0xFC08_8005 (EPPDR)

Access: User read-only

	7	6	5	4	3	2	1	0
R	EPPD7	EPPD6	EPPD5	EPPD4	EPPD3	EPPD2	EPPD1	EPPD0
W								
Reset:	$\overline{\text{IRQ7}}$	$\overline{\text{IRQ6}}$	$\overline{\text{IRQ5}}$	$\overline{\text{IRQ4}}$	$\overline{\text{IRQ3}}$	$\overline{\text{IRQ2}}$	$\overline{\text{IRQ1}}$	$\overline{\text{IRQ0}}$

Figure 15-6. EPORT Port Pin Data Register (EPPDR)

Table 15-7. EPPDR Field Descriptions

Field	Description
7–0 EPPD n	Edge port pin data bits. The read-only EPPDR reflects the current state of the EPORT pins $\overline{\text{IRQ7}}$ – $\overline{\text{IRQ0}}$. Writing to EPPDR has no effect, and the write cycle terminates normally. Reset does not affect EPPDR.

15.4.6 Edge Port Flag Register (EPFR)

The EPORT flag register (EPFR) individually latches EPORT edge events.

Address: 0xFC08_8006 (EPFR)

Access: User read/write

	7	6	5	4	3	2	1	0
R	EPF7	EPF6	EPF5	EPF4	EPF3	EPF2	EPF1	EPF0
W								
Reset:	0	0	0	0	0	0	0	0

Figure 15-7. EPORT Port Flag Register (EPFR)

Table 15-8. EPFR Field Descriptions

Field	Description
7–0 EPF n	<p>Edge port flag bits. When an EPORT pin is configured for edge triggering, its corresponding read/write bit in EPFR indicates that the selected edge has been detected. Reset clears EPF7 – EPF0.</p> <p>Bits in this register are set when the selected edge is detected on the corresponding pin. A bit remains set until cleared by writing a 1 to it. Writing 0 has no effect. If a pin is configured as level-sensitive (EPPARn = 00), pin transitions do not affect this register.</p> <p>0 Selected edge for $\overline{\text{IRQ}n}$ pin has not been detected.</p> <p>1 Selected edge for $\overline{\text{IRQ}n}$ pin has been detected.</p>

Chapter 16

Enhanced Direct Memory Access (eDMA)

16.1 Overview

The enhanced direct memory access (eDMA) controller is a second-generation module capable of performing complex data transfers with minimal intervention from a host processor. The hardware microarchitecture includes a DMA engine that performs source- and destination-address calculations, and the actual data-movement operations, along with local memory containing transfer control descriptors for each channel.

16.2 Block Diagram

Figure 16-1 is a block diagram of the eDMA module.

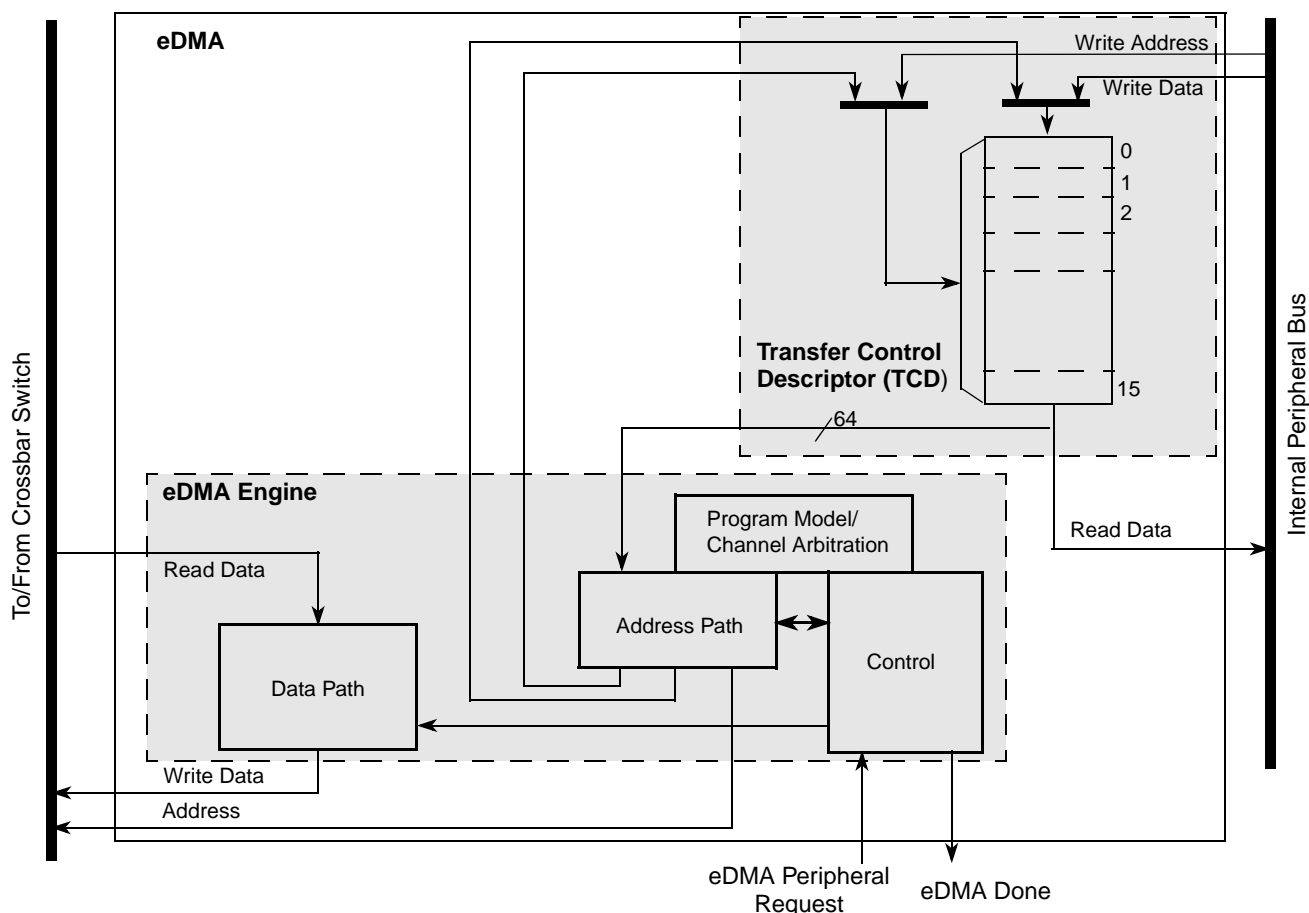


Figure 16-1. eDMA Block Diagram

16.3 Features

The eDMA is a highly-programmable data-transfer engine optimized to minimize the required intervention from the host processor. It is intended for use in applications where the data size to be transferred is statically known and not defined within the data packet itself. The eDMA module features:

- All data movement via dual-address transfers: read from source, write to destination
 - Programmable source and destination addresses and transfer size, plus support for enhanced addressing modes
- 16-channel implementation that performs complex data transfers with minimal intervention from a host processor
 - Internal data buffer, used as temporary storage to support 16-byte burst transfers
 - Connections to the crossbar switch for bus mastering the data movement
- Transfer control descriptor (TCD) organized to support two-deep, nested transfer operations
 - 32-byte TCD stored in local memory for each channel
 - An inner data transfer loop defined by a minor byte transfer count
 - An outer data transfer loop defined by a major iteration count
- Channel activation via one of three methods:
 - Explicit software initiation
 - Initiation via a channel-to-channel linking mechanism for continual transfers
 - Peripheral-paced hardware requests (one per channel)
- Support for fixed-priority and round-robin channel arbitration
- Channel completion reported via optional interrupt requests
 - One interrupt per channel, optionally asserted at completion of major iteration count
 - Error terminations are optionally enabled per channel and logically summed together to form one error interrupt to the interrupt controller
- Optional support for scatter/gather DMA processing

Throughout this chapter, *n* is used to reference the channel number.

16.4 Modes of Operation

16.4.1 Normal Mode

In normal mode, the eDMA transfers data between a source and a destination. The source and destination can be a memory block or an I/O block capable of operation with the eDMA.

A service request initiates a transfer of a specific number of bytes (NBYTES) as specified in the transfer control descriptor (TCD). The minor loop is the sequence of read-write operations that transfers these NBYTES per service request. A major loop is the number of minor loop iterations defining a task.

16.4.2 Debug Mode

In debug mode, the eDMA stops transferring data. If debug mode is entered during the transfer of a data block described by a minor loop in the current active channel's TCD, the eDMA continues operation until completion of the minor loop.

16.5 External Signal Description

This section describes the external signals of the eDMA controller.

Table 16-1. External Signal List

Signal Name	I/O	Description
$\overline{\text{DREQ0}}$	I	Provides external requests from peripherals needing DMA service. When asserted, the device is requesting service. This request pin is tied to DMA channel 0.
$\overline{\text{DACK0}}$	O	Indicates when the external DMA request has been acknowledged.

16.5.1 External Signal Timing

Asserting the external DMA request signal, $\overline{\text{DREQn}}$, initiates a service request for that channel. It must remain asserted until the corresponding $\overline{\text{DACKn}}$ signal indicates the channel's data transfer has started. The $\overline{\text{DACKn}}$ output is asserted for one cycle during the address phase of the channel's first internal read access.

- When no further requests are needed, the $\overline{\text{DREQn}}$ signal must negate after the $\overline{\text{DACKn}}$ assertion and on or before the second cycle following the data phase of the last internal bus write (see [Figure 16-2](#)).
- If another service request is needed, $\overline{\text{DREQn}}$ may simply remain asserted.
- To request continuous service, $\overline{\text{DREQn}}$ may remain continuously asserted.

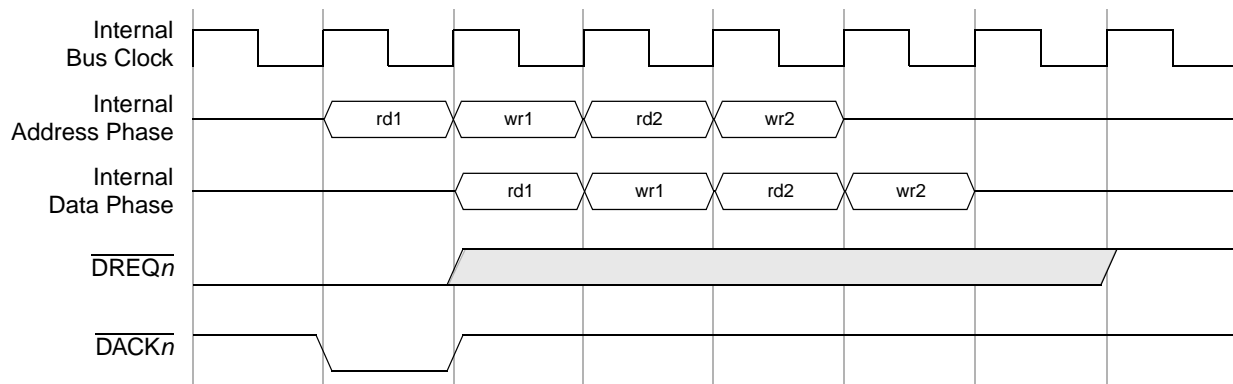


Figure 16-2. $\overline{\text{DREQn}}$ and $\overline{\text{DACKn}}$ Timing

After a service request has been initiated, it cannot be canceled. Removing a service request after it has been asserted may result in one of three actions depending on the DMA engine's status:

- The request is never recognized because another channel is executing.

- The request is considered spurious and discarded, because the request is removed during arbitration for next channel selection.
- The channel is selected by arbitration and begins execution.

16.6 Memory Map/Register Definition

The eDMA's programming model is partitioned into two regions: the first region defines a number of registers providing control functions, while the second region corresponds to the local transfer control descriptor memory.

Reading reserved bits in a register return the value of zero and writes to reserved bits in a register are ignored. Reading or writing to a reserved memory location generates a bus error.

Table 16-2. eDMA Controller Memory Map

Address	Register	Width (bits)	Access	Reset Value	Section/Page
0xFC04_4000	eDMA Control Register (EDMA_CR)	32	R/W	0x0000_0000	16.6.1/16-4
0xFC04_4004	eDMA Error Status Register (EDMA_ES)	32	R	0x0000_0000	16.6.2/16-5
0xFC04_400E	eDMA Enable Request Register (EDMA_ERQ)	16	R/W	0x0000	16.6.3/16-8
0xFC04_4016	eDMA Enable Error Interrupt Register (EDMA_EEI)	16	R/W	0x0000	16.6.4/16-9
0xFC04_4018	eDMA Set Enable Request (EDMA_SERQ)	8	W	0x00	16.6.5/16-9
0xFC04_4019	eDMA Clear Enable Request (EDMA_CERQ)	8	W	0x00	16.6.6/16-10
0xFC04_401A	eDMA Set Enable Error Interrupt Register (EDMA_SEEI)	8	W	0x00	16.6.7/16-11
0xFC04_401B	eDMA Clear Enable Error Interrupt Register (EDMA_CEEI)	8	W	0x00	16.6.8/16-11
0xFC04_401C	eDMA Clear Interrupt Request Register (EDMA_CINT)	8	W	0x00	16.6.9/16-12
0xFC04_401D	eDMA Clear Error Register (EDMA_CERR)	8	W	0x00	16.6.10/16-13
0xFC04_401E	eDMA Set START Bit Register (EDMA_SSRT)	8	W	0x00	16.6.11/16-13
0xFC04_401F	eDMA Clear DONE Status Bit Register (EDMA_CDNE)	8	W	0x00	16.6.12/16-14
0xFC04_4026	eDMA Interrupt Request Register (EDMA_INT)	32	R/W	0x0000	16.6.13/16-15
0xFC04_402E	eDMA Error Register (EDMA_ERR)	32	R/W	0x0000	16.6.14/16-15
0xFC04_4100 + hex(<i>n</i>)	eDMA Channel <i>n</i> Priority Register (DCHPRIn) for <i>n</i> = 0 – 15	8	R/W	See Section	16.6.15/16-16
0xFC04_5000 + hex(32× <i>n</i>)	Transfer Control Descriptor (TCD <i>n</i>) for <i>n</i> = 0 – 15	256	R/W	See Section	16.6.16/16-17

16.6.1 eDMA Control Register (EDMA_CR)

The EDMA_CR defines the basic operating configuration of the eDMA. Arbitration can be configured to use a fixed-priority or a round-robin scheme. In fixed-priority arbitration, the highest priority channel requesting service is selected to execute. The channel priority registers assign the priorities (see [Section 16.6.15, “eDMA Channel *n* Priority Registers \(DCHPRIn\)”](#)). In round-robin arbitration mode, the channel priorities are ignored, and channels are cycled through without regard to priority.

NOTE

For proper operation, writes to the EDMA_CR register must only be performed when the DMA channels are inactive (TCR_n_CSR[ACTIVE] bits are cleared).

Address: 0xFC04_4000 (EDMA_CR)

Access: User read/write

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
R	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
W																
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	0	0	0	0	0	0	0	0	0	0	0	0	0	ERCA	EDBG	0
W																
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Figure 16-3. eDMA Control Register (EDMA_CR)**Table 16-3. eDMA_CR Field Descriptions**

Field	Description
31–3	Reserved, must be cleared.
2 ERCA	Enable round robin channel arbitration. 0 Fixed priority arbitration is used for channel selection. 1 Round robin arbitration is used for channel selection.
1 EDBG	Enable debug. 0 When in debug mode the DMA continues to operate. 1 When in debug mode, the eDMA stalls the start of a new channel. Executing channels are allowed to complete. Channel execution resumes when the system exits debug mode or the EDBG bit is cleared.
0	Reserved, must be cleared.

16.6.2 eDMA Error Status Register (EDMA_ES)

The EDMA_ES provides information concerning the last recorded channel error. Channel errors can be caused by a configuration error (an illegal setting in the transfer-control descriptor or an illegal priority register setting in fixed-arbitration mode) or an error termination to a bus master read or write cycle.

A configuration error is reported when the starting source or destination address, source or destination offsets, minor loop byte count, or the transfer size represent an inconsistent state. Each of these possible causes are detailed in the below list:

- The addresses and offsets must be aligned on 0-modulo-transfer-size boundaries
- The minor loop byte count must be a multiple of the source and destination transfer sizes.
- All source reads and destination writes must be configured to the natural boundary of the programmed transfer size respectively.

- In fixed arbitration mode, a configuration error is caused by any two channel priorities being equal. All channel priority levels must be unique when fixed arbitration mode is enabled.
- If a scatter/gather operation is enabled upon channel completion, a configuration error is reported if the scatter/gather address (DLAST_SGA) is not aligned on a 32-byte boundary.
- If minor loop channel linking is enabled upon channel completion, a configuration error is reported when the link is attempted if the TCD_n_CITER[E_LINK] bit does not equal the TCD_n_BITER[E_LINK] bit.

If enabled, all configuration error conditions, except the scatter/gather and minor-loop link errors, report as the channel activates and asserts an error interrupt request. A scatter/gather configuration error is reported when the scatter/gather operation begins at major loop completion when properly enabled. A minor loop channel link configuration error is reported when the link operation is serviced at minor loop completion.

If a system bus read or write is terminated with an error, the data transfer is stopped and the appropriate bus error flag set. In this case, the state of the channel's transfer control descriptor is updated by the eDMA engine with the current source address, destination address and current iteration count at the point of the fault. When a system-bus error occurs, the channel terminates after the read or write transaction (which is already pipelined after errant access) has completed. If a bus error occurs on the last read prior to beginning the write sequence, the write executes using the data captured during the bus error. If a bus error occurs on the last write prior to switching to the next read sequence, the read sequence executes before the channel terminates due to the destination bus error.

The occurrence of any error causes the eDMA engine to stop the active channel immediately, and the appropriate channel bit in the eDMA error register is asserted. At the same time, the details of the error condition are loaded into the EDMA_ES. The major loop complete indicators, setting the transfer control descriptor DONE flag and the possible assertion of an interrupt request, are not affected when an error is detected. After the error status has been updated, the eDMA engine continues operating by servicing the next appropriate channel. A channel that experiences an error condition is not automatically disabled. If a channel is terminated by an error and then issues another service request before the error is fixed, that channel executes and terminate with the same error condition.

Address: 0xFC04_4004 (EDMA_ES)

Access: User read-only

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
R	VLD	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
W																
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	0	CPE	0	0	ERRCHN				SAE	SOE	DAE	DOE	NCE	SGE	SBE	DBE
W																
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Figure 16-4. eDMA Error Status Register (EDMA_ES)

Table 16-4. EDMA_ES Field Descriptions

Field	Description
31 VLD	Logical OR of all EDMA_ERR status bits. 0 No EDMA_ERR bits are set. 1 At least one EDMA_ERR bit is set indicating a valid error exists that has not been cleared.
30–15	Reserved, must be cleared.
14 CPE	Channel priority error 0 No channel priority error. 1 The last recorded error was a configuration error in the channel priorities. Channel priorities are not unique.
13–12	Reserved, must be cleared.
11–8 ERRCHN	Error channel number. The channel number of the last recorded error. (excluding CPE errors)
7 SAE	Source address error. 0 No source address configuration error. 1 The last recorded error was a configuration error detected in the TCD _n _SADDR field. TCD _n _SADDR is inconsistent with TCD _n _ATTR[SSIZE]
6 SOE	Source offset error. 0 No source offset configuration error. 1 The last recorded error was a configuration error detected in the TCD _n _SOFF field. TCD _n _SOFF is inconsistent with TCD _n _ATTR[SSIZE].
5 DAE	Destination address error. 0 No destination address configuration error. 1 The last recorded error was a configuration error detected in the TCD _n _DADDR field. TCD _n _DADDR is inconsistent with TCD _n _ATTR[DSIZE].
4 DOE	Destination offset error. 0 No destination offset configuration error. 1 The last recorded error was a configuration error detected in the TCD _n _DOFF field. TCD _n _DOFF is inconsistent with TCD _n _ATTR[DSIZE].
3 NCE	NBYTES/CITER configuration error. 0 No NBYTES/CITER configuration error. 1 The last recorded error was a configuration error detected in the TCD _n _NBYTES or TCD _n _CITER fields. <ul style="list-style-type: none"> • TCD_n_NBYTES is not a multiple of TCD_n_ATTR[SSIZE] and TCD_n_ATTR[DSIZE], or • TCD_n_CITER[CITER] is equal to zero, or • TCD_n_CITER[E_LINK] is not equal to TCD_n_BITER[E_LINK].
2 SGE	Scatter/gather configuration error. 0 No scatter/gather configuration error. 1 The last recorded error was a configuration error detected in the TCD _n _DLAST_SGA field. This field is checked at the beginning of a scatter/gather operation after major loop completion if TCD _n _CSR[E_SG] is enabled. TCD _n _DLAST_SGA is not on a 32 byte boundary.
1 SBE	Source bus error. 0 No source bus error. 1 The last recorded error was a bus error on a source read.
0 DBE	Destination bus error. 0 No destination bus error. 1 The last recorded error was a bus error on a destination write.

16.6.3 eDMA Enable Request Register (EDMA_ERQ)

The EDMA_ERQ register provides a bit map for the 16 implemented channels to enable the request signal for each channel. The state of any given channel enable is directly affected by writes to this register; it is also affected by writes to the EDMA_SERQ and EDMA_CERQ. The EDMA_{S,C}ERQR are provided so the request enable for a single channel can easily be modified without needing to perform a read-modify-write sequence to the EDMA_ERQ.

DMA request input signals and this enable request flag must be asserted before a channel's hardware service request is accepted. The state of the eDMA enable request flag does not affect a channel service request made explicitly through software or a linked channel request.

Address: 0xFC04_400E (EDMA_ERQ)

Access: User read/write

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	ERQ	ERQ	ERQ	ERQ	ERQ	ERQ	ERQ	ERQ	ERQ	ERQ	ERQ	ERQ	ERQ	ERQ	ERQ	ERQ
W	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Figure 16-5. eDMA Enable Request Register (EDMA_ERQ)

Table 16-5. EDMA_ERQ Field Descriptions

Field	Description
15–0 ERQ _n	Enable DMA Request <i>n</i> . 0 The DMA request signal for channel <i>n</i> is disabled. 1 The DMA request signal for channel <i>n</i> is enabled.

The assignments between the DMA requests from the peripherals to the channels of the eDMA are shown in [Table 16-6](#).

Table 16-6. DMA Request Summary for eDMA

Channel	Source	Description
0	$\overline{\text{DREQ0}}$	External DMA request 0
1	UISR0[FFULL/RXRDY]	UART0 Receive
2	UISR0[TXRDY]	UART0 Transmit
3	UISR1[FFULL/RXRDY]	UART1 Receive
4	UISR1[TXRDY]	UART1 Transmit
5	UISR2[FFULL/RXRDY]	UART2 Receive
6	UISR2[TXRDY]	UART2 Transmit
7	DTER0[CAP] or DTER0[REF]	Timer 0
8	DTER1[CAP] or DTER1[REF]	Timer 1
9	DTER2[CAP] or DTER2[REF]	Timer 2

Table 16-6. DMA Request Summary for eDMA (continued)

Channel	Source	Description
10	DTER3[CAP] or DTER3[REF]	Timer 3
11–15	Software Activated	Activated explicitly by setting the TCD _n _CSR[START] bit

As a given channel completes the processing of its major iteration count, a flag in the transfer control descriptor that affect the ending state of the EDMA_ERQ bit for that channel. If the TCD_n_CSR[D_REQ] bit is set, the corresponding EDMA_ERQ bit is cleared, disabling the DMA request. If the D_REQ bit clears, the state of the EDMA_ERQ bit is unaffected.

16.6.4 eDMA Enable Error Interrupt Registers (EDMA_EEI)

The EDMA_EEI register provides a bit map for the 16 channels to enable the error interrupt signal for each channel. The state of any given channel's error interrupt enable is directly affected by writes to this register; it is also affected by writes to the EDMA_SEEI and EDMA_CEEI. The EDMA_{S,C}EEIR are provided so the error interrupt enable for a single channel can easily be modified without the need to perform a read-modify-write sequence to the EDMA_EEI register.

The DMA error indicator and the error interrupt enable flag must be asserted before an error interrupt request for a given channel is asserted to the interrupt controller.

Address: 0xFC04_4016 (EDMA_EEI)

Access: User read/write

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	EEI15	EEI14	EEI13	EEI12	EEI11	EEI10	EEI9	EEI8	EEI7	EEI6	EEI5	EEI4	EEI3	EEI2	EEI1	EEI0
W																
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Figure 16-6. eDMA Enable Error Interrupt Register (EDMA_EEI)

Table 16-7. EDMA_EEI Field Descriptions

Field	Description
15–0 EEIn	Enable error interrupt <i>n</i> . 0 The error signal for channel <i>n</i> does not generate an error interrupt. 1 The assertion of the error signal for channel <i>n</i> generates an error interrupt request.

16.6.5 eDMA Set Enable Request Register (EDMA_SERQ)

The EDMA_SERQ provides a simple memory-mapped mechanism to set a given bit in the EDMA_ERQ to enable the DMA request for a given channel. The data value on a register write causes the corresponding bit in the EDMA_ERQ to be set. Setting the SAER bit provides a global set function, forcing the entire contents of EDMA_ERQ to be set. Reads of this register return all zeroes.

Address: 0xFC04_4018 (EDMA_SERQ)

Access: User write-only

	7	6	5	4	3	2	1	0
R	0	0	0	0	0	0	0	0
W		SAER			SERQ			
Reset	0	0	0	0	0	0	0	0

Figure 16-7. eDMA Set Enable Request Register (EDMA_SERQ)

Table 16-8. EDMA_SERQ Field Descriptions

Field	Description
7	Reserved, must be cleared.
6 SAER	Set all enable requests. 0 Set only those EDMA_ERQ bits specified in the SERQ field. 1 Set all bits in EDMA_ERQ.
5–4	Reserved, must be cleared.
3–0 SERQ	Set enable request. Sets the corresponding bit in EDMA_ERQ

16.6.6 eDMA Clear Enable Request Register (EDMA_CERQ)

The EDMA_CERQ provides a simple memory-mapped mechanism to clear a given bit in the EDMA_ERQ to disable the DMA request for a given channel. The data value on a register write causes the corresponding bit in the EDMA_ERQ to be cleared. Setting the CAER bit provides a global clear function, forcing the entire contents of the EDMA_ERQ to be cleared, disabling all DMA request inputs. Reads of this register return all zeroes.

Address: 0xFC04_4019 (EDMA_CERQ)

Access: User write-only

	7	6	5	4	3	2	1	0
R	0	0	0	0	0	0	0	0
W		CAER			CERQ			
Reset	0	0	0	0	0	0	0	0

Figure 16-8. eDMA Clear Enable Request Register (EDMA_CERQ)

Table 16-9. EDMA_CERQ Field Descriptions

Field	Description
7	Reserved, must be cleared.
6 CAER	Clear all enable requests. 0 Clear only those EDMA_ERQ bits specified in the CERQ field. 1 Clear all bits in EDMA_ERQ.

Table 16-9. EDMA_CERQ Field Descriptions (continued)

Field	Description
5–4	Reserved, must be cleared.
3–0 CERQ	Clear enable request. Clears the corresponding bit in EDMA_ERQ.

16.6.7 eDMA Set Enable Error Interrupt Register (EDMA_SEEI)

The EDMA_SEEI provides a simple memory-mapped mechanism to set a given bit in the EDMA_EEI to enable the error interrupt for a given channel. The data value on a register write causes the corresponding bit in the EDMA_EEI to be set. Setting the SAEE bit provides a global set function, forcing the entire EDMA_EEI contents to be set. Reads of this register return all zeroes.

Address: 0xFC04_401A (EDMA_SEEI)

Access: User write-only

	7	6	5	4	3	2	1	0
R	0	0	0	0	0	0	0	0
W		SAEE			SEEI			
Reset	0	0	0	0	0	0	0	0

Figure 16-9. eDMA Set Enable Error Interrupt Register (EDMA_SEEI)

Table 16-10. EDMA_SEEI Field Descriptions

Field	Description
7	Reserved, must be cleared.
6 SAEE	Sets all enable error interrupts. 0 Set only those EDMA_EEI bits specified in the SEEI field. 1 Sets all bits in EDMA_EEI.
5–4	Reserved, must be cleared.
3–0 SEEI	Set enable error interrupt. Sets the corresponding bit in EDMA_EEI.

16.6.8 eDMA Clear Enable Error Interrupt Register (EDMA_CEEI)

The EDMA_CEEI provides a simple memory-mapped mechanism to clear a given bit in the EDMA_EEI to disable the error interrupt for a given channel. The data value on a register write causes the corresponding bit in the EDMA_EEI to be cleared. Setting the CAEE bit provides a global clear function, forcing the EDMA_EEI contents to be cleared, disabling all DMA request inputs. Reads of this register return all zeroes.

Address: 0xFC04_401B (EDMA_CEEI)

Access: User write-only

	7	6	5	4	3	2	1	0
R	0	0	0	0	0	0		
W		CAEE			CEEI			
Reset	0	0	0	0	0	0	0	0

Figure 16-10. eDMA Clear Enable Error Interrupt Register (EDMA_CEEI)

Table 16-11. EDMA_CEEI Field Descriptions

Field	Description
7	Reserved, must be cleared.
6 CAEE	Clear all enable error interrupts. 0 Clear only those EDMA_EEI bits specified in the CEEI field. 1 Clear all bits in EDMA_EEI.
5–4	Reserved, must be cleared.
3–0 CEEI	Clear enable error interrupt. Clears the corresponding bit in EDMA_EEI.

16.6.9 eDMA Clear Interrupt Request Register (EDMA_CINT)

The EDMA_CINT provides a simple, memory-mapped mechanism to clear a given bit in the EDMA_INT to disable the interrupt request for a given channel. The given value on a register write causes the corresponding bit in the EDMA_INT to be cleared. Setting the CAIR bit provides a global clear function, forcing the entire contents of the EDMA_INT to be cleared, disabling all DMA interrupt requests. Reads of this register return all zeroes.

Address: 0xFC04_401C (EDMA_CINT)

Access: User write-only

	7	6	5	4	3	2	1	0
R	0	0	0	0	0	0		
W		CAIR			CINT			
Reset	0	0	0	0	0	0	0	0

Figure 16-11. eDMA Clear Interrupt Request (EDMA_CINT)

Table 16-12. EDMA_CINT Field Descriptions

Field	Description
7	Reserved, must be cleared.
6 CAIR	Clear all interrupt requests. 0 Clear only those EDMA_INT bits specified in the CINT field. 1 Clear all bits in EDMA_INT.

Table 16-12. EDMA_CINT Field Descriptions (continued)

Field	Description
5–4	Reserved, must be cleared.
3–0 CINT	Clear interrupt request. Clears the corresponding bit in EDMA_INT.

16.6.10 eDMA Clear Error Register (EDMA_CERR)

The EDMA_CERR provides a simple memory-mapped mechanism to clear a given bit in the EDMA_ERR to disable the error condition flag for a given channel. The given value on a register write causes the corresponding bit in the EDMA_ERR to be cleared. Setting the CAEI bit provides a global clear function, forcing the EDMA_ERR contents to be cleared, clearing all channel error indicators. Reads of this register return all zeroes.

Address: 0xFC04_401D (EDMA_CERR)

Access: User write-only

	7	6	5	4	3	2	1	0
R	0	0	0	0	0	0	0	0
W		CAEI			CERR			
Reset	0	0	0	0	0	0	0	0

Figure 16-12. eDMA Clear Error Register (EDMA_CERR)

Table 16-13. EDMA_CERR Field Descriptions

Field	Description
7	Reserved, must be cleared.
6 CAEI	Clear all error indicators. 0 Clear only those EDMA_ERR bits specified in the CERR field. 1 Clear all bits in EDMA_ERR.
5–4	Reserved, must be cleared.
3–0 CERR	Clear error indicator. Clears the corresponding bit in EDMA_ERR.

16.6.11 eDMA Set START Bit Register (EDMA_SSRT)

The EDMA_SSRT provides a simple memory-mapped mechanism to set the START bit in the TCD of the given channel. The data value on a register write causes the START bit in the corresponding transfer control descriptor to be set. Setting the SAST bit provides a global set function, forcing all START bits to be set. Reads of this register return all zeroes.

Address: 0xFC04_401E (EDMA_SSRT)

Access: User write-only

	7	6	5	4	3	2	1	0
R	0	0	0	0	0	0	0	0
W		SAST			SSRT			
Reset	0	0	0	0	0	0	0	0

Figure 16-13. eDMA Set START Bit Register (EDMA_SSRT)

Table 16-14. EDMA_SSRT Field Descriptions

Field	Description
7	Reserved, must be cleared.
6 SAST	Set all START bits (activates all channels). 0 Set only those TCD _n _CSR[START] bits specified in the SSRT field. 1 Set all bits in TCD _n _CSR[START].
5–4	Reserved, must be cleared.
3–0 SSRT	Set START bit. Sets the corresponding bit in TCD _n _CSR[START].

16.6.12 eDMA Clear DONE Status Bit Register (EDMA_CDNE)

The EDMA_CDNE provides a simple memory-mapped mechanism to clear the DONE bit in the TCD of the given channel. The data value on a register write causes the DONE bit in the corresponding transfer control descriptor to be cleared. Setting the CADN bit provides a global clear function, forcing all DONE bits to be cleared. Reads of this register return all zeroes.

Address: 0xFC04_401F (EDMA_CDNE)

Access: User write-only

	7	6	5	4	3	2	1	0
R	0	0	0	0	0	0		
W		CADN			CDNE			
Reset	0	0	0	0	0	0	0	0

Figure 16-14. eDMA Clear DONE Status Bit Register (EDMA_CDNE)

Table 16-15. EDMA_CDNE Field Descriptions

Field	Description
7	Reserved, must be cleared.
6 CADN	Clears all DONE bits. 0 Clears only those TCD _n _CSR[DONE] bits specified in the CDNE field. 1 Clears all bits in TCD _n _CSR[DONE]
5–4	Reserved, must be cleared.
3–0 CDNE	Clear DONE bit. Clears the corresponding bit in TCD _n _CSR[DONE].

16.6.13 eDMA Interrupt Request Register (EDMA_INT)

The EDMA_INT provide a bit map for the 16 channels signaling the presence of an interrupt request for each channel. Depending on the appropriate bit setting in the transfer-control descriptions, the eDMA engine generates an interrupt a data transfer completion. The outputs of this register are directly routed to the interrupt controller (INTC). During the interrupt-service routine associated with any given channel, it is the software's responsibility to clear the appropriate bit, negating the interrupt request. Typically, a write to the EDMA_CINT in the interrupt service routine is used for this purpose.

The state of any given channel's interrupt request is directly affected by writes to this register; it is also affected by writes to the EDMA_CINT. On writes to the EDMA_INT, a 1 in any bit position clears the corresponding channel's interrupt request. A zero in any bit position has no affect on the corresponding channel's current interrupt status. The EDMA_CINT is provided so the interrupt request for a single channel can easily be cleared without the need to perform a read-modify-write sequence to the EDMA_INT.

Address: 0xFC04_4026 (EDMA_INT)

Access: User read/write

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	INT15	INT14	INT13	INT12	INT11	INT10	INT9	INT8	INT7	INT6	INT5	INT4	INT3	INT2	INT1	INT0
W	w1c	w1c	w1c	w1c	w1c	w1c	w1c	w1c	w1c	w1c	w1c	w1c	w1c	w1c	w1c	w1c
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Figure 16-15. eDMA Interrupt Request Register (EDMA_INT)

Table 16-16. EDMA_INT Field Descriptions

Field	Description
15–0 INT n	eDMA interrupt request n 0 The interrupt request for channel n is cleared. 1 The interrupt request for channel n is active.

16.6.14 eDMA Error Register (EDMA_ERR)

The EDMA_ERR provide a bit map for the 16 channels, signaling the presence of an error for each channel. The eDMA engine signals the occurrence of a error condition by setting the appropriate bit in this register. The outputs of this register are enabled by the contents of the EDMA_EEI, and then routed to the interrupt controller. During the execution of the interrupt-service routine associated with any DMA errors, it is software's responsibility to clear the appropriate bit, negating the error-interrupt request. Typically, a write to the EDMA_CERR in the interrupt-service routine is used for this purpose. The normal DMA channel completion indicators (setting the transfer control descriptor DONE flag and the possible assertion of an interrupt request) are not affected when an error is detected.

The contents of this register can also be polled because a non-zero value indicates the presence of a channel error regardless of the state of the EDMA_EEI. The state of any given channel's error indicators is affected by writes to this register; it is also affected by writes to the EDMA_CERR. On writes to the EDMA_ERR, a one in any bit position clears the corresponding channel's error status. A zero in any bit position has no affect on the corresponding channel's current error status. The EDMA_CERR is provided so the error indicator for a single channel can easily be cleared.

Address: 0xFC04_402E (EDMA_ERR)

Access: User read/write

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	ERR 15	ERR 14	ERR 13	ERR 12	ERR 11	ERR 10	ERR 9	ERR 8	ERR 7	ERR 6	ERR 5	ERR 4	ERR 3	ERR 2	ERR 1	ERR 0
W	w1c	w1c	w1c	w1c	w1c	w1c	w1c	w1c	w1c	w1c	w1c	w1c	w1c	w1c	w1c	w1c
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Figure 16-16. eDMA Error (EDMA_ERR) Register

Table 16-17. EDMA_ERR Field Descriptions

Field	Description
15–0 ERR n	eDMA Error n . 0 An error in channel n has not occurred. 1 An error in channel n has occurred.

16.6.15 eDMA Channel n Priority Registers (DCHPRI n)

When the fixed-priority channel arbitration mode is enabled (EDMA_CR[ERCA] = 0), the contents of these registers define the unique priorities associated with each channel. The channel priorities are evaluated by numeric value; for example, 0 is the lowest priority, 1 is the next higher priority, then 2, 3, etc. Software must program the channel priorities with unique values. Otherwise, a configuration error is reported. The range of the priority value is limited to the values of 0 through 15.

Channel preemption is enabled on a per-channel basis by setting the DCHPRI n [ECP] bit. Channel preemption allows the executing channel's data transfers to temporarily suspend in favor of starting a higher priority channel. After the preempting channel has completed all its minor loop data transfers, the preempted channel is restored and resumes execution. After the restored channel completes one read/write sequence, it is again eligible for preemption. If any higher priority channel is requesting service, the restored channel is suspended and the higher priority channel is serviced. Nested preemption (attempting to preempt a preempting channel) is not supported. After a preempting channel begins execution, it cannot be preempted. Preemption is available only when fixed arbitration is selected.

Address: 0xFC04_4100 + n , where $n = 0 - 15$ (DCHPRI n)

Access: User read/write

	7	6	5	4	3	2	1	0
R	ECP	0	0	0	CHPRI			
W								
Reset	0	0	0	0	–1	–1	–1	–1

¹ Reset value for the channel priority fields, CHPRI, is equal to the corresponding channel number for each priority register, i.e., DCHPRI15[CHPRI] equals 0b1111.

Figure 16-17. eDMA Channel n Priority Register (DCHPRI n)

Table 16-18. DCHPRIn Field Descriptions

Field	Description
7 ECP	Enable channel preemption. 0 Channel <i>n</i> cannot be suspended by a higher priority channel's service request. 1 Channel <i>n</i> can be temporarily suspended by the service request of a higher priority channel.
6–4	Reserved, must be cleared.
3–0 CHPRI	Channel <i>n</i> arbitration priority. Channel priority when fixed-priority arbitration is enabled.

16.6.16 Transfer Control Descriptors (TCDn)

Each channel requires a 32-byte transfer control descriptor for defining the desired data movement operation. The channel descriptors are stored in the local memory in sequential order: channel 0, channel 1,... channel 15. Each TCD_{*n*} definition is presented as 11 registers of 16 or 32 bits. [Table 16-19](#) is a register list of the basic TCD structure.

Table 16-19. TCDn Memory Structure

eDMA Offset	TCD _{<i>n</i>} Register Name	Abbreviation	Width (bits)
0xFC04_5000 + (0x20 × <i>n</i>)	Source Address	TCD _{<i>n</i>} _SADDR	32
0xFC04_5004 + (0x20 × <i>n</i>)	Transfer Attributes	TCD _{<i>n</i>} _ATTR	16
0xFC04_5006 + (0x20 × <i>n</i>)	Signed Source Address Offset	TCD _{<i>n</i>} _SOFF	16
0xFC04_5008 + (0x20 × <i>n</i>)	Minor Byte Count	TCD _{<i>n</i>} _NBYTES	32
0xFC04_500C + (0x20 × <i>n</i>)	Last Source Address Adjustment	TCD _{<i>n</i>} _SLAST	32
0xFC04_5010 + (0x20 × <i>n</i>)	Destination Address	TCD _{<i>n</i>} _DADDR	32
0xFC04_5014 + (0x20 × <i>n</i>)	Current Minor Loop Link, Major Loop Count	TCD _{<i>n</i>} _CITER	16
0xFC04_5016 + (0x20 × <i>n</i>)	Signed Destination Address Offset	TCD _{<i>n</i>} _DOFF	16
0xFC04_5018 + (0x20 × <i>n</i>)	Last Destination Address Adjustment/Scatter Gather Address	TCD _{<i>n</i>} _DLAST_SGA	32
0xFC04_501C + (0x20 × <i>n</i>)	Beginning Minor Loop Link, Major Loop Count	TCD _{<i>n</i>} _BITER	16
0xFC04_501E + (0x20 × <i>n</i>)	Control and Status	TCD _{<i>n</i>} _CSR	16

The following figures and tables define the fields of the TCD_{*n*} structure:

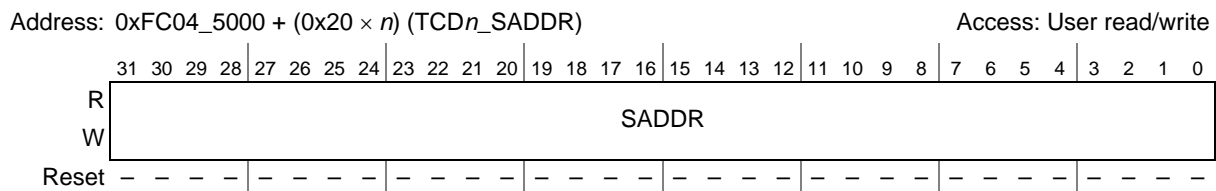
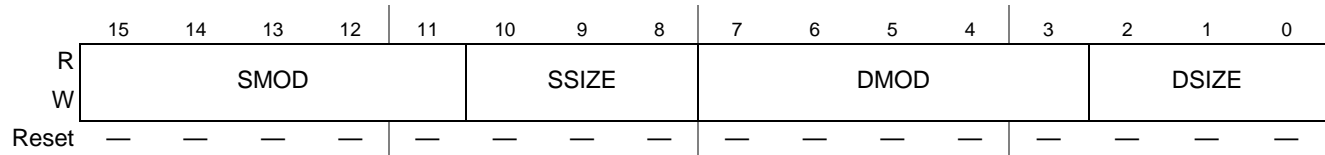
**Figure 16-18. TCD_{*n*} Source Address (TCD_{*n*}_SADDR)**

Table 16-20. TCD_n_SADDR Field Descriptions

Field	Description
31–0 SADDR	Source address. Memory address pointing to the source data.

Address: 0xFC04_5004 + (0x20 × *n*) (TCD_n_ATTR)

Access: User read/write

**Figure 16-19. TCD_n Transfer Attributes (TCD_n_ATTR)****Table 16-21. TCD_n_ATTR Field Descriptions**

Field	Description
15–11 SMOD	Source address modulo. 0 Source address modulo feature is disabled. non-0 This value defines a specific address range specified to be the value after SADDR + SOFF calculation is performed or the original register value. The setting of this field provides the ability to implement a circular data queue easily. For data queues requiring power-of-2 size bytes, the queue should start at a 0-modulo-size address and the SMOD field should be set to the appropriate value for the queue, freezing the desired number of upper address bits. The value programmed into this field specifies the number of lower address bits allowed to change. For a circular queue application, the SOFF is typically set to the transfer size to implement post-increment addressing with the SMOD function constraining the addresses to a 0-modulo-size range.
10–8 SSIZE	Source data transfer size. 000 8-bit 001 16-bit 010 32-bit 100 16-byte Else Reserved The attempted use of a Reserved encoding causes a configuration error.
7–3 DMOD	Destination address modulo. See the SMOD definition.
2–0 DSIZE	Destination data transfer size. See the SSIZE definition.

Address: 0xFC04_5006 + (0x20 × *n*) (TCD_n_SOFF)

Access: User read/write

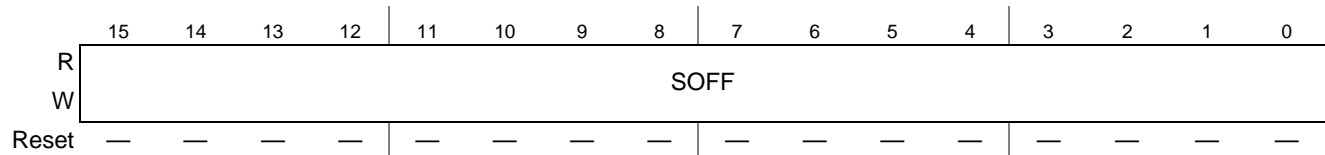
**Figure 16-20. TCD_n Signed Source Address Offset (TCD_n_SOFF)**

Table 16-22. TCDn_SOFF Field Descriptions

Field	Description
15–0 SOFF	Source address signed offset. Sign-extended offset applied to the current source address to form the next-state value as each source read is completed.

Address: 0xFC04_5008 + (0x20 × *n*) (TCD*n*_NBYTES)

Access: User read/write

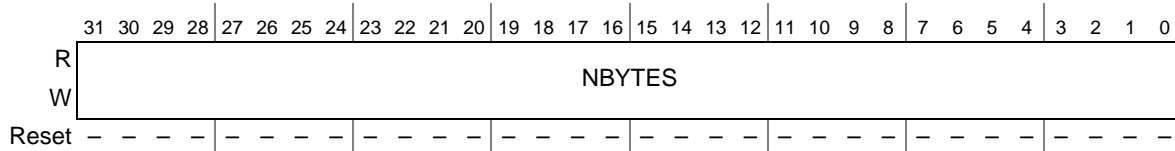


Figure 16-21. TCDn Minor Byte Count (TCDn_NBYTES)

Table 16-23. TCDn_NBYTES Field Descriptions

Field	Description
31–0 NBYTES	<p>Minor byte transfer count. Number of bytes to be transferred in each service request of the channel. As a channel activates, the appropriate TCD contents load into the eDMA engine, and the appropriate reads and writes perform until the minor byte transfer count has transferred. This is an indivisible operation and cannot be halted. (Although, it may be stalled by using the bandwidth control field, or via preemption.) After the minor count is exhausted, the SADDR and DADDR values are written back into the TCD memory, the major iteration count is decremented and restored to the TCD memory. If the major iteration count is completed, additional processing is performed.</p> <p>Note: An NBYTES value of 0x0000_0000 is interpreted as a 4 GB transfer.</p>

Address: 0xFC04_500C + (0x20 × *n*) (TCD_{*n*}_SLAST)

Access: User read/write

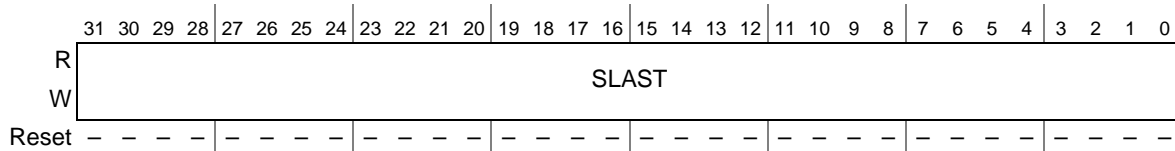


Figure 16-22. TCDn Source Last Address Adjustment (TCDn_SLAST)

Table 16-24. TCDn_SLAST Field Descriptions

Field	Description
31–0 SLAST	Last source address adjustment. Adjustment value added to the source address at the completion of the major iteration count. This value can be applied to restore the source address to the initial value, or adjust the address to reference the next data structure.

Address: $0xFC04_5010 + (0x20 \times n)$ (TCD $_n$ _DADDR)

Access: User read/write

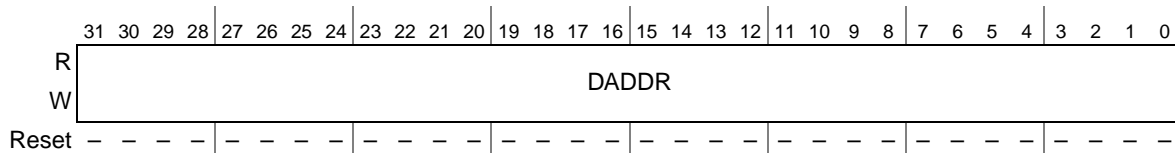


Figure 16-23. TCD_n Destination Address (TCD_n DADDR)

Table 16-25. TCDn_DADDR Field Descriptions

Field	Description
31–0 DADDR	Destination address. Memory address pointing to the destination data.

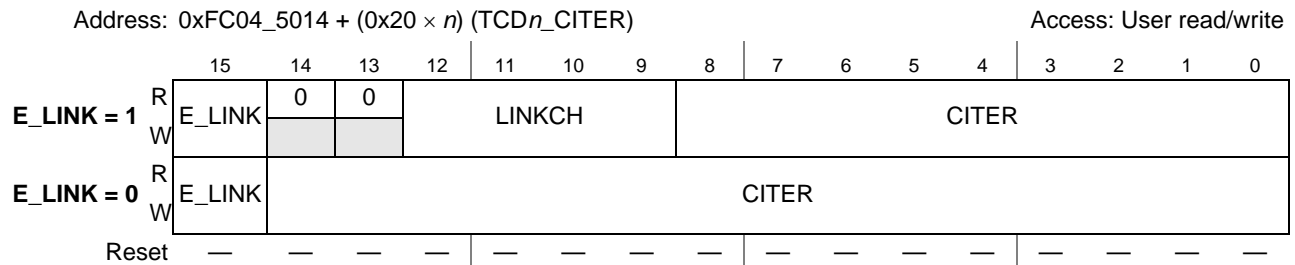


Figure 16-24. TCDn Current Major Iteration Count (TCDn_CITER)

Table 16-26. TCDn_CITER Field Descriptions

Field	Description
15 E_LINK	<p>Enable channel-to-channel linking on minor-loop complete. As the channel completes the minor loop, this flag enables linking to another channel, defined by the LINKCH field. The link target channel initiates a channel service request via an internal mechanism that sets the TCDn_CSR[START] bit of the specified channel.</p> <p>If channel linking is disabled, the CITER value is extended to 15 bits in place of a link channel number. If the major loop is exhausted, this link mechanism is suppressed in favor of the MAJOR_E_LINK channel linking.</p> <p>0 The channel-to-channel linking is disabled. 1 The channel-to-channel linking is enabled.</p> <p>Note: This bit must be equal to the BITER.E_LINK bit. Otherwise, a configuration error is reported.</p>
14–13	Reserved, must be cleared.
12–9 LINKCH	<p>Link channel number. If channel-to-channel linking is enabled (E_LINK = 1), then after the minor loop is exhausted, the eDMA engine initiates a channel service request to the channel defined by these four bits by setting that channel's TCDn_CSR[START] bit.</p> <p>0–15 Link to DMA channel 0–15</p>
14–0 or 8–0 CITER	<p>Current major iteration count. This 9-bit (E_LINK = 1) or 15-bit (E_LINK = 0) count represents the current major loop count for the channel. It is decremented each time the minor loop is completed and updated in the transfer control descriptor memory. After the major iteration count is exhausted, the channel performs a number of operations (e.g., final source and destination address calculations), optionally generating an interrupt to signal channel completion before reloading the CITER field from the beginning iteration count (BITER) field.</p> <p>Note: When the CITER field is initially loaded by software, it must be set to the same value as that contained in the BITER field.</p> <p>Note: If the channel is configured to execute a single service request, the initial values of BITER and CITER should be 0x0001.</p>

Address: $0xFC04_5016 + (0x20 \times n)$ (TCDn_DOFF)

Access: User read/write

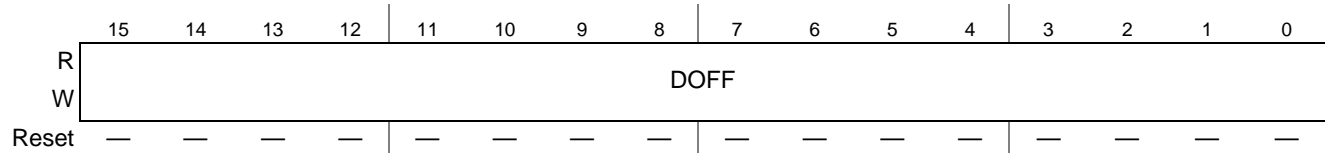


Figure 16-25. TCDn Destination Address Signed Offset (TCDn_DOFF)

Table 16-27. TCDn_DOFF Field Descriptions

Field	Description
15–0 DOFF	Destination address signed offset. Sign-extended offset applied to the current destination address to form the next-state value as each destination write is completed.

Address: $0xFC04_5018 + (0x20 \times n)$ (TCDn_DLAST_SGA)

Access: User read/write

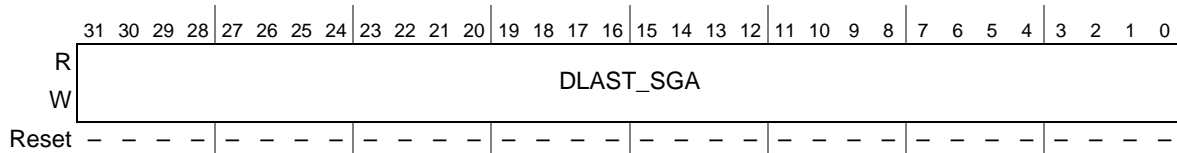


Figure 16-26. TCDn Destination Last Address Adjustment (TCDn_DLAST_SGA)

Table 16-28. TCDn_DLAST_SGA Field Descriptions

Field	Description
31–0 DLAST_SGA	<p>Destination last address adjustment or the memory address for the next transfer control descriptor to be loaded into this channel (scatter/gather).</p> <p>If (TCDn_CSR[E_SG] = 0) then</p> <ul style="list-style-type: none"> Adjustment value added to the destination address at the completion of the major iteration count. This value can apply to restore the destination address to the initial value or adjust the address to reference the next data structure. <p>else</p> <ul style="list-style-type: none"> This address points to the beginning of a 0-modulo-32-byte region containing the next transfer control descriptor to be loaded into this channel. This channel reload is performed as the major iteration count completes. The scatter/gather address must be 0-modulo-32-byte, else a configuration error is reported.

Address: $0xFC04_501C + (0x20 \times n)$ (TCDn_BITER)

Access: User read/write

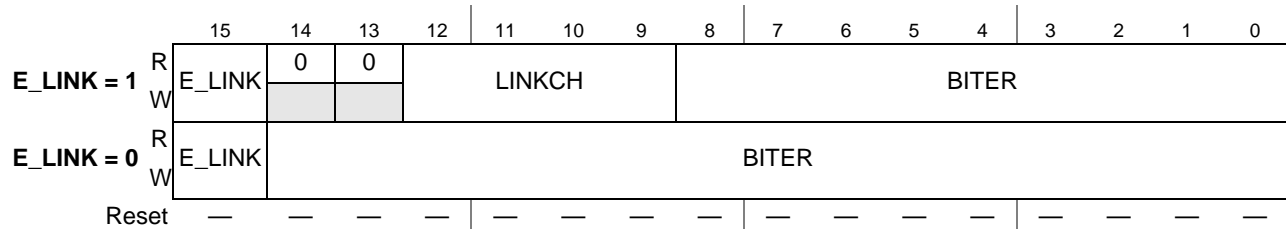


Figure 16-27. TCDn Beginning Major Iteration Count (TCDn_BITER)

Table 16-29. TCD_n_BITER Field Descriptions

Field	Description
15 E_LINK	<p>Enables channel-to-channel linking on minor loop complete. As the channel completes the minor loop, this flag enables the linking to another channel, defined by BITER.LINKCH. The link target channel initiates a channel service request via an internal mechanism that sets the TCD_n_CSR[START] bit of the specified channel. If channel linking disables, the BITER value extends to 15 bits in place of a link channel number. If the major loop is exhausted, this link mechanism is suppressed in favor of the MAJOR_E_LINK channel linking.</p> <p>0 The channel-to-channel linking is disabled. 1 The channel-to-channel linking is enabled.</p> <p>Note: When the software loads the TCD, this field must be set equal to the corresponding CITER field. Otherwise, a configuration error is reported. As the major iteration count is exhausted, the contents of this field is reloaded into the CITER field.</p>
14–13	Reserved, must be cleared.
12–9 LINKCH	<p>Link channel number. If channel-to-channel linking is enabled (E_LINK = 1), then after the minor loop is exhausted, the eDMA engine initiates a channel service request at the channel defined by these four bits by setting that channel's TCD_n_CSR[START] bit.</p> <p>0–15 Link to DMA channel 0–15</p> <p>Note: When the software loads the TCD, this field must be set equal to the corresponding CITER field. Otherwise, a configuration error is reported. As the major iteration count is exhausted, the contents of this field is reloaded into the CITER field.</p>
14–0 or 8–0 BITER	<p>Starting major iteration count. As the transfer control descriptor is first loaded by software, this 9-bit (E_LINK = 1) or 15-bit (E_LINK = 0) field must be equal to the value in the CITER field. As the major iteration count is exhausted, the contents of this field are reloaded into the CITER field.</p> <p>Note: When the software loads the TCD, this field must be set equal to the corresponding CITER field. Otherwise, a configuration error is reported. As the major iteration count is exhausted, the contents of this field is reloaded into the CITER field. If the channel is configured to execute a single service request, the initial values of BITER and CITER should be 0x0001.</p>

Address: 0xFC04_501E + (0x20 × *n*) (TCD_n_CSR)

Access: User read/write

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	BWC		0	0	MAJOR_LINKCH				DONE	ACTIVE	MAJOR_E_LINK	E_SG	D_REQ	INT_HALF	INT_MAJOR	START
W																
Reset	—	—	—	—	—	—	—	—	0	0	—	—	—	—	—	0

Figure 16-28. TCD_n Control and Status (TCD_n_CSR)

Table 16-30. TCDn_CSR Field Descriptions

Field	Description
15–14 BWC	Bandwidth control. Throttles the amount of bus bandwidth consumed by the eDMA. In general, as the eDMA processes the minor loop, it continuously generates read/write sequences until the minor count is exhausted. This field forces the eDMA to stall after the completion of each read/write access to control the bus request bandwidth seen by the crossbar switch (XBS). 00 No eDMA engine stalls 01 Reserved 10 eDMA engine stalls for 4 cycles after each r/w 11 eDMA engine stalls for 8 cycles after each r/w Note: If the source and destination sizes are equal, this field is ignored between the first and second transfers and after the last write of each minor loop. This behavior is a side effect of reducing start-up latency.
13–12	Reserved, must be cleared.
11–8 MAJOR_LINKCH	Link channel number. If (MAJOR_E_LINK = 0) then <ul style="list-style-type: none"> No channel-to-channel linking (or chaining) is performed after the major loop counter is exhausted. else <ul style="list-style-type: none"> After the major loop counter is exhausted, the eDMA engine initiates a channel service request at the channel defined by these four bits by setting that channel's TCDn_CSR[START] bit. 0–15 Link to DMA channel 0–15
7 DONE	Channel done. This flag indicates the eDMA has completed the major loop. The eDMA engine sets it as the CITER count reaches zero; The software clears it, or the hardware when the channel is activated. Note: This bit must be cleared to write the MAJOR_E_LINK or E_SG bits.
6 ACTIVE	Channel active. This flag signals the channel is currently in execution. It is set when channel service begins, and the eDMA clears it as the minor loop completes or if any error condition is detected.
5 MAJOR_E_LINK	Enable channel-to-channel linking on major loop complete. As the channel completes the major loop, this flag enables the linking to another channel, defined by MAJOR_LINKCH. The link target channel initiates a channel service request via an internal mechanism that sets the TCDn_CSR[START] bit of the specified channel. Note: To support the dynamic linking coherency model, this field is forced to zero when written to while the TCDn_CSR[DONE] bit is set. 0 The channel-to-channel linking is disabled. 1 The channel-to-channel linking is enabled.
4 E_SG	Enable scatter/gather processing. As the channel completes the major loop, this flag enables scatter/gather processing in the current channel. If enabled, the eDMA engine uses DLAST_SGA as a memory pointer to a 0-modulo-32 address containing a 32-byte data structure loaded as the transfer control descriptor into the local memory. Note: To support the dynamic scatter/gather coherency model, this field is forced to zero when written to while the TCDn_CSR[DONE] bit is set. 0 The current channel's TCD is normal format. 1 The current channel's TCD specifies a scatter gather format. The DLAST_SGA field provides a memory pointer to the next TCD to be loaded into this channel after the major loop completes its execution.
3 D_REQ	Disable request. If this flag is set, the eDMA hardware automatically clears the corresponding DMAERQ bit when the current major iteration count reaches zero. 0 The channel's DMAERQ bit is not affected. 1 The channel's DMAERQ bit is cleared when the major loop is complete.

Table 16-30. TCD_n_CSR Field Descriptions (continued)

Field	Description
2 INT_HALF	Enable an interrupt when major counter is half complete. If this flag is set, the channel generates an interrupt request by setting the appropriate bit in the EDMA_INT when the current major iteration count reaches the halfway point. Specifically, the comparison performed by the eDMA engine is (CITER == (BITER >> 1)). This halfway point interrupt request is provided to support double-buffered (aka ping-pong) schemes or other types of data movement where the processor needs an early indication of the transfer's progress. The halfway complete interrupt disables when BITER values are less than two. 0 The half-point interrupt is disabled. 1 The half-point interrupt is enabled.
1 INT_MAJOR	Enable an interrupt when major iteration count completes. If this flag is set, the channel generates an interrupt request by setting the appropriate bit in the EDMA_INT when the current major iteration count reaches zero. 0 The end-of-major loop interrupt is disabled. 1 The end-of-major loop interrupt is enabled.
0 START	Channel start. If this flag is set, the channel is requesting service. The eDMA hardware automatically clears this flag after the channel begins execution. 0 The channel is not explicitly started. 1 The channel is explicitly started via a software initiated service request.

16.7 Functional Description

This section provides an overview of the microarchitecture and functional operation of the eDMA module.

16.7.1 eDMA Microarchitecture

The eDMA module is partitioned into two major modules: the eDMA engine and the transfer-control descriptor local memory. Additionally, the eDMA engine is further partitioned into four submodules:

- eDMA Engine
 - Address Path:

This block implements registered versions of two channel transfer control descriptors, channel x and channel y, and manages all master bus-address calculations. All the channels provide the same functionality. This structure allows data transfers associated with one channel to be preempted after the completion of a read/write sequence if a higher priority channel activation is asserted while the first channel is active. After a channel is activated, it runs until the minor loop is completed, unless preempted by a higher priority channel. This provides a mechanism (enabled by DCHPRI_n[ECP]) where a large data move operation can be preempted to minimize the time another channel is blocked from execution.

When any channel is selected to execute, the contents of its TCD are read from local memory and loaded into the address path channel x registers for a normal start and into channel y registers for a preemption start. After the minor loop completes execution, the address path hardware writes the new values for the TCD_n_{SADDR, DADDR, CITER} back to local memory. If the major iteration count is exhausted, additional processing are performed, including the final address pointer updates, reloading the TCD_n_CITER field, and a possible fetch of the next TCD_n from memory as part of a scatter/gather operation.

- Data Path:

This block implements the bus master read/write datapath. It includes 16 bytes of register storage and the necessary multiplex logic to support any required data alignment. The internal read data bus is the primary input, and the internal write data bus is the primary output.

The address and data path modules directly support the 2-stage pipelined internal bus. The address path module represents the 1st stage of the bus pipeline (address phase), while the data path module implements the 2nd stage of the pipeline (data phase).

- Program Model/Channel Arbitration:

This block implements the first section of the eDMA programming model as well as the channel arbitration logic. The programming model registers are connected to the internal peripheral bus (not shown). The eDMA peripheral request inputs and interrupt request outputs are also connected to this block (via control logic).

- Control:

This block provides all the control functions for the eDMA engine. For data transfers where the source and destination sizes are equal, the eDMA engine performs a series of source read/destination write operations until the number of bytes specified in the minor loop byte count has moved. For descriptors where the sizes are not equal, multiple accesses of the smaller size data are required for each reference of the larger size. As an example, if the source size references 16-bit data and the destination is 32-bit data, two reads are performed, then one 32-bit write.

- Transfer Control Descriptor Memory

- Memory Controller:

This logic implements the required dual-ported controller, managing accesses from the eDMA engine as well as references from the internal peripheral bus. As noted earlier, in the event of simultaneous accesses, the eDMA engine is given priority and the peripheral transaction is stalled.

- Memory Array: TCD storage is implemented using a single-port, synchronous RAM array.

16.7.2 eDMA Basic Data Flow

The basic flow of a data transfer can be partitioned into three segments. As shown in [Figure 16-29](#), the first segment involves the channel activation. In the diagram, this example uses the assertion of the eDMA peripheral request signal to request service for channel *n*. Channel activation via software and the TCD_{*n*}_CSR[START] bit follows the same basic flow as peripheral requests. The eDMA request input signal is registered internally and then routed through the eDMA engine: first through the control module, then into the program model and channel arbitration. In the next cycle, the channel arbitration performs, using the fixed-priority or round-robin algorithm. After arbitration is complete, the activated channel number is sent through the address path and converted into the required address to access the local memory for TCD_{*n*}. Next, the TCD memory is accessed and the required descriptor read from the local memory and loaded into the eDMA engine address path channel *x* or *y* registers. The TCD memory is 64 bits wide to minimize the time needed to fetch the activated channel descriptor and load it into the address path channel *x* or *y* registers.

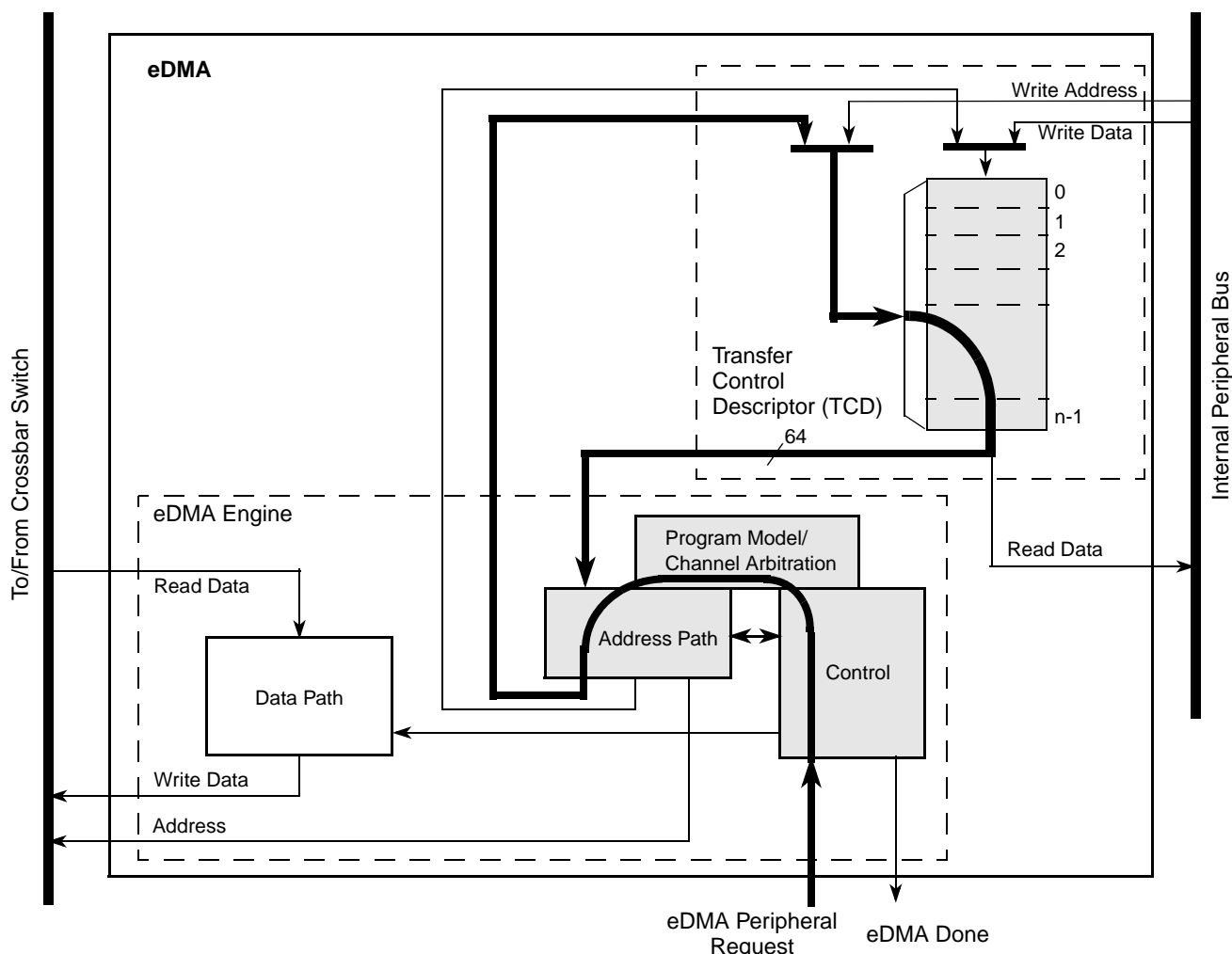


Figure 16-29. eDMA Operation, Part 1

In the second part of the basic data flow (Figure 16-30), the modules associated with the data transfer (address path, data path, and control) sequence through the required source reads and destination writes to perform the actual data movement. The source reads are initiated and the fetched data is temporarily stored in the data path block until it is gated onto the internal bus during the destination write. This source read/destination write processing continues until the minor byte count has transferred.

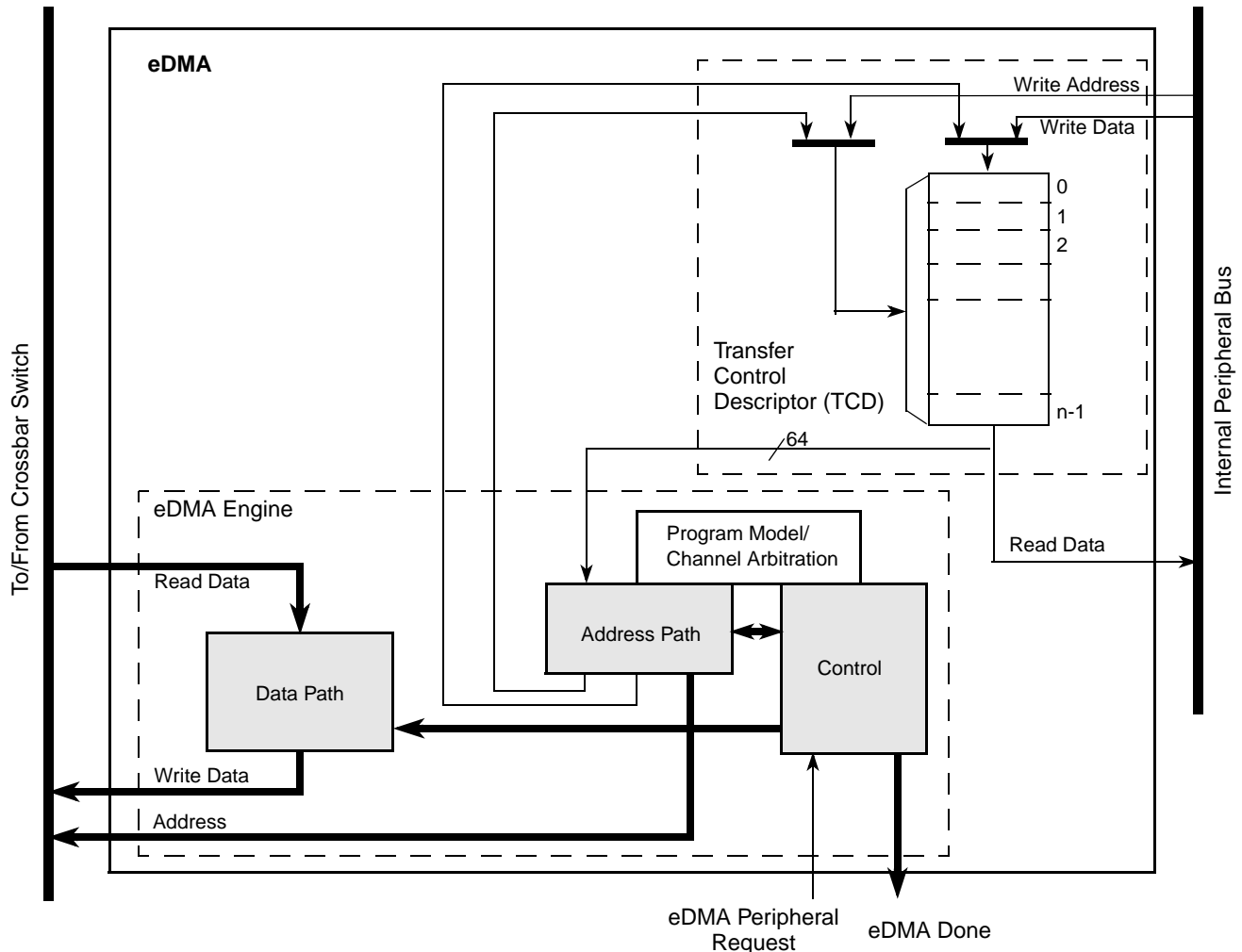


Figure 16-30. eDMA Operation, Part 2

After the minor byte count has moved, the final phase of the basic data flow performs. In this segment, the address path logic performs the required updates to certain fields in the appropriate TCD, e.g., SADDR, DADDR, CITER. If the major iteration count is exhausted, additional operations are performed. These include the final address adjustments and reloading of the BITER field into the CITER. Assertion of an optional interrupt request also occurs at this time, as does a possible fetch of a new TCD from memory using the scatter/gather address pointer included in the descriptor. The updates to the TCD memory and the assertion of an interrupt request are shown in [Figure 16-31](#).

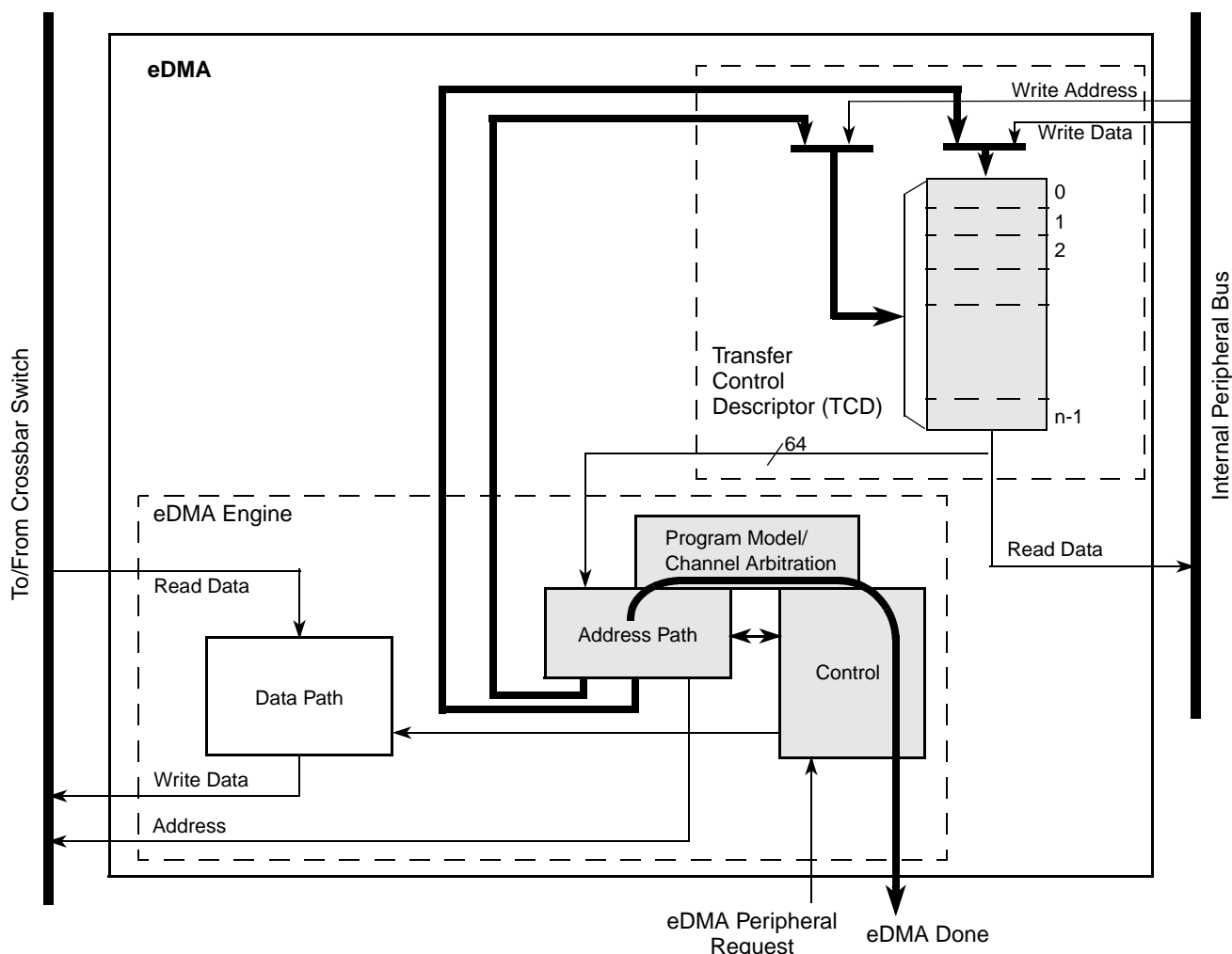


Figure 16-31. eDMA Operation, Part 3

16.8 Initialization/Application Information

16.8.1 eDMA Initialization

A typical initialization of the eDMA has the following sequence:

1. Write the EDMA_CR if a configuration other than the default is desired.
2. Write the channel priority levels into the DCHPRI_n registers if a configuration other than the default is desired.
3. Enable error interrupts in the EDMA_EEI if so desired.
4. Write the 32-byte TCD for each channel that may request service.
5. Enable any hardware service requests via the EDMA_ERQ.
6. Request channel service by software (setting the TCD_n_CSR[START] bit) or hardware (slave device asserting its eDMA peripheral request signal).

After any channel requests service, a channel is selected for execution based on the arbitration and priority levels written into the programmer's model. The eDMA engine read the entire TCD, including the TCD control and status fields (Table 16-31) for the selected channel into its internal address path module. As the TCD is read, the first transfer is initiated on the internal bus unless a configuration error is detected. Transfers from the source (as defined by the source address, TCD $_n$ _SADDR) to the destination (as defined by the destination address, TCD $_n$ _DADDR) continue until the specified number of bytes (TCD $_n$ _NBYTES) are transferred. When transfer is complete, the eDMA engine's local TCD $_n$ _SADDR, TCD $_n$ _DADDR, and TCD $_n$ _CITER are written back to the main TCD memory and any minor loop channel linking is performed, if enabled. If the major loop is exhausted, further post processing executes (interrupts, major loop channel linking, and scatter/gather operations) if enabled.

Table 16-31. TCD Control and Status Fields

TCD$_n$_CSR Field Name	Description
START	Control bit to start channel explicitly when using a software initiated DMA service (Automatically cleared by hardware)
ACTIVE	Status bit indicating the channel is currently in execution
DONE	Status bit indicating major loop completion (cleared by software when using a software initiated DMA service)
D_REQ	Control bit to disable DMA request at end of major loop completion when using a hardware initiated DMA service
BWC	Control bits for throttling bandwidth control of a channel
E_SG	Control bit to enable scatter-gather feature
INT_HALF	Control bit to enable interrupt when major loop is half complete
INT_MAJ	Control bit to enable interrupt when major loop completes

Table 16-32 shows how each DMA request initiates one minor-loop transfer (iteration) without CPU intervention. DMA arbitration can occur after each minor loop, and one level of minor loop DMA preemption is allowed. The number of minor loops in a major loop is specified by the beginning iteration count (BITER).

Table 16-32. Example of Multiple Loop Iterations

				Current Major Loop Iteration Count (CITER)
DMA Request		Minor Loop	Major Loop	3
	.			
	.			
	.			
DMA Request		Minor Loop	Major Loop	2
	.			
	.			
	.			
DMA Request		Minor Loop	Major Loop	1
	.			
	.			
	.			

Table 16-33 lists the memory array terms and how the TCD settings interrelate.

Table 16-33. Memory Array Terms

xADDR: (Starting Address)	xSIZE (size of one data transfer)	Minor Loop (NBYTES in Minor Loop, often the same value as xSIZE)	Offset (xOFF): number of bytes added to current address after each transfer (often the same value as xSIZE)
	.		
	.		
.	.	Minor Loop	Each DMA source (S) and destination (D) has its own: Address (xADDR) Size (xSIZE) Offset (xOFF) Modulo (xMOD) Last Address Adjustment (xLAST) where x = S or D
.	.		
.	.		
.	.		
.	.		
xLAST: Number of bytes added to current address after major loop (typically used to loop back)	.	Last Minor Loop	Peripheral queues typically have size and offset equal to NBYTES.
	.		
	.		
	.		

16.8.2 DMA Programming Errors

The eDMA performs various tests on the transfer control descriptor to verify consistency in the descriptor data. Most programming errors are reported on a per channel basis with the exception of channel priority error (EDMA_ES[CPE]).

For all error types other than channel priority error, the channel number causing the error is recorded in the EDMA_ES. If the error source is not removed before the next activation of the problem channel, the error is detected and recorded again.

If priority levels are not unique, when any channel requests service, a channel priority error is reported. The highest channel priority with an active request is selected, but the lowest numbered channel with that priority is selected by arbitration and executed by the eDMA engine. The hardware service request handshake signals, error interrupts, and error reporting is associated with the selected channel.

16.8.3 DMA Arbitration Mode Considerations

16.8.3.1 Fixed Channel Arbitration

In this mode, the channel service request from the highest priority channel is selected to execute.

16.8.3.2 Round Robin Channel Arbitration

Channels are serviced starting with the highest channel number and rotating through to the lowest channel number without regard to the channel priority levels

16.8.4 DMA Transfer

16.8.4.1 Single Request

To perform a simple transfer of n bytes of data with one activation, set the major loop to one ($TCDn_CITER = TCDn_BITER = 1$). The data transfer begins after the channel service request is acknowledged and the channel is selected to execute. After the transfer is complete, the $TCDn_CSR[DONE]$ bit is set and an interrupt generates if properly enabled.

For example, the following TCD entry is configured to transfer 16 bytes of data. The eDMA is programmed for one iteration of the major loop transferring 16 bytes per iteration. The source memory has a byte wide memory port located at 0x1000. The destination memory has a longword-wide port located at 0x2000. The address offsets are programmed in increments to match the transfer size: one byte for the source and four bytes for the destination. The final source and destination addresses are adjusted to return to their beginning values.

Example 16-1. Single Request DMA Transfer

```
TCDn_CITER = TCDn_BITER = 1
TCDn_NBYTES = 16
TCDn_SADDR = 0x1000
TCDn_SOFF = 1
TCDn_ATTR[SSIZE] = 0
TCDn_SLAST = -16
TCDn_DADDR = 0x2000
TCDn_DOFF = 4
TCDn_ATTR[DSIZE] = 2
TCDn_DLAST_SGA = -16
TCDn_CSR[INT_MAJ] = 1
TCDn_CSR[START] = 1 (Should be written last after all other fields have been initialized)
All other TCDn fields = 0
```

This generates the following event sequence:

1. User write to the $TCDn_CSR[START]$ bit requests channel service.
2. The channel is selected by arbitration for servicing.
3. eDMA engine writes: $TCDn_CSR[DONE] = 0$, $TCDn_CSR[START] = 0$, $TCDn_CSR[ACTIVE] = 1$.
4. eDMA engine reads: channel TCD data from local memory to internal register file.
5. The source-to-destination transfers are executed as follows:
 - a) Read byte from location 0x1000, read byte from location 0x1001, read byte from 0x1002, read byte from 0x1003.

- b) Write longword to location 0x2000 → first iteration of the minor loop.
 - c) Read byte from location 0x1004, read byte from location 0x1005, read byte from 0x1006, read byte from 0x1007.
 - d) Write longword to location 0x2004 → second iteration of the minor loop.
 - e) Read byte from location 0x1008, read byte from location 0x1009, read byte from 0x100A, read byte from 0x100B.
 - f) Write longword to location 0x2008 → third iteration of the minor loop.
 - g) Read byte from location 0x100C, read byte from location 0x100D, read byte from 0x100E, read byte from 0x100F.
 - h) Write longword to location 0x200C → last iteration of the minor loop → major loop complete.
6. The eDMA engine writes: $TCDn_SADDR = 0x1000$, $TCDn_DADDR = 0x2000$, $TCDn_CITER = 1$ ($TCDn_BITER$).
 7. The eDMA engine writes: $TCDn_CSR[ACTIVE] = 0$, $TCDn_CSR[DONE] = 1$, $EDMA_INT[n] = 1$.
 8. The channel retires and the eDMA goes idle or services the next channel.

16.8.4.2 Multiple Requests

Besides transferring 32 bytes via two hardware requests, the next example is the same as previous. The only fields that change are the major loop iteration count and the final address offsets. The eDMA is programmed for two iterations of the major loop transferring 16 bytes per iteration. After the channel's hardware requests are enabled in $EDMA_ERQ$, the slave device initiates channel service requests.

```
TCDn_CITER = TCDn_BITER = 2
TCDn_SLAST = -32
TCDn_DLAST_SGA = -32
```

This would generate the following sequence of events:

1. First hardware (eDMA peripheral) request for channel service.
2. The channel is selected by arbitration for servicing.
3. eDMA engine writes: $TCDn_CSR[DONE] = 0$, $TCDn_CSR[START] = 0$, $TCDn_CSR[ACTIVE] = 1$.
4. eDMA engine reads: channel $TCDn$ data from local memory to internal register file.
5. The source to destination transfers are executed as follows:
 - a) Read byte from location 0x1000, read byte from location 0x1001, read byte from 0x1002, read byte from 0x1003.
 - b) Write longword to location 0x2000 → first iteration of the minor loop.
 - c) Read byte from location 0x1004, read byte from location 0x1005, read byte from 0x1006, read byte from 0x1007.
 - d) Write longword to location 0x2004 → second iteration of the minor loop.
 - e) Read byte from location 0x1008, read byte from location 0x1009, read byte from 0x100A, read byte from 0x100B.

- f) Write longword to location 0x2008 → third iteration of the minor loop.
- g) Read byte from location 0x100C, read byte from location 0x100D, read byte from 0x100E, read byte from 0x100F.
- h) Write longword to location 0x200C → last iteration of the minor loop.
- 6. eDMA engine writes: TCD_n_SADDR = 0x1010, TCD_n_DADDR = 0x2010, TCD_n_CITER = 1.
- 7. eDMA engine writes: TCD_n_CSR[ACTIVE] = 0.
- 8. The channel retires → one iteration of the major loop. The eDMA goes idle or services the next channel.
- 9. Second hardware (eDMA peripheral) requests channel service.
- 10. The channel is selected by arbitration for servicing.
- 11. eDMA engine writes: TCD_n_CSR[DONE] = 0, TCD_n_CSR[START] = 0, TCD_n_CSR[ACTIVE] = 1.
- 12. eDMA engine reads: channel TCD data from local memory to internal register file.
- 13. The source to destination transfers are executed as follows:
 - a) Read byte from location 0x1010, read byte from location 0x1011, read byte from 0x1012, read byte from 0x1013.
 - b) Write longword to location 0x2010 → first iteration of the minor loop.
 - c) Read byte from location 0x1014, read byte from location 0x1015, read byte from 0x1016, read byte from 0x1017.
 - d) Write longword to location 0x2014 → second iteration of the minor loop.
 - e) Read byte from location 0x1018, read byte from location 0x1019, read byte from 0x101A, read byte from 0x101B.
 - f) Write longword to location 0x2018 → third iteration of the minor loop.
 - g) Read byte from location 0x101C, read byte from location 0x101D, read byte from 0x101E, read byte from 0x101F.
 - h) Write longword to location 0x201C → last iteration of the minor loop → major loop complete.
- 14. eDMA engine writes: TCD_n_SADDR = 0x1000, TCD_n_DADDR = 0x2000, TCD_n_CITER = 2 (TCD_n_BITER).
- 15. eDMA engine writes: TCD_n_CSR[ACTIVE] = 0, TCD_n_CSR[DONE] = 1, EDMA_INT[n] = 1.
- 16. The channel retires → major loop complete. The eDMA goes idle or services the next channel.

16.8.4.3 Modulo Feature

The modulo feature of the eDMA provides the ability to implement a circular data queue in which the size of the queue is a power of 2. MOD is a 5-bit field for the source and destination in the TCD, and it specifies which lower address bits increment from their original value after the address+offset calculation. All upper address bits remain the same as in the original value. A setting of 0 for this field disables the modulo feature.

Table 16-34 shows how the transfer addresses are specified based on the setting of the MOD field. Here a circular buffer is created where the address wraps to the original value while the 28 upper address bits

(0x1234567x) retain their original value. In this example the source address is set to 0x12345670, the offset is set to 4 bytes and the MOD field is set to 4, allowing for a 2^4 byte (16-byte) size queue.

Table 16-34. Modulo Feature Example

Transfer Number	Address
1	0x12345670
2	0x12345674
3	0x12345678
4	0x1234567C
5	0x12345670
6	0x12345674

16.8.5 eDMA TCD n Status Monitoring

16.8.5.1 Minor Loop Complete

There are two methods to test for minor loop completion when using software initiated service requests. The first is to read the TCD n _CITER field and test for a change. (Another method may be extracted from the sequence shown below). The second method is to test the TCD n _CSR[START] bit and the TCD n _CSR[ACTIVE] bit. The minor-loop-complete condition is indicated by both bits reading zero after the TCD n _CSR[START] was set. Polling the TCD n _CSR[ACTIVE] bit may be inconclusive, because the active status may be missed if the channel execution is short in duration.

The TCD status bits execute the following sequence for a software activated channel:

	TCD n _CSR bits			State
	START	ACTIVE	DONE	
1	1	0	0	Channel service request via software
2	0	1	0	Channel is executing
3a	0	0	0	Channel has completed the minor loop and is idle
3b	0	0	1	Channel has completed the major loop and is idle

The best method to test for minor-loop completion when using hardware (peripheral) initiated service requests is to read the TCD n _CITER field and test for a change. The hardware request and acknowledge handshakes signals are not visible in the programmer's model.

The TCD status bits execute the following sequence for a hardware-activated channel:

	TCD n _CSR bits			State
	START	ACTIVE	DONE	
1	0	0	0	Channel service request via hardware (peripheral request asserted)
2	0	1	0	Channel is executing
3a	0	0	0	Channel has completed the minor loop and is idle
3b	0	0	1	Channel has completed the major loop and is idle

For both activation types, the major-loop-complete status is explicitly indicated via the TCD n _CSR[DONE] bit.

The TCD n _CSR[START] bit is cleared automatically when the channel begins execution regardless of how the channel activates.

16.8.5.2 Active Channel TCD n Reads

The eDMA reads back the true TCD n _SADDR, TCD n _DADDR, and TCD n _NBYTES values if read while a channel executes. The true values of the SADDR, DADDR, and NBYTES are the values the eDMA engine currently uses in its internal register file and not the values in the TCD local memory for that channel. The addresses (SADDR and DADDR) and NBYTES (decrements to zero as the transfer progresses) can give an indication of the progress of the transfer. All other values are read back from the TCD local memory.

16.8.5.3 Preemption Status

Preemption is available only when fixed arbitration is selected as the channel arbitration mode. A preemptive situation is one in which a preempt-enabled channel runs and a higher priority request becomes active. When the eDMA engine is not operating in fixed channel arbitration mode, the determination of the actively running relative priority outstanding requests become undefined. Channel priorities are treated as equal (constantly rotating) when round-robin arbitration mode is selected.

The TCD n _CSR[ACTIVE] bit for the preempted channel remains asserted throughout the preemption. The preempted channel is temporarily suspended while the preempting channel executes one major loop iteration. If two TCD n _CSR[ACTIVE] bits are set simultaneously in the global TCD map, a higher priority channel is actively preempting a lower priority channel.

16.8.6 Channel Linking

Channel linking (or chaining) is a mechanism where one channel sets the TCD n _CSR[START] bit of another channel (or itself), therefore initiating a service request for that channel. When properly enabled, the EDMA engine automatically performs this operation at the major or minor loop completion.

The minor loop channel linking occurs at the completion of the minor loop (or one iteration of the major loop). The TCD n _CITER[E_LINK] field determines whether a minor loop link is requested. When enabled, the channel link is made after each iteration of the major loop except for the last. When the major

loop is exhausted, only the major loop channel link fields are used to determine if a channel link should be made. For example, the initial fields of:

```
TCDn_CITER[E_LINK] = 1
TCDn_CITER[LINKCH] = 0xC
TCDn_CITER[CITER] value = 0x4
TCDn_CSR[MAJOR_E_LINK] = 1
TCDn_CSR[MAJOR_LINKCH] = 0x7
```

executes as:

1. Minor loop done → set TCD12_CSR[START] bit
2. Minor loop done → set TCD12_CSR[START] bit
3. Minor loop done → set TCD12_CSR[START] bit
4. Minor loop done, major loop done → set TCD7_CSR[START] bit

When minor loop linking is enabled ($TCDn_CITER[E_LINK] = 1$), the $TCDn_CITER[CITER]$ field uses a nine bit vector to form the current iteration count. When minor loop linking is disabled ($TCDn_CITER[E_LINK] = 0$), the $TCDn_CITER[CITER]$ field uses a 15-bit vector to form the current iteration count. The bits associated with the $TCDn_CITER[LINKCH]$ field are concatenated onto the CITER value to increase the range of the CITER.

NOTE

The $TCDn_CITER[E_LINK]$ bit and the $TCDn_BITER[E_LINK]$ bit must equal or a configuration error is reported. The CITER and BITER vector widths must be equal to calculate the major loop, half-way done interrupt point.

[Table 16-35](#) summarizes how a DMA channel can link to another DMA channel, i.e, use another channel's TCD, at the end of a loop.

Table 16-35. Channel Linking Parameters

Desired Link Behavior	TCD Control Field Name	Description
Link at end of Minor Loop	CITER[E_LINK]	Enable channel-to-channel linking on minor loop completion (current iteration)
	CITER[LINKCH]	Link channel number when linking at end of minor loop (current iteration)
Link at end of Major Loop	CSR[MAJOR_E_LINK]	Enable channel-to-channel linking on major loop completion
	CSR[MAJOR_LINKCH]	Link channel number when linking at end of major loop

16.8.7 Dynamic Programming

This section provides recommended methods to change the programming model during channel execution.

16.8.7.1 Dynamic Channel Linking and Dynamic Scatter/Gather

Dynamic channel linking and dynamic scatter/gather is the process of changing the $TCDn_CSR[MAJOR_E_LINK]$ or $TCDn_CSR[E_SG]$ bits during channel execution. These bits are read

from the TCD local memory at the end of channel execution, therefore allowing software to enable either feature during channel execution.

Because software can change the configuration during execution, a coherency sequence must be followed. Consider the scenario the user attempts to execute a dynamic channel link by enabling the `TCDn_CSR[MAJOR_E_LINK]` bit as the eDMA engine retires the channel. The `TCDn_CSR[MAJOR_E_LINK]` would be set in the programmer's model, but it would be indeterminate whether the actual link was made before the channel retired.

The following coherency sequence is recommended when executing a dynamic channel link or dynamic scatter/gather request:

1. Set the `TCDn_CSR[MAJOR_E_LINK]` bit.
2. Read back the `TCDn_CSR[MAJOR_E_LINK]` bit.
3. Test the `TCDn_CSR[MAJOR_E_LINK]` request status.
 - a) If the bit is set, the dynamic link attempt was successful.
 - b) If the bit is cleared, the attempted dynamic link did not succeed, the channel was already retiring.

This same coherency model is true for dynamic scatter/gather operations. For both dynamic requests, the TCD local memory controller forces the `TCDn_CSR[MAJOR_E_LINK]` and `TCDn_CSR[E_SG]` bits to zero on any writes to a `TCDn` after the `TCDn_CSR[DONE]` bit for that channel is set, indicating the major loop is complete.

NOTE

Software must clear the `TCDn_CSR[DONE]` bit before writing the `TCDn_CSR[MAJOR_E_LINK]` or `TCDn_CSR[E_SG]` bits. The `TCDn_CSR[DONE]` bit is cleared automatically by the eDMA engine after a channel begins execution.

Chapter 17

FlexBus

17.1 Introduction

This chapter describes external bus data transfer operations and error conditions. It describes transfers initiated by the ColdFire processor (or any other bus master) and includes detailed timing diagrams showing the interaction of signals in supported bus operations.

NOTE

In this chapter, unless otherwise noted, clock refers to the FB_CLK used for the external bus ($f_{\text{sys}}/2$).

The external data bus is shared between the FlexBus module and the SDRAM controller. When the SDRAM controller is in SDR mode (DRAMSEL = 1), the data bus is switched dynamically between the SDRAM controller and the FlexBus module. However, when the SDRAM controller is in DDR mode (DRAMSEL = 0), D[31:16] is dedicated to the SDRAM data bus and D[15:0] is dedicated to the FlexBus data bus. In this case, external pins D[15:0], are mapped internally to the upper two bytes of the FlexBus data bus, FB_D[31:16]. This chapter only uses FB_D[31:0] or FB_D[31:X] to designate the data bus, but the actual pins used depend on the DRAMSEL setting. Take this into consideration throughout this chapter.

17.1.1 Overview

A multi-function external bus interface called the FlexBus interface controller is provided on the device with basic functionality of interfacing to slave-only devices with a maximum bus frequency up to 83.33 MHz. It can be directly connected to the following asynchronous or synchronous devices with little or no additional circuitry:

- External boot ROMs
- Flash memories
- Gate-array logic
- Other simple target (slave) devices

For asynchronous devices, a simple chip-select based interface can be used.

The FlexBus interface has up to six general purpose chip-selects, $\overline{\text{FB_CS}}[5:0]$. The actual number of chip selects available depends upon the device and its pin configuration. See [Table 13-1](#) for more details. Chip-select $\overline{\text{FB_CS0}}$ can be dedicated to boot memory access and programmed to be byte (8 bits), word

(16 bits), or longword (32 bits) wide. Control signal timing is compatible with common ROM and flash memories.

17.1.2 Features

Key FlexBus features include:

- Six independent, user-programmable chip-select signals ($\overline{\text{FB_CS}}[5:0]$) that can interface with external SRAM, PROM, EPROM, EEPROM, flash, and other peripherals
- 8-, 16-, and 32-bit port sizes
- Byte-, word-, longword-, and 16-byte line-sized transfers
- Programmable burst- and burst-inhibited transfers selectable for each chip select and transfer direction
- Programmable address-setup time with respect to the assertion of chip select
- Programmable address-hold time with respect to the negation of chip select and transfer direction

17.2 External Signals

This section describes the external signals involved in data-transfer operations.

Table 17-1. FlexBus Signal Summary

Signal Name	I/O ¹	Description
FB_A[23:0]	O	Address bus. During the first cycle, this bus drives the upper address byte, addr[31:24].
FB_D[31:0]	I/O	Data bus
$\overline{\text{FB_CS}}[5:0]$	O	General purpose chip-selects. The actual number of chip selects available depends upon the device and its pin configuration. See Table 13-1 for more details.
$\overline{\text{FB_BE/BWE}}[3:0]$	O	Byte enable/byte write enable
$\overline{\text{FB_OE}}$	O	Output enable
FB_R/ $\overline{\text{W}}$	O	Read/write. 1 = Read, 0 = Write
$\overline{\text{FB_TS}}$	O	Transfer start
$\overline{\text{FB_TA}}$	I	Transfer acknowledge

¹ Because this device shares the FlexBus signals with the SDRAM controller, these signal directions are only valid when the FlexBus controls them. The directions may change during SDRAM cycles.

17.2.1 Address and Data Buses (FB_A[23:0], FB_D[31:0])

The FB_A[23:0] and FB_D[31:0] buses carry the address and data, respectively. The number of byte lanes carrying the data is determined by the port size associated with the matching chip select.

Because this device shares the FlexBus signals with the SDRAM controller, these signals tristate between bus cycles.

17.2.2 Chip Selects ($\overline{\text{FB_CS}}[5:0]$)

The chip-select signal indicates which device is selected. A particular chip-select asserts when the transfer address is within the device's address space, as defined in the base- and mask-address registers. The actual number of chip selects available depends upon the pin configuration. See [Table 13-1](#) for more details.

17.2.3 Byte Enables/Byte Write Enables ($\overline{\text{FB_BE/BWE}}[3:0]$)

When driven low, the byte enable ($\overline{\text{FB_BE/BWE}}[3:0]$) outputs indicate data is to be latched or driven onto a byte of the data bus. $\overline{\text{FB_BE/BWE}}_n$ signals are asserted only to the memory bytes used during read or write accesses. A configuration option is provided to assert these signals on reads and writes (byte enable) or writes only (byte-write enable).

The $\overline{\text{FB_BE/BWE}}_n$ signals are asserted during accesses to on-chip peripherals but not to on-chip SRAM or cache. For external SRAM or flash devices, the $\overline{\text{FB_BE/BWE}}_n$ outputs must be connected to individual byte strobe signals.

17.2.4 Output Enable ($\overline{\text{FB_OE}}$)

The output enable signal ($\overline{\text{FB_OE}}$) is sent to the interfacing memory and/or peripheral to enable a read transfer. $\overline{\text{FB_OE}}$ is only asserted during read accesses when a chip select matches the current address decode.

Because this device shares the FlexBus signals with the SDRAM controller, this signal tristates between bus cycles.

17.2.5 Read/Write ($\overline{\text{FB_R/W}}$)

The processor drives the $\overline{\text{FB_R/W}}$ signal to indicate the current bus operation direction. It is driven high during read bus cycles and low during write bus cycles.

Because this device shares the FlexBus signals with the SDRAM controller, this signal tristates between bus cycles.

17.2.6 Transfer Start ($\overline{\text{FB_TS}}$)

The assertion of $\overline{\text{FB_TS}}$ indicates that the device has begun a bus transaction and the address and attributes are valid. $\overline{\text{FB_TS}}$ is asserted for one bus clock cycle.

Because this device shares the FlexBus signals with the SDRAM controller, this signal tristates between bus cycles.

17.2.7 Transfer Acknowledge ($\overline{\text{FB_TA}}$)

This signal indicates the external data transfer is complete. When the processor recognizes $\overline{\text{FB_TA}}$ during a read cycle, it latches the data and then terminates the bus cycle. When the processor recognizes $\overline{\text{FB_TA}}$ during a write cycle, the bus cycle is terminated.

If auto-acknowledge is disabled ($CSCR_n[AA] = 0$), the external device drives $\overline{FB_TA}$ to terminate the bus transfer; if auto-acknowledge is enabled ($CSCR_n[AA] = 1$), $\overline{FB_TA}$ is generated internally after a specified number of wait states, or the external device may assert external $\overline{FB_TA}$ before the wait-state countdown, terminating the cycle early. The device negates $\overline{FB_CSn}$ one cycle after the last $\overline{FB_TA}$ asserts. During read cycles, the peripheral must continue to drive data until $\overline{FB_TA}$ is recognized. For write cycles, the processor continues driving data one clock after $\overline{FB_CSn}$ is negated.

The number of wait states is determined by $CSCR_n$ or the external $\overline{FB_TA}$ input. If the external $\overline{FB_TA}$ is used, the peripheral has total control on the number of wait states.

NOTE

External devices should only assert $\overline{FB_TA}$ while the $\overline{FB_CSn}$ signal to the external device is asserted.

Because this device shares the FlexBus signals with the SDRAM controller, this signal tristates between bus cycles.

17.3 Memory Map/Register Definition

The following tables describe the registers and bit meanings for configuring chip-select operation. Table 17-2 shows the chip-select register memory map.

The actual number of chip select registers available depends upon the device and its pin configuration. See Table 13-1 for more details. If the device does not support certain chip select signals or the pin is not configured for a chip-select function, then that corresponding set of chip-select registers has no effect on an external pin.

Table 17-2. FlexBus Chip Select Memory Map

Address	Register	Width (bits)	Access	Reset Value	Section/ Page
0xFC00_8000 + ($n \times 0xC$)	Chip-Select Address Register (CSAR n) $n = 0 - 5$	32	R/W	0x0000_0000	17.3.1/17-4
0xFC00_8004 + ($n \times 0xC$)	Chip-Select Mask Register (CSMR n) $n = 0 - 5$	32	R/W	0x0000_0000	17.3.2/17-5
0xFC00_8008 + ($n \times 0xC$)	Chip-Select Control Register (CSCR n) $n = 0 - 5$	32	R/W	See Section	17.3.3/17-6

17.3.1 Chip-Select Address Registers (CSAR0 – CSAR5)

The CSAR n registers specify the chip-select base addresses.

NOTE

Because the FlexBus module is one of the slaves connected to the crossbar switch, it is only accessible within a certain memory range. The only applicable address ranges for which the chip-selects can be active are 0x0000_0000 – 0x3FFF_FFFF and 0xC000_0000 – 0xDFFF_FFFF. Set the CSAR n registers appropriately.

Address: 0xFC00_8000 (CSAR0)
 0xFC00_800C (CSAR1)
 0xFC00_8018 (CSAR2)
 0xFC00_8024 (CSAR3)
 0xFC00_8030 (CSAR4)
 0xFC00_803C (CSAR5)

Access: User read/write

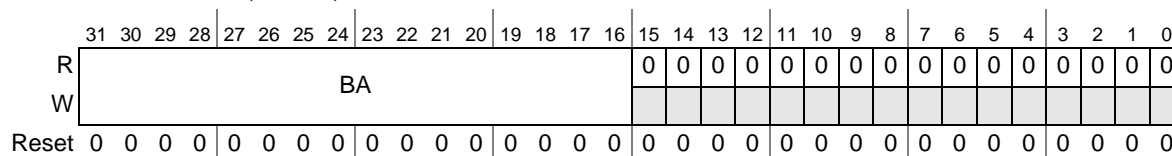


Figure 17-1. Chip-Select Address Registers (CSAR n)

Table 17-3. CSAR n Field Descriptions

Field	Description
31–16 BA	Base address. Defines the base address for memory dedicated to chip-select $\overline{FB_CSn}$. BA is compared to bits 31–16 on the internal address bus to determine if chip-select memory is being accessed.
15–0	Reserved, must be cleared.

17.3.2 Chip-Select Mask Registers (CSMR0 – CSMR5)

CSMR n registers specify the address mask and allowable access types for the respective chip-selects.

Address: 0xFC00_8004 (CSMR0)
 0xFC00_8010 (CSMR1)
 0xFC00_801C (CSMR2)
 0xFC00_8028 (CSMR3)
 0xFC00_8034 (CSMR4)
 0xFC00_8040 (CSMR5)

Access: User read/write

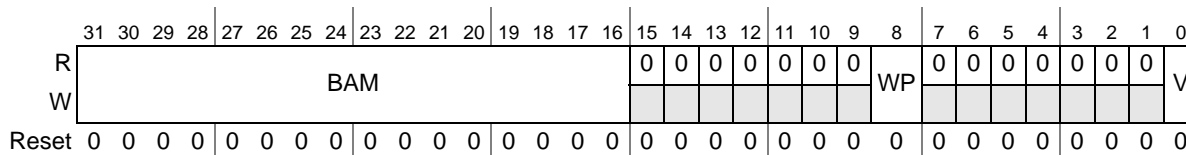


Figure 17-2. Chip-Select Mask Registers (CSMR n)

Table 17-4. CSMR_n Field Descriptions

Field	Description
31–16 BAM	<p>Base address mask. Defines the chip-select block size by masking address bits. Setting a BAM bit causes the corresponding CSAR bit to be a don't care in the decode.</p> <p>0 Corresponding address bit is used in chip-select decode. 1 Corresponding address bit is a don't care in chip-select decode.</p> <p>The block size for $\overline{\text{FB_CS}}_n$ is 2^n; $n = (\text{number of bits set in respective CSMR[BAM]}) + 16$. For example, if CSAR0 equals 0x0000 and CSMR0[BAM] equals 0x0008, $\overline{\text{FB_CS}}_0$ addresses two discontinuous 64-Kbyte memory blocks: one from 0x0_0000 – 0x0_FFFF and one from 0x8_0000 – 0x8_FFFF. Likewise, for $\overline{\text{FB_CS}}_0$ to access 32 Mbytes of address space starting at location 0x00_0000, $\overline{\text{FB_CS}}_1$ must begin at the next byte after $\overline{\text{FB_CS}}_0$ for a 16-Mbyte address space. Then, CSAR0 equals 0x0000, CSMR0[BAM] equals 0x01FF, CSAR1 equals 0x0200, and CSMR1[BAM] equals 0x00FF.</p>
15–9	Reserved, must be cleared.
8 WP	<p>Write protect. Controls write accesses to the address range in the corresponding CSAR. Attempting to write to the range of addresses for which CSAR_n[WP] is set results in a bus error termination of the internal cycle and no external cycle.</p> <p>0 Read and write accesses are allowed 1 Only read accesses are allowed</p>
7–1	Reserved, must be cleared.
0 V	<p>Valid bit. Indicates whether the corresponding CSAR, CSMR, and CSCR contents are valid. Programmed chip-selects do not assert until V bit is set (except for $\overline{\text{FB_CS}}_0$, which acts as the global chip-select). Reset clears each CSMR_n[V].</p> <p>Note: At reset, no chip-select other than $\overline{\text{FB_CS}}_0$ can be used until the CSMR0[V] is set. Afterward, $\overline{\text{FB_CS}}[5:0]$ functions as programmed.</p> <p>0 Chip-select invalid 1 Chip-select valid</p>

17.3.3 Chip-Select Control Registers (CSCR0 – CSCR5)

Each CSCR_n controls the auto-acknowledge, address setup and hold times, port size, burst capability, and number of wait states. To support the global chip-select, $\overline{\text{FB_CS}}_0$, the CSCR0 reset values differ from the

other CSCRs. $\overline{\text{FB_CS0}}$ allows address decoding for an external device to serve as the boot memory before system initialization and configuration are completed.

Address: 0xFC00_8008 (CSCR0)
 0xFC00_8014 (CSCR1)
 0xFC00_8020 (CSCR2)
 0xFC00_802C (CSCR3)
 0xFC00_8038 (CSCR4)
 0xFC00_8044 (CSCR5)

Access: User
 read/write

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
R	SWS				0		0		SWSEN	0		ASET	RDAH		WRAH	
W																
Reset: CSCR0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1
Reset: CSCR1–5	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	WS				SBM		AA		PS		BEM	BSTR	BSTW	0		0
W																
Reset: CSCR0	1	1	1	1	1	1	[DRAM SEL]	1	D4	D3	1	0	0	0	0	0
Reset: CSCR1–5	0	0	0	0	0	0	[DRAM SEL]	1	0	0	1	0	0	0	0	0

Figure 17-3. Chip-Select Control Registers (CSCR n)

Table 17-5. CSCR n Field Descriptions

Field	Description
31–26 SWS	Secondary wait states. The number of wait states inserted before an internal transfer acknowledge is generated for a burst transfer except for the first termination, which is controlled by the wait state count. The secondary wait state is used only if the SWSEN bit is set. Otherwise, the WS value is used for all burst transfers.
25–24	Reserved, must be cleared
23 SWSEN	Secondary wait state enable. 0 The WS value inserts wait states before an internal transfer acknowledge is generated for all transfers. 1 The SWS value inserts wait states before an internal transfer acknowledge is generated for burst transfer secondary terminations.
22	Reserved, must be cleared
21–20 ASET	Address setup. This field controls the assertion of the chip-select with respect to assertion of a valid address and attributes. The address and attributes are considered valid at the same time $\overline{\text{FB_TS}}$ asserts. 00 Assert $\overline{\text{FB_CSn}}$ on first rising clock edge after address is asserted. (Default $\overline{\text{FB_CSn}}$) 01 Assert $\overline{\text{FB_CSn}}$ on second rising clock edge after address is asserted. 10 Assert $\overline{\text{FB_CSn}}$ on third rising clock edge after address is asserted. 11 Assert $\overline{\text{FB_CSn}}$ on fourth rising clock edge after address is asserted. (Default $\overline{\text{FB_CS0}}$)

Table 17-5. CSCR_n Field Descriptions (continued)

Field	Description															
19–18 RDAH	<p>Read address hold or deselect. This field controls the address and attribute hold time after the termination during a read cycle that hits in the chip-select address space. The hold time applies only at the end of a transfer. Therefore, during a burst transfer or a transfer to a port size smaller than the transfer size, the hold time is only added after the last bus cycle.</p> <p>The number of cycles the address and attributes are held after $\overline{\text{FB_CS}}_n$ negation depends on the value of CSCR_n[AA] as shown below.</p> <table><tr><th>RDAH</th><th>AA = 0</th><th>AA = 1</th></tr><tr><td>00 ($\overline{\text{FB_CS}}_n$ Default)</td><td>1 cycle</td><td>0 cycles</td></tr><tr><td>01</td><td>2 cycles</td><td>1 cycles</td></tr><tr><td>10</td><td>3 cycles</td><td>2 cycles</td></tr><tr><td>11 ($\overline{\text{FB_CS}}_0$ Default)</td><td>4 cycles</td><td>3 cycles</td></tr></table>	RDAH	AA = 0	AA = 1	00 ($\overline{\text{FB_CS}}_n$ Default)	1 cycle	0 cycles	01	2 cycles	1 cycles	10	3 cycles	2 cycles	11 ($\overline{\text{FB_CS}}_0$ Default)	4 cycles	3 cycles
RDAH	AA = 0	AA = 1														
00 ($\overline{\text{FB_CS}}_n$ Default)	1 cycle	0 cycles														
01	2 cycles	1 cycles														
10	3 cycles	2 cycles														
11 ($\overline{\text{FB_CS}}_0$ Default)	4 cycles	3 cycles														
17–16 WRAH	<p>Write address hold or deselect. This field controls the address, data, and attribute hold time after the termination of a write cycle that hits in the chip-select address space. The hold time applies only at the end of a transfer. Therefore, during a burst transfer or a transfer to a port size smaller than the transfer size, the hold time is only added after the last bus cycle.</p> <p>00 Hold address and attributes one cycle after $\overline{\text{FB_CS}}_n$ negates on writes. (Default $\overline{\text{FB_CS}}_n$)</p> <p>01 Hold address and attributes two cycles after $\overline{\text{FB_CS}}_n$ negates on writes.</p> <p>10 Hold address and attributes three cycles after $\overline{\text{FB_CS}}_n$ negates on writes.</p> <p>11 Hold address and attributes four cycles after $\overline{\text{FB_CS}}_n$ negates on writes. (Default $\overline{\text{FB_CS}}_0$)</p>															
15–10 WS	<p>Wait states. The number of wait states inserted after $\overline{\text{FB_CS}}_n$ asserts and before an internal transfer acknowledge is generated (WS = 0 inserts zero wait states, WS = 0x3F inserts 63 wait states). If AA is reserved, $\overline{\text{FB_TA}}$ must be asserted by the external system regardless of the number of generated wait states. In that case, the external transfer acknowledge ends the cycle. An external $\overline{\text{FB_TA}}$ supersedes the generation of an internal $\overline{\text{FB_TA}}$.</p>															
9 SBM	<p>Split bus mode. For proper operation of the chip select signals, this bit must be set when the SDRAM controller is in DDR mode (DRAMSEL signal is negated). The reset value of SBM is the opposite of the DRAMSEL signal.</p> <p>0 Device is not in split bus mode (SDRAM controller is in SDR mode, DRAMSEL = 1).</p> <p>1 Device is in split bus mode (SDRAM controller is in DDR mode, DRAMSEL = 0).</p> <p>Note: Placing the device in split bus mode is only controlled by the DRAMSEL signal. This bit is only used to provide correct operation of the chip select signals.</p>															
8 AA	<p>Auto-acknowledge enable. Determines the assertion of the internal transfer acknowledge for accesses specified by the chip-select address.</p> <p>0 No internal $\overline{\text{FB_TA}}$ is asserted. Cycle is terminated externally</p> <p>1 Internal transfer acknowledge is asserted as specified by WS</p> <p>Note: If AA is set for a corresponding $\overline{\text{FB_CS}}_n$ and the external system asserts an external $\overline{\text{FB_TA}}$ before the wait-state countdown asserts the internal $\overline{\text{FB_TA}}$, the cycle is terminated. Burst cycles increment the address bus between each internal termination.</p> <p>Note:</p>															
7–6 PS	<p>Port size. Specifies the data port width associated with each chip-select. It determines where data is driven during write cycles and where data is sampled during read cycles.</p> <p>00 32-bit port size. Valid data sampled and driven on FB_D[31:0]</p> <p>01 8-bit port size. Valid data sampled and driven on FB_D[31:24] if SBM = 0 or FB_D[7:0] if SBM = 1</p> <p>1x 16-bit port size. Valid data sampled and driven on FB_D[31:16] if SBM = 0 or FB_D[15:0] if SBM = 1</p>															

Table 17-5. CSCR n Field Descriptions (continued)

Field	Description
5 BEM	Byte-enable mode. Specifies the byte enable operation. Certain memories have byte enables that must be asserted during reads and writes. BEM can be set in the relevant CSCR to provide the appropriate mode of byte enable support for these SRAMs. 0 $\overline{\text{FB_BE/BWE}}$ is not asserted for reads. $\overline{\text{FB_BE/BWE}}$ is asserted for data write only. 1 $\overline{\text{FB_BE/BWE}}$ is asserted for read and write accesses.
4 BSTR	Burst-read enable. Specifies whether burst reads are used for memory associated with each $\overline{\text{FB_CS}}_n$. 0 Data exceeding the specified port size is broken into individual, port-sized, non-burst reads. For example, a longword read from an 8-bit port is broken into four 8-bit reads. 1 Enables data burst reads larger than the specified port size, including longword reads from 8- and 16-bit ports, word reads from 8-bit ports, and line reads from 8, 16-, and 32-bit ports.
3 BSTW	Burst-write enable. Specifies whether burst writes are used for memory associated with each $\overline{\text{FB_CS}}_n$. 0 Break data larger than the specified port size into individual, port-sized, non-burst writes. For example, a longword write to an 8-bit port takes four byte writes. 1 Enables burst write of data larger than the specified port size, including longword writes to 8 and 16-bit ports, word writes to 8-bit ports, and line writes to 8-, 16-, and 32-bit ports.
2–0	Reserved, must be cleared.

17.4 Functional Description

17.4.1 Chip-Select Operation

Each chip-select has a dedicated set of registers for configuration and control:

- Chip-select address registers (CSAR n) control the base address space of the chip-select. See [Section 17.3.1, “Chip-Select Address Registers \(CSAR0 – CSAR5\).”](#)
- Chip-select mask registers (CSMR n) provide 16-bit address masking and access control. See [Section 17.3.2, “Chip-Select Mask Registers \(CSMR0 – CSMR5\).”](#)
- Chip-select control registers (CSCR n) provide port size and burst capability indication, wait-state generation, address setup and hold times, and automatic acknowledge generation features. See [Section 17.3.3, “Chip-Select Control Registers \(CSCR0 – CSCR5\).”](#)

$\overline{\text{FB_CS}}_0$ is a global chip-select after reset and provides external boot memory capability.

17.4.1.1 General Chip-Select Operation

When a bus cycle is routed to the FlexBus, the device first compares its address with the base address and mask configurations programmed for chip-selects 0 to 5 (configured in CSCR0 – CSCR5). The results depend on if the address matches or not as shown in [Table 17-6](#).

Table 17-6. Results of Address Comparison

Address Matches CSAR n ?	Result
Yes, one CSAR	The appropriate chip-select is asserted, generating an external bus cycle as defined in the chip-select control register.
No	The internal bus cycle terminates and no chip select is asserted.
Yes, multiple CSARs	The chip-select signals are driven. However, they are driven using an external burst-inhibited bus cycle with external termination on a 32-bit port.

17.4.1.2 8-, 16-, and 32-Bit Port Sizing

Static bus sizing is programmable through the port size bits, CSCR[PS]. The processor always drives a 24-bit address on the FB_A bus regardless of the external device's address size. The external device must connect its address lines to the appropriate FB_A bits from FB_A0 upward. It must also connect its data lines to the FB_D bus from FB_D31 downward. No bit ordering is required when connecting address and data lines to the FB_A and FB_D buses. For example, a full 16-bit address/16-bit data device connects its addr[15:0] to FB_A[16:1] and data[15:0] to FB_D[31:16]. See [Figure 17-4](#) for a graphical connection.

17.4.1.3 Global Chip-Select Operation

$\overline{\text{FB_CS0}}$, the global (boot) chip-select, supports external boot memory accesses before system initialization. Its operation differs from other external chip-select outputs after system reset.

After system reset, $\overline{\text{FB_CS0}}$ is asserted for every external access. No other chip-select can be used until the valid bit, CSMR0[V], is set; at this point $\overline{\text{FB_CS0}}$ functions as configured. After this, $\overline{\text{FB_CS}}[5:1]$ can be used as well. At reset, the logic levels on the FB_D[4:3] signals determine global chip-select port size.

See [Chapter 9, “Chip Configuration Module \(CCM\),”](#) for more information.

17.4.2 Data Transfer Operation

Data transfers between the chip and other devices involve these signals:

- Address/data bus (FB_A[23:0], FB_D[31:0])
- Control signals ($\overline{\text{FB_TS}}$, $\overline{\text{FB_TA}}$, $\overline{\text{FB_CS}}_n$, $\overline{\text{FB_OE}}$, $\overline{\text{FB_BE/BWE}}[3:0]$)
- Attribute signals (FB_R/ $\overline{\text{W}}$)

The address, write data, $\overline{\text{FB_TS}}$, $\overline{\text{FB_CS}}_n$, and all attribute signals change on the rising edge of the FlexBus clock (FB_CLK). Read data is latched into the device on the rising edge of the clock.

The FlexBus supports byte-, word-, longword-, and 16-byte (line) operand transfers and allows accesses to 8-, 16-, and 32-bit data ports. Transfer parameters (address setup and hold, port size, the number of wait states for the external device being accessed, automatic internal transfer termination enable or disable, and burst enable or disable) are programmed in the chip-select control registers (CSCRs). See [Section 17.3.3, “Chip-Select Control Registers \(CSCR0 – CSCR5\).”](#)

17.4.3 Data Byte Alignment and Physical Connections

The device aligns data transfers in FlexBus byte lanes with the number of lanes depending on the data port width. The byte lane assignment is also dependent on the split bus mode setting in the CSCR_{*n*} register.

[Figure 17-4](#) shows the byte lanes that external memory connects to and the sequential transfers of a longword transfer for the supported port sizes when not in split bus mode. For example, an 8-bit memory connects to the single lane FB_D[31:24] (FB_BE/BWE0). A longword transfer through this 8-bit port takes four transfers, starting with the MSB to the LSB. A longword transfer through a 32-bit port requires one transfer on each four-byte lane of the FlexBus.

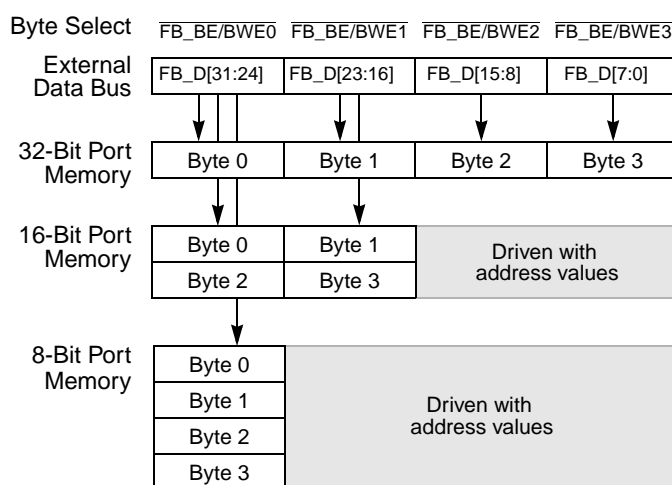


Figure 17-4. Connections for External Memory Port Sizes (CSCR_{*n*}[SBM] = 0)

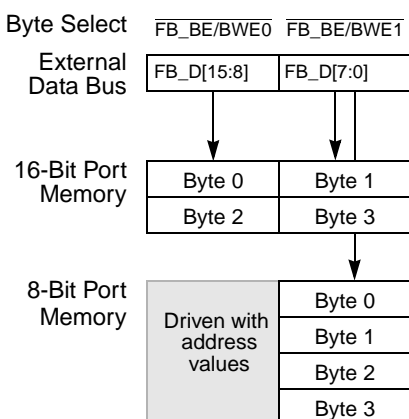


Figure 17-5. Connections for External Memory Port Sizes (CSCR_{*n*}[SBM] = 1)

17.4.4 Bus Cycle Execution

As shown in [Figure 17-8](#) and [Figure 17-10](#), basic bus operations occur in four clocks:

1. S0: At the first clock edge, the address, attributes, and $\overline{\text{FB_TS}}$ are driven.
2. S1: $\overline{\text{FB_CSn}}$ is asserted at the second rising clock edge to indicate the device selected; by that time, the address and attributes are valid and stable. $\overline{\text{FB_TS}}$ is negated at this edge.

For a write transfer, data is driven on the bus at this clock edge and continues to be driven until one clock cycle after $\overline{\text{FB_CSn}}$ negates. For a read transfer, data is also driven into the device during this cycle.

External slave asserts $\overline{\text{FB_TA}}$ at this clock edge.

3. S2: Read data and $\overline{\text{FB_TA}}$ are sampled on the third clock edge. $\overline{\text{FB_TA}}$ can be negated after this edge and read data can then be tri-stated.
4. S3: $\overline{\text{FB_CSn}}$ is negated at the fourth rising clock edge. This last clock of the bus cycle uses what would be an idle clock between cycles to provide hold time for address, attributes, and write data.

17.4.4.1 Data Transfer Cycle States

An on-chip state machine controls the data-transfer operation in the device. [Figure 17-6](#) shows the state-transition diagram for basic read and write cycles.

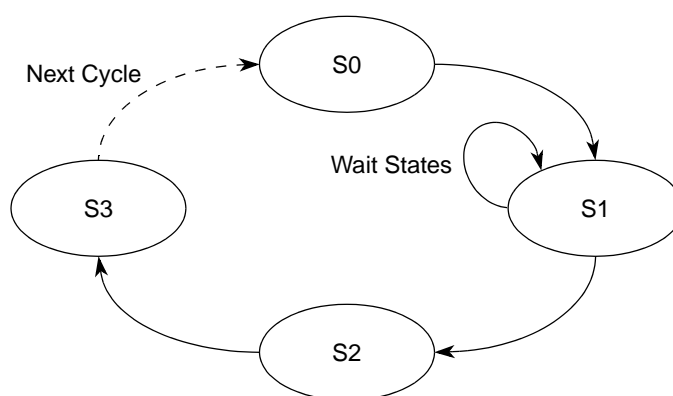


Figure 17-6. Data-Transfer-State-Transition Diagram

[Table 17-7](#) describes the states as they appear in subsequent timing diagrams.

Table 17-7. Bus Cycle States

State	Cycle	Description
S0	All	The read or write cycle is initiated. On the rising clock edge, the device places a valid address on $\text{FB_A}[23:0]$, asserts $\overline{\text{FB_TS}}$, and drives $\text{FB_R}/\overline{\text{W}}$ high for a read and low for a write.

Table 17-7. Bus Cycle States (continued)

State	Cycle	Description
S1	All	<p>$\overline{\text{FB_TS}}$ is negated on the rising edge of FB_CLK, and $\overline{\text{FB_CSn}}$ is asserted. Data is driven on $\text{FB_D}[31:X]$ for writes, and $\text{FB_D}[31:X]$ is tristated for reads. Address continues to be driven on the FB_A pins.</p> <p>If $\overline{\text{FB_TA}}$ is recognized asserted, then the cycle moves on to S2. If $\overline{\text{FB_TA}}$ is not asserted internally or externally, then the S1 state continues to repeat.</p>
	Read	Data is driven by the external device before the next rising edge of FB_CLK (the rising edge that begins S2) with $\overline{\text{FB_TA}}$ asserted.
S2	All	For internal termination, $\overline{\text{FB_CSn}}$ is negated and the internal system bus transfer is completed. For external termination, the external device should negate $\overline{\text{FB_TA}}$, and the $\overline{\text{FB_CSn}}$ chip select negates after the rising edge of FB_CLK at the end of S2.
	Read	The processor latches data on the rising clock edge entering S2. The external device can stop driving data after this edge. However, data can be driven until the end of S3 or any additional address hold cycles.
S3	All	Address, data, and $\text{FB_R}/\overline{\text{W}}$ go invalid off the rising edge of FB_CLK at the beginning of S3, terminating the read or write cycle.

17.4.5 FlexBus Timing Examples

NOTE

Because this device shares the FlexBus signals with the SDRAM controller, all signals, except the chip selects, tristate between bus cycles.

17.4.5.1 Basic Read Bus Cycle

During a read cycle, the ColdFire device receives data from memory or a peripheral device. [Figure 17-7](#) is a read cycle flowchart.

NOTE

Throughout this chapter FB_D[31:X] indicates a 32-, 16-, or 8-bit wide data bus.

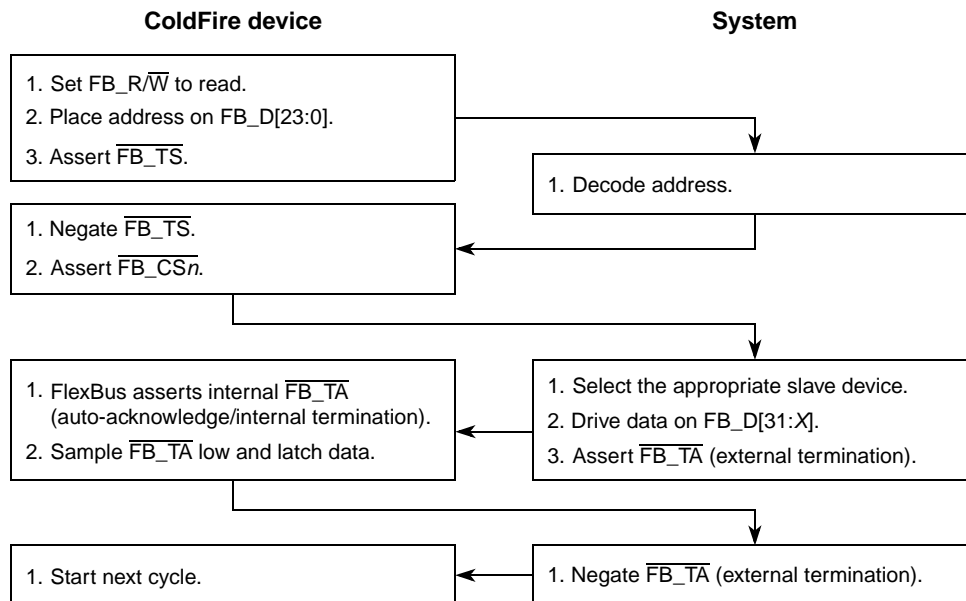


Figure 17-7. Read Cycle Flowchart

The read cycle timing diagram is shown in [Figure 17-8](#).

NOTE

In the next set of timing diagrams, the dotted lines indicate $\overline{\text{FB_TA}}$, $\overline{\text{FB_OE}}$, and $\overline{\text{FB_CS}}_n$ timing when internal termination is used ($\text{CSCR}[\text{AA}] = 1$). The external and internal $\overline{\text{FB_TA}}$ assert at the same time; however, $\overline{\text{FB_TA}}$ is not driven externally for internally-terminated bus cycles.

NOTE

The processor drives the data lines during the first clock cycle of the transfer with the full 32-bit address. This may be ignored by standard connected devices using non-multiplexed address and data buses. However, some applications may find this feature beneficial.

The address and data busses are muxed between the FlexBus and SDRAM controller. At the end of the read bus cycles the address signals are indeterminate.

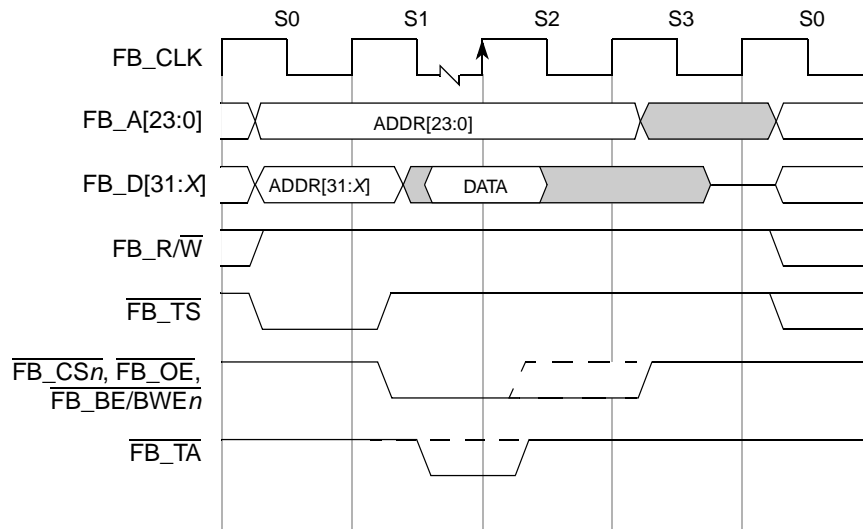


Figure 17-8. Basic Read-Bus Cycle

17.4.5.2 Basic Write Bus Cycle

During a write cycle, the device sends data to memory or to a peripheral device. Figure 17-9 shows the write cycle flowchart.

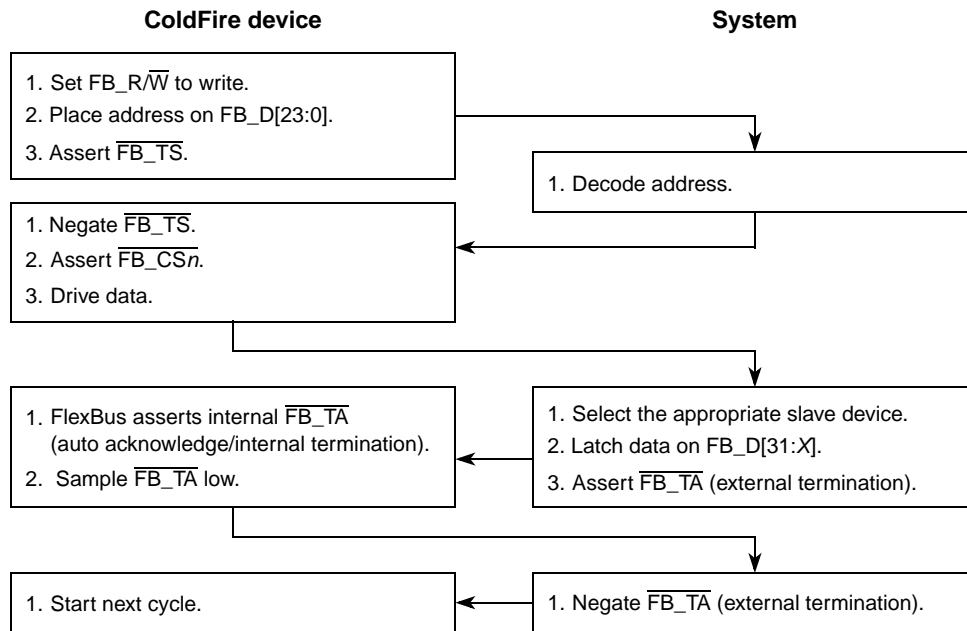


Figure 17-9. Write-Cycle Flowchart

Figure 17-10 shows the write cycle timing diagram.

NOTE

The address and data busses are muxed between the FlexBus and SDRAM controller. At the end of the write bus cycles, the address signals are indeterminate.

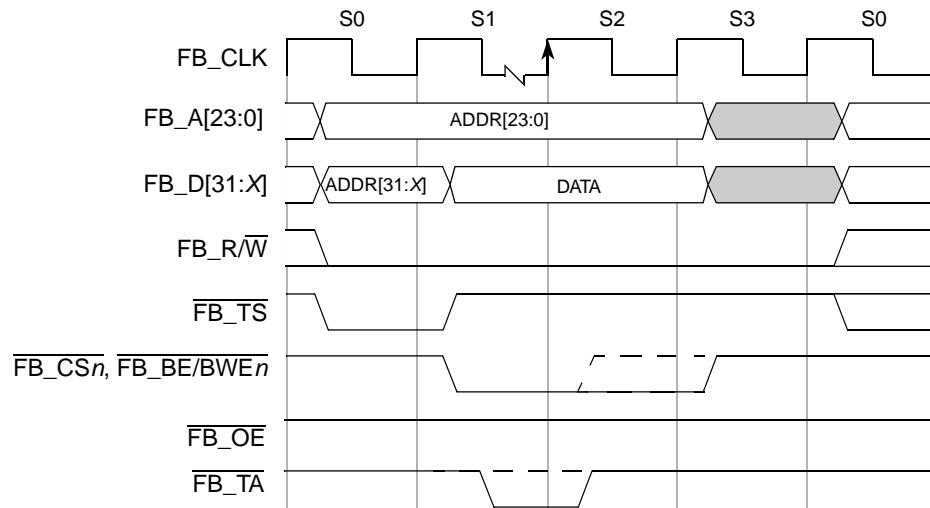


Figure 17-10. Basic Write-Bus Cycle

17.4.5.3 Bus Cycle Sizing

This section shows timing diagrams for various port size scenarios. Figure 17-11 illustrates the basic byte read transfer to an 8-bit device with no wait states. The address is driven on the FB_A[23:8] bus throughout the bus cycle. The external device returns the read data on FB_D[31:24] and may tristate the data line or continue driving the data one clock after FB_TA is sampled asserted.

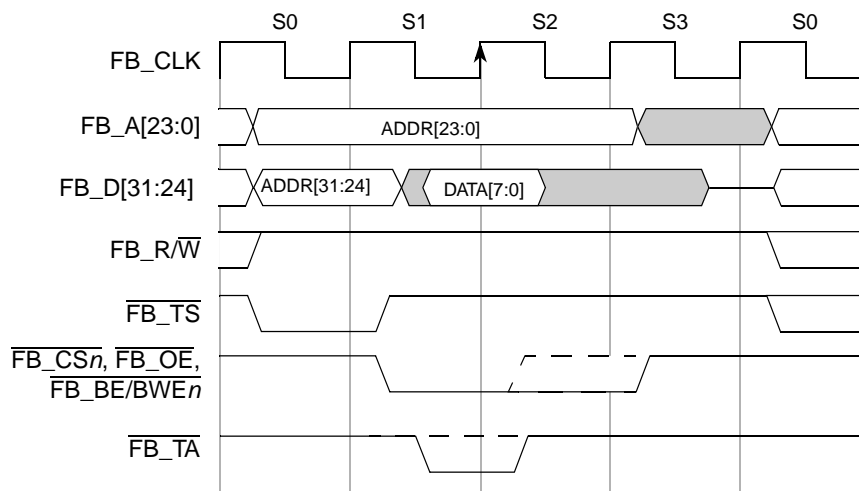


Figure 17-11. Single Byte-Read Transfer

Figure 17-12 shows the similar configuration for a write transfer. The data is driven from the second clock on FB_D[31:24].

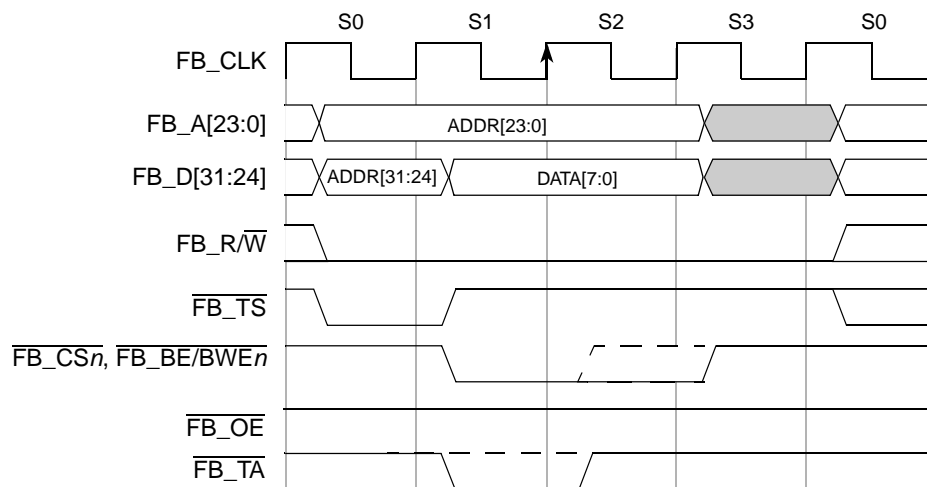


Figure 17-12. Single Byte-Write Transfer

Figure 17-13 illustrates the basic word read transfer to a 16-bit device with no wait states. The address is driven on the FB_A[23:8 :0] bus throughout the bus cycle. The external device returns the read data on FB_D[31:16], and may tristate the data line or continue driving the data one clock after FB_TA is sampled asserted.

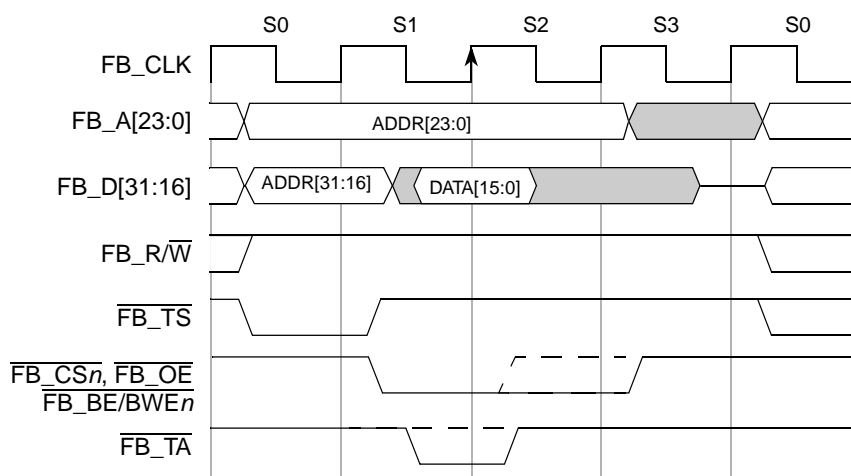


Figure 17-13. Single Word-Read Transfer

Figure 17-14 shows the similar configuration for a write transfer. The data is driven from the second clock on FB_D[31:16].

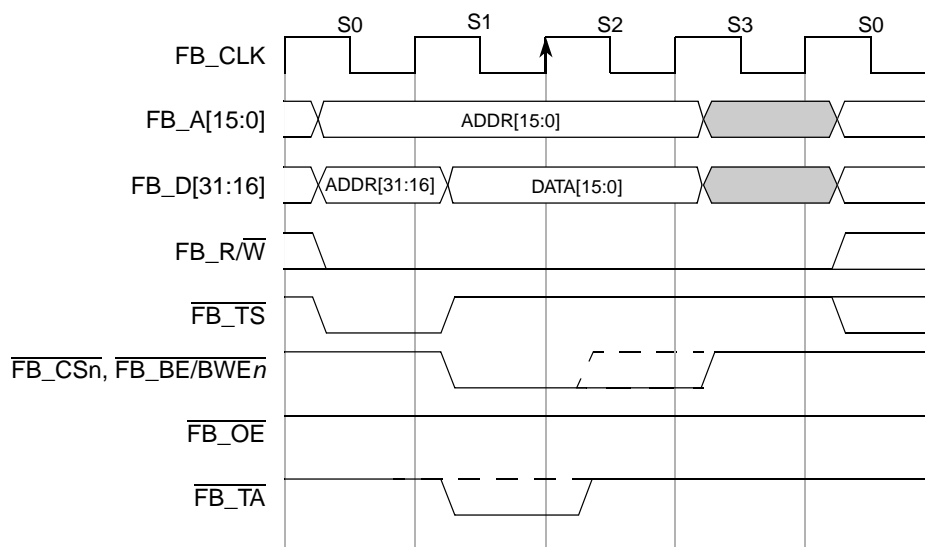


Figure 17-14. Single Word-Write Transfer

Figure 17-15 depicts a longword read from a 32-bit device.

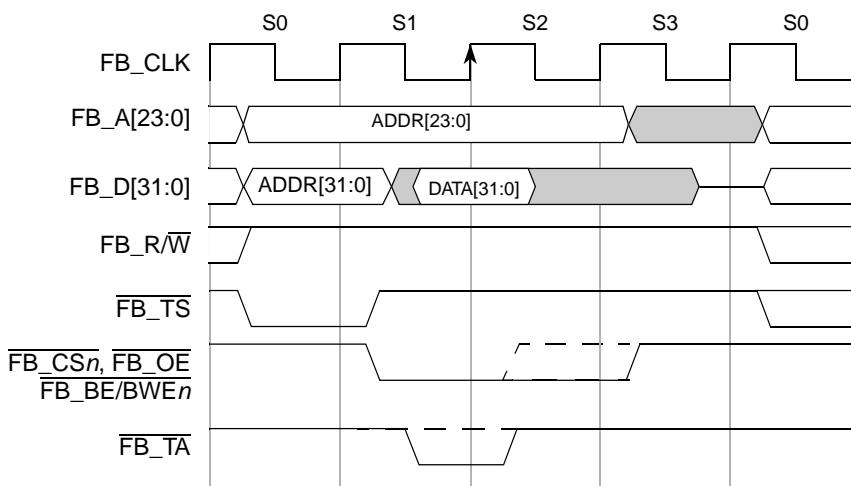


Figure 17-15. Longword-Read Transfer

Figure 17-16 illustrates the longword write to a 32-bit device.

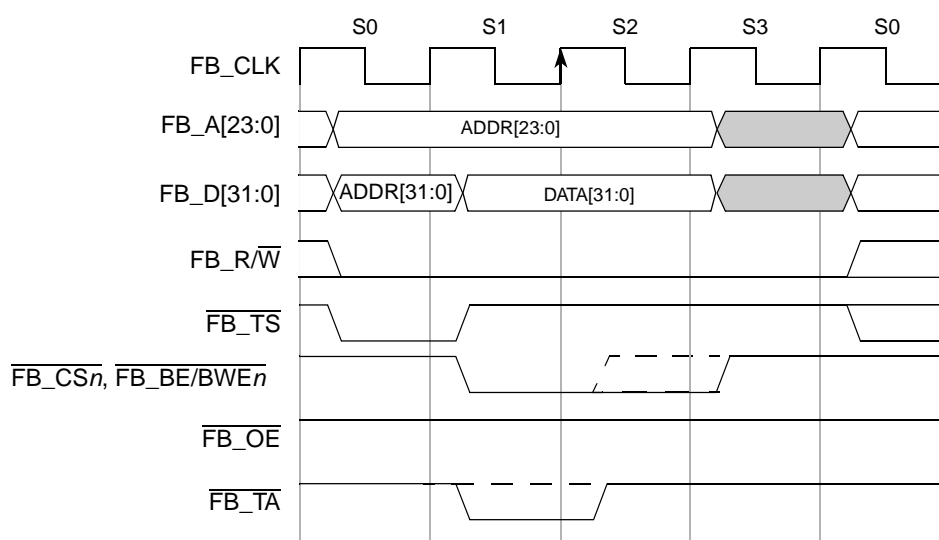


Figure 17-16. Longword-Write Transfer

17.4.5.4 Timing Variations

The FlexBus module has several features that can change the timing characteristics of a basic read- or write-bus cycle to provide additional address setup, address hold, and time for a device to provide or latch data.

17.4.5.4.1 Wait States

Wait states can be inserted before each beat of a transfer by programming the CSCR_n registers. Wait states can give the peripheral or memory more time to return read data or sample write data.

Figure 17-17 and Figure 17-18 show the basic read and write bus cycles (also shown in Figure 17-8 and Figure 17-13) with the default of no wait states.

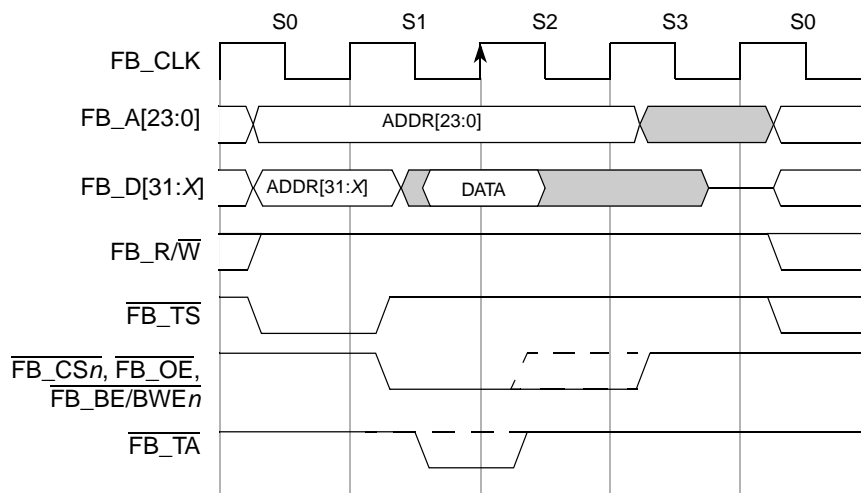


Figure 17-17. Basic Read-Bus Cycle (No Wait States)

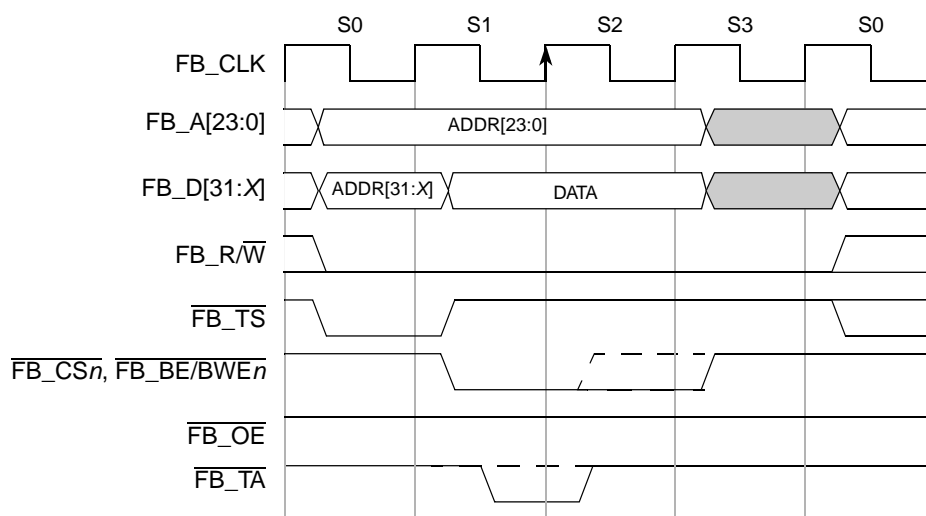


Figure 17-18. Basic Write-Bus Cycle (No Wait States)

If wait states are used, the S1 state repeats continuously until the the chip-select auto-acknowledge unit asserts internal transfer acknowledge or the external $\overline{\text{FB_TA}}$ is recognized as asserted. Figure 17-19 and Figure 17-20 show a read and write cycle with one wait state.

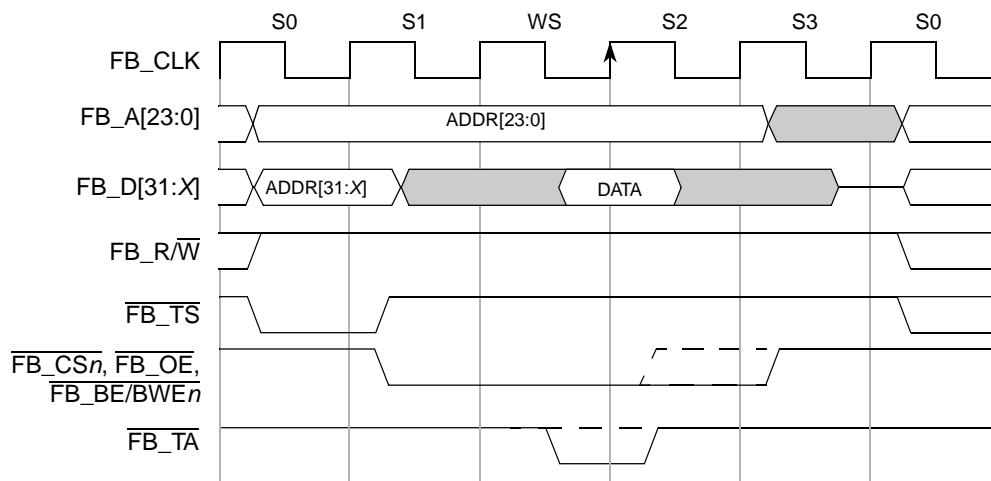


Figure 17-19. Read-Bus Cycle (One Wait State)

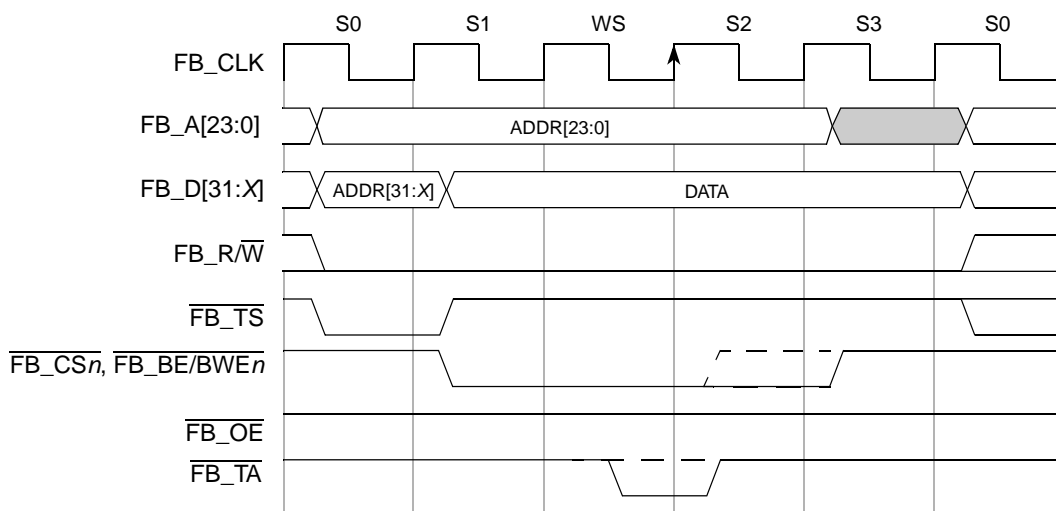


Figure 17-20. Write-Bus Cycle (One Wait State)

17.4.5.4.2 Address Setup and Hold

The timing of the assertion and negation of the chip selects, byte selects, and output enable can be programmed on a chip-select basis. Each chip-select can be programmed to assert one to four clocks after

transfer start ($\overline{\text{FB_TS}}$) is asserted. Figure 17-21 and Figure 17-22 show read- and write-bus cycles with two clocks of address setup.

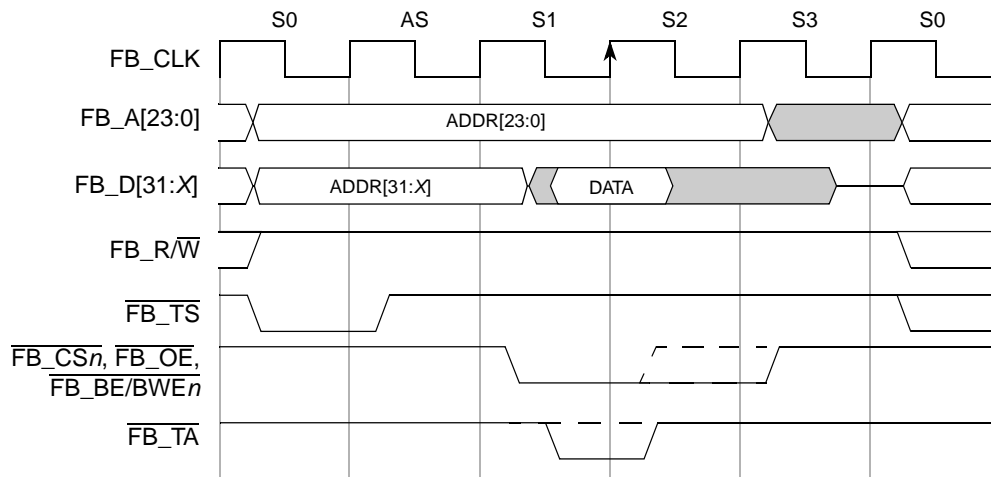


Figure 17-21. Read-Bus Cycle with Two-Clock Address Setup (No Wait States)

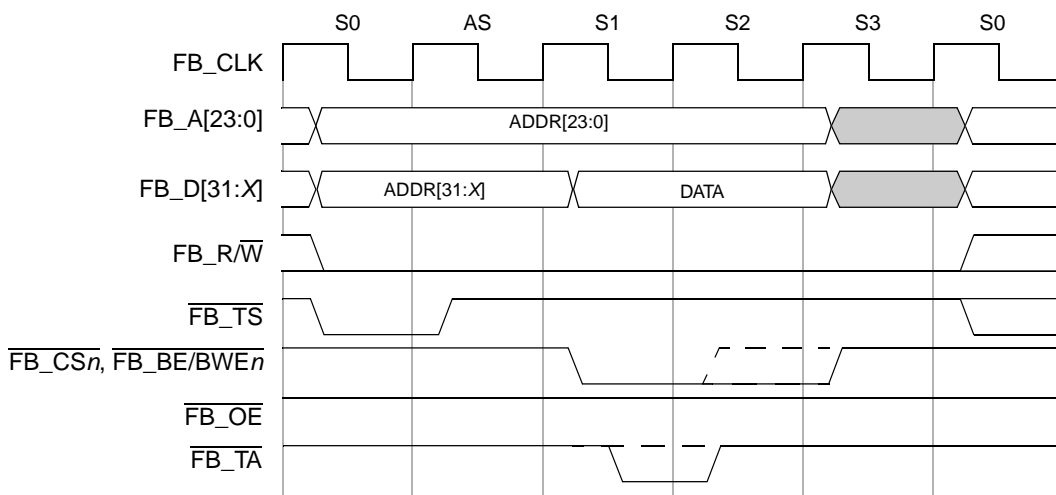


Figure 17-22. Write-Bus Cycle with Two Clock Address Setup (No Wait States)

In addition to address setup, a programmable address hold option for each chip select exists. Address and attributes can be held one to four clocks after chip-select, byte-selects, and output-enable negate.

Figure 17-23 and Figure 17-24 show read and write bus cycles with two clocks of address hold.

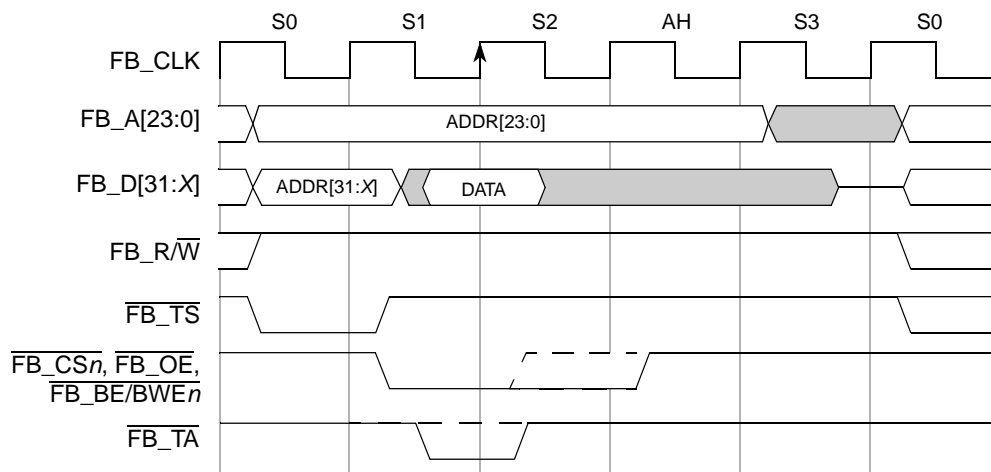


Figure 17-23. Read Cycle with Two-Clock Address Hold (No Wait States)

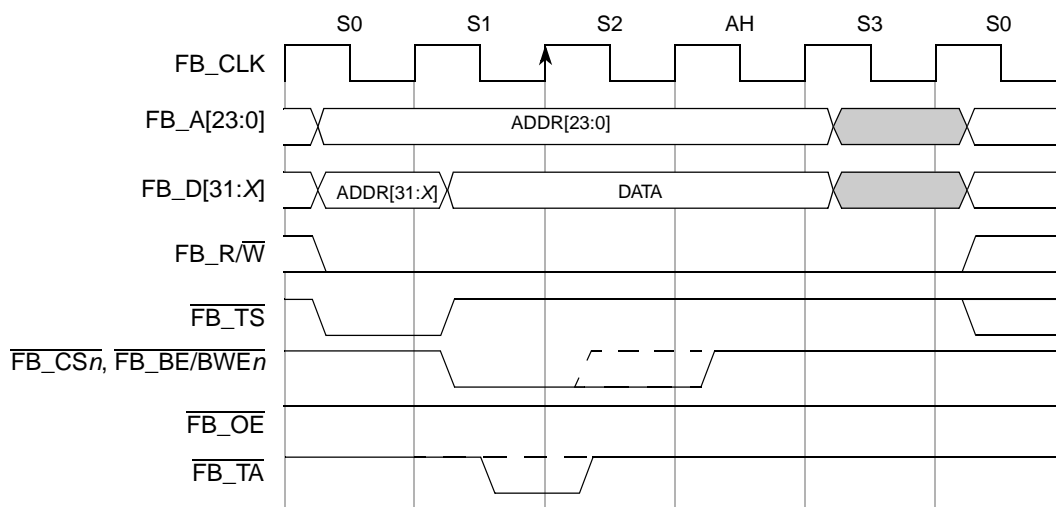


Figure 17-24. Write Cycle with Two-Clock Address Hold (No Wait States)

Figure 17-25 shows a bus cycle using address setup, wait states, and address hold.

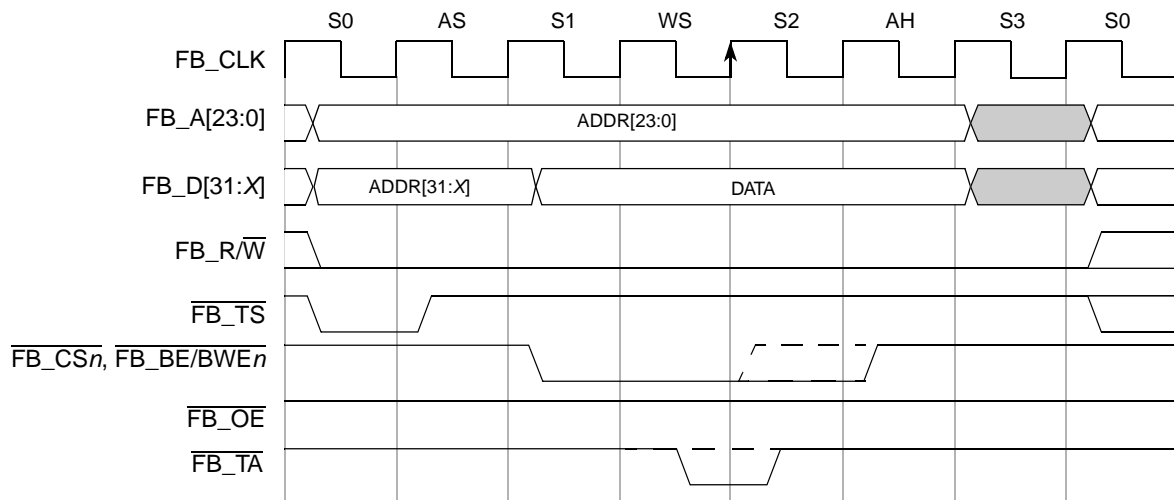


Figure 17-25. Write Cycle with Two-Clock Address Setup and Two-Clock Hold (One Wait State)

17.4.6 Burst Cycles

The device can be programmed to initiate burst cycles if its transfer size exceeds the port size of the selected destination. With bursting disabled, any transfer larger than the port size breaks into multiple individual transfers. With bursting enabled, an access larger than port size results in a burst cycle of multiple beats. Table 17-8 shows the result of such transfer translations.

Table 17-8. Transfer Size and Port Size Translation

Port Size PS[1:0]	Transfer Size	Burst-Inhibited: Number of Transfers Burst Enabled: Number of Beats
01 (8-bit)	word	2
	longword	4
	line	16
1x (16-bit)	longword	2
	line	8
00 (32-bit)	line	4

The FlexBus can support 2-1-1-1 burst cycles to maximize system performance. Delaying termination of the cycle can add wait states. If internal termination is used, different wait state counters can be used for the first access and the following beats.

The CSCR_n registers enable bursting for reads, writes, or both. Memory spaces can be declared burst-inhibited for reads and writes by clearing the appropriate CSCR_n[BSTR,BSTW] bits.

Figure 17-26 shows a longword read to an 8-bit device programmed for burst enable. The transfer results in a 4-beat burst and the data is driven on FB_D[31:24].

NOTE

Address lines increment only during internally-terminated burst cycles. The first address is driven throughout the entire burst for externally-terminated cycles.

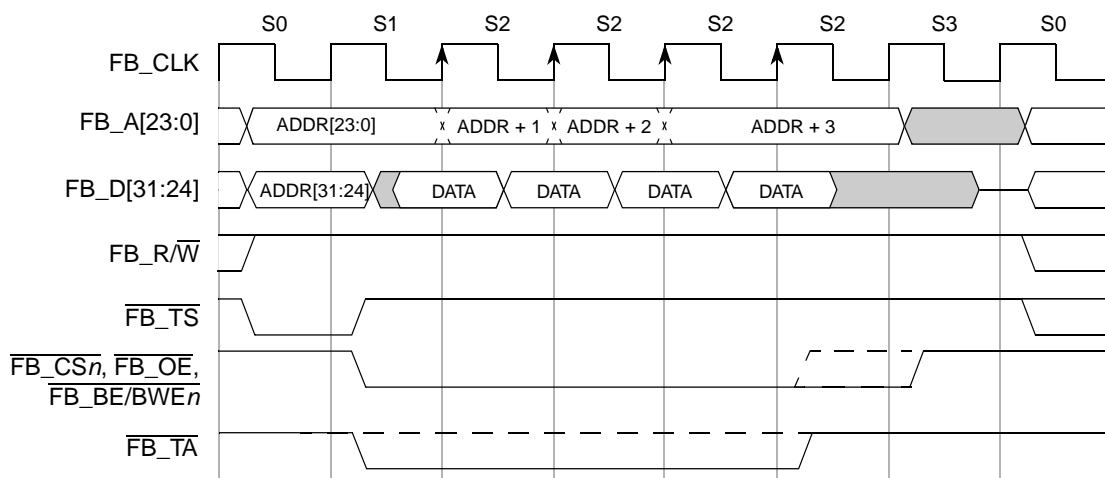


Figure 17-26. Longword-Read Burst from 8-Bit Port 2-1-1-1 (No Wait States)

Figure 17-27 shows a longword write to an 8-bit device with burst enabled. The transfer results in a 4-beat burst and the data is driven on FB_D[31:24].

NOTE

The first beat of any write burst cycle has at least one wait state. If the bus cycle is programmed for zero wait states ($CSCR_n[WS] = 0$), one wait state is added. Otherwise, the programmed number of wait states are used.

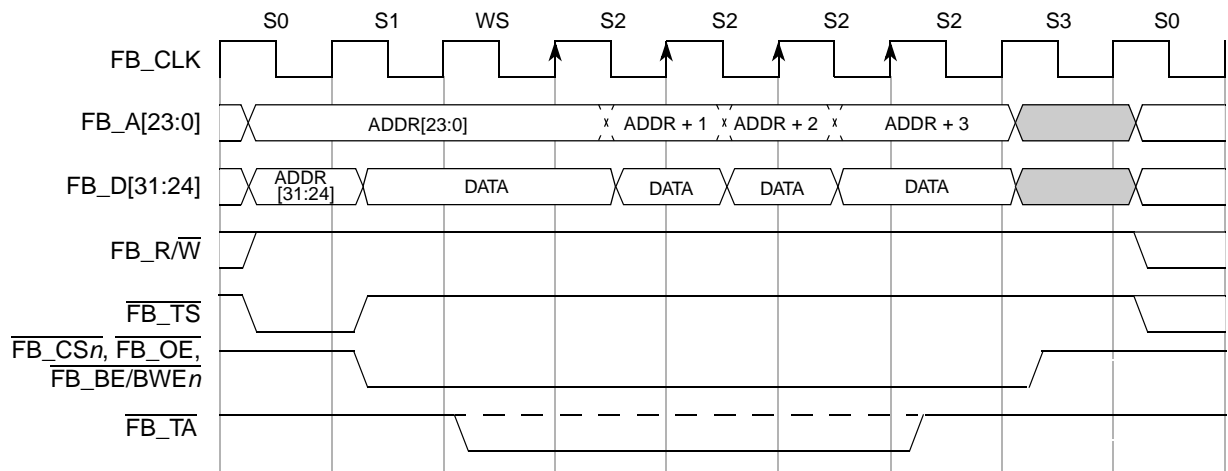


Figure 17-27. Longword-Write Burst to 8-Bit Port 3-1-1-1 (No Wait States)

Figure 17-28 shows a longword read from an 8-bit device with burst inhibited. The transfer results in four individual transfers.

NOTE

There is an extra clock of address setup (AS) for each burst-inhibited transfer between states S0 and S1.

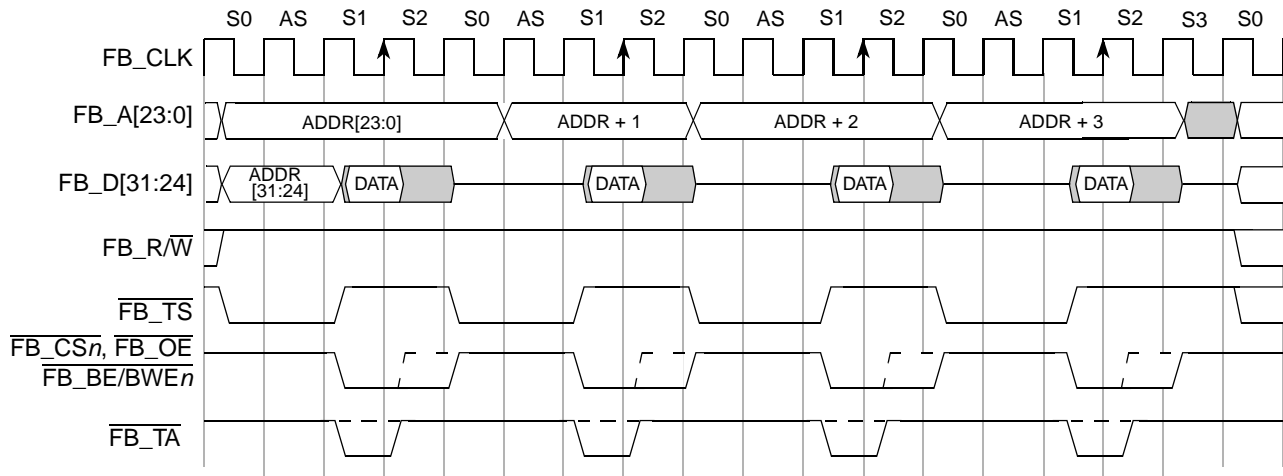


Figure 17-28. Longword-Read Burst-Inhibited from 8-Bit Port (No Wait States)

Figure 17-29 shows a longword write to an 8-bit device with burst inhibited. The transfer results in four individual transfers.

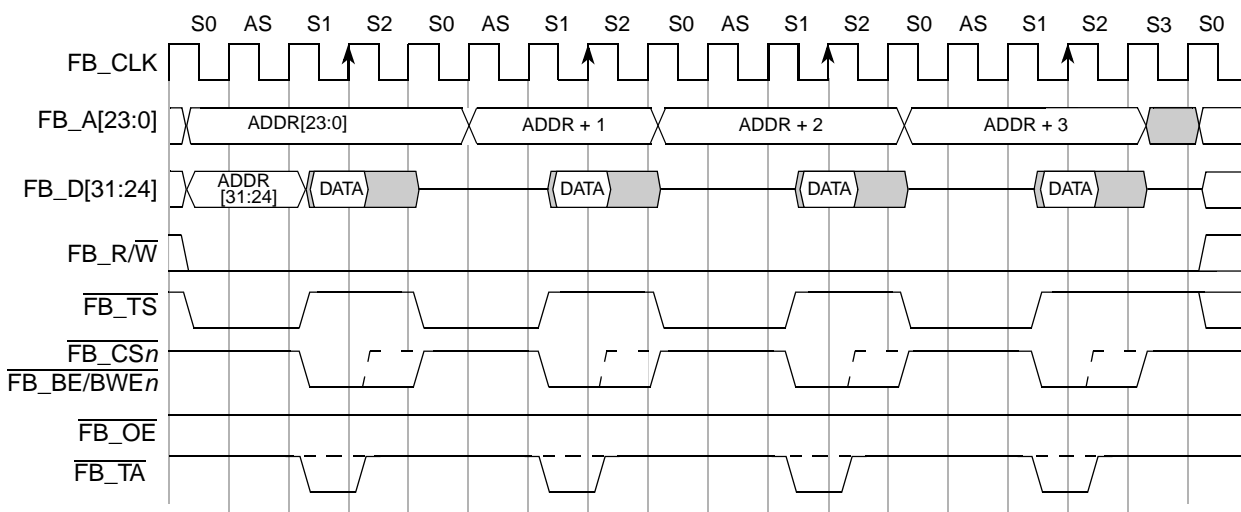


Figure 17-29. Longword-Write Burst-Inhibited to 8-Bit Port (No Wait States)

Figure 17-30 illustrates another read burst transfer, but in this case a wait state is added between individual beats.

NOTE

CSCR_n[WS] determines the number of wait states in the first beat.
However, for subsequent beats, the CSCR_n[WS] (or CSCR_n[SWS] if CSCR_n[SWSEN] is set) determines the number of wait states.

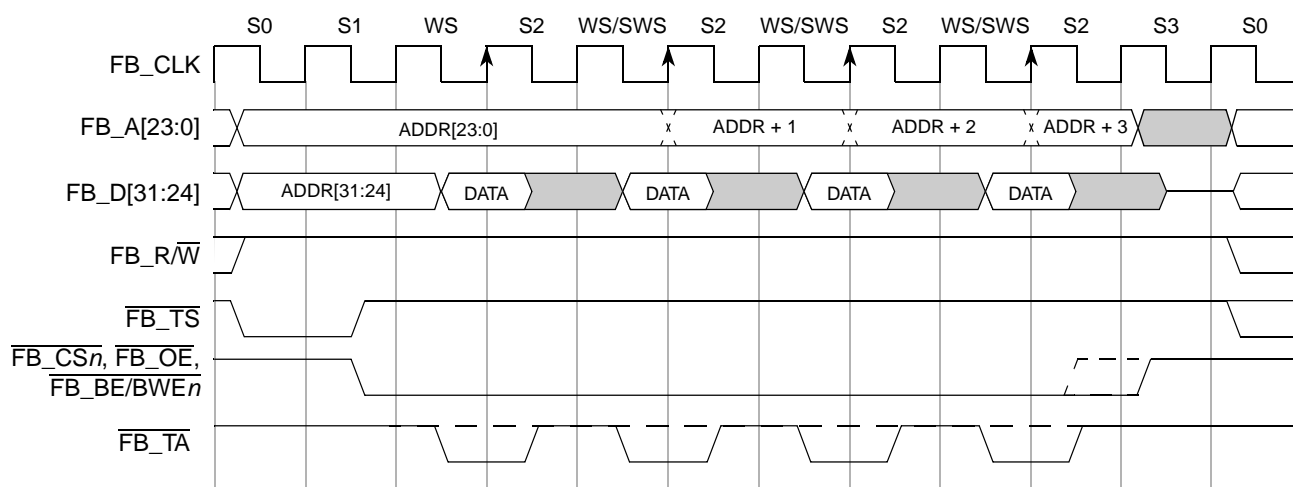


Figure 17-30. Longword-Read Burst from 8-Bit Port 3-2-2-2 (One Wait State)

Figure 17-30 illustrates a write burst transfer with one wait state.

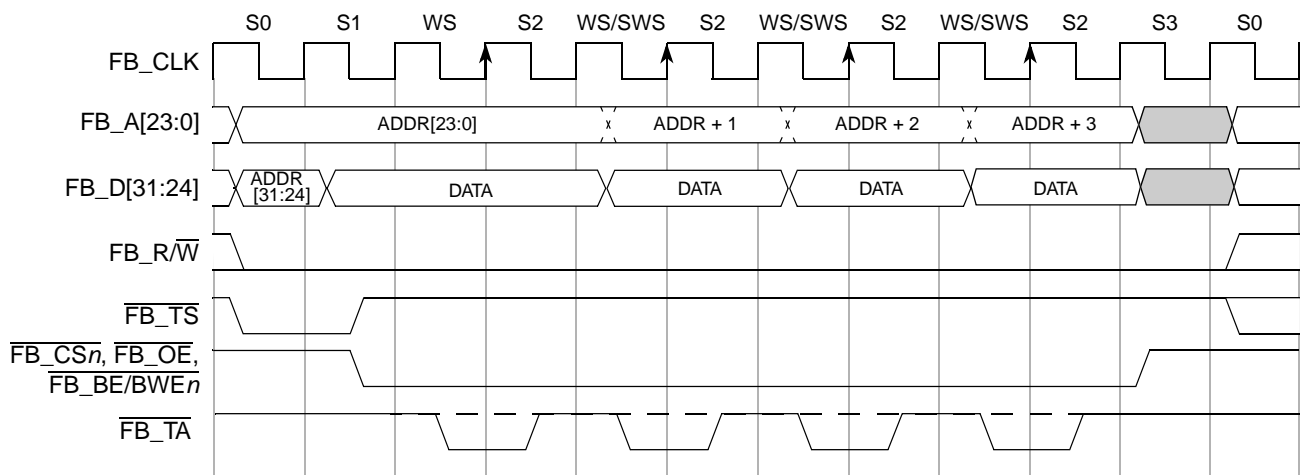
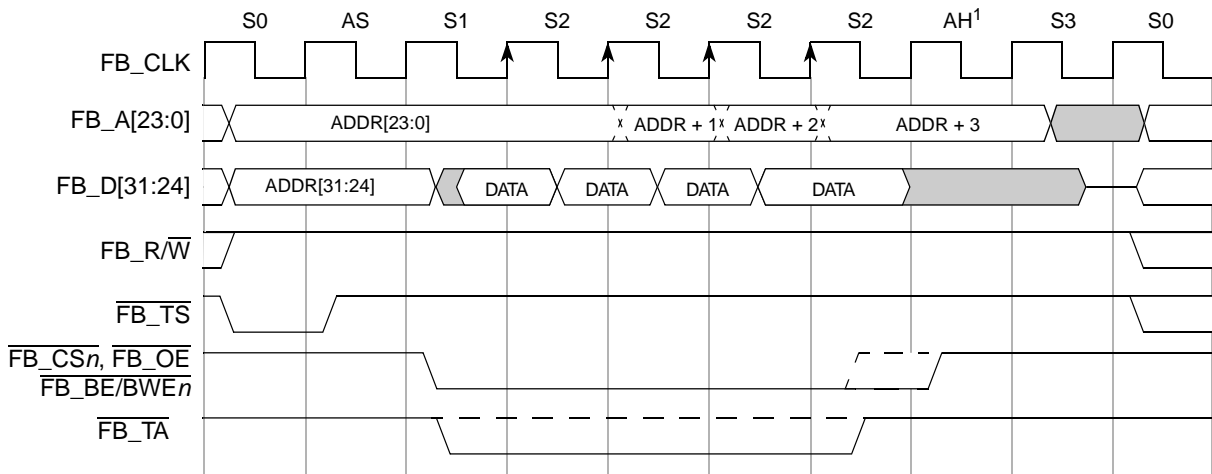


Figure 17-31. Longword-Write Burst to 8-Bit Port 3-2-2-2 (One Wait State)

If address setup and hold are used, only the first and last beat of the burst cycle are affected. Figure 17-32 shows a read cycle with one clock of address setup and address hold.

NOTE

When using internal termination in this scenario ($CSCR_n[AA] = 1$), the address increments after the clock-edge boundary. The attached device must be able to account for this, or a wait state must be added.



¹ The address hold time depends on the setting of $CSCR_n[AA]$. See Section 17.3.3, "Chip-Select Control Registers (CSCR0 – CSCR5)", for more details.

Figure 17-32. Longword-Read Burst from 8-Bit Port 3-1-1-1 (Address Setup and Hold)

Figure 17-33 shows a write cycle with one clock of address setup and address hold.

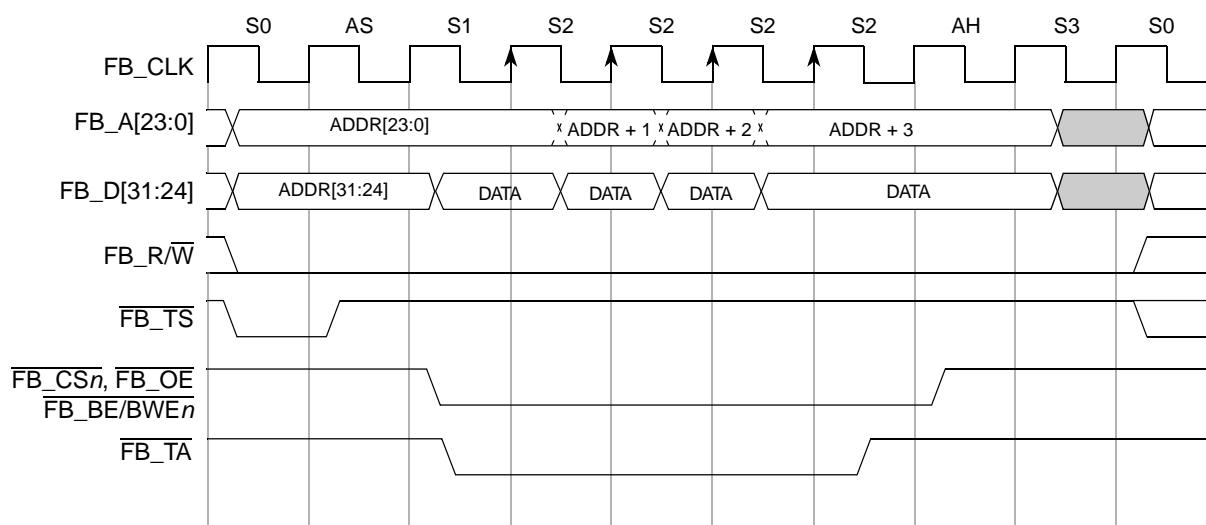


Figure 17-33. Longword-Write Burst to 8-Bit Port 3-1-1-1 (Address Setup and Hold)

17.4.7 Misaligned Operands

Because operands, unlike opcodes, can reside at any byte boundary, they are allowed to be misaligned.

- Byte operand is properly aligned at any address
- Word operand is misaligned at an odd address
- Longword is misaligned at any address not a multiple of four

Although the processor enforces no alignment restrictions for data operands (including program counter (PC) relative data addressing), misaligned operands require additional bus cycles.

Instruction words and extension words (opcodes) must reside on word boundaries. Attempting to prefetch a misaligned instruction word causes an address-error exception.

The processor core converts misaligned, cache-inhibited operand accesses to multiple aligned accesses.

[Example 17-1](#) shows the transfer of a longword operand from a byte address to a 32-bit port. First, a byte transfers at an offset of 0x1. The slave device supplies the byte and acknowledges the data transfer. When the processor starts the second cycle, a word transfers with a byte offset of 0x2. The next two bytes are transferred in this cycle. In the third cycle, byte 3 transfers. The byte offset is now 0x0, the port supplies the final byte, and the operation completes.

	31	24 23	16 15	8 7	0	FB_A[2:0]
Transfer 1	—	Byte 0	—	—	—	001
Transfer 2	—	—	Byte 1	Byte 2	—	010
Transfer 3	Byte 3	—	—	—	—	100

Example 17-1. A Misaligned Longword Transfer (32-Bit Port)

If an operand is cacheable and is misaligned across a cache-line boundary, both lines are loaded into the cache. The example in [Example 17-2](#) differs from the one in [Example 17-1](#) because the operand is word-sized and the transfer takes only two bus cycles.

	31	24 23	16 15	8 7	0	FB_A[2:0]
Transfer 1	—	—	—	Byte 0	—	001
Transfer 2	Byte 0	—	—	—	—	100

Example 17-2. A Misaligned Word Transfer (32-Bit Port)

17.4.8 Bus Errors

The ColdFire device has no bus monitor. If the auto-acknowledge feature is not enabled for the address that generates the error, the bus cycle can be terminated by asserting $\overline{\text{FB_TA}}$ or by using the software watchdog timer. If the processor must manage a bus error differently, asserting an interrupt to the core along with $\overline{\text{FB_TA}}$ when the bus error occurs can invoke an interrupt handler.

Chapter 18

SDRAM Controller (SDRAMC)

18.1 Introduction

This chapter describes configuration and operation of the synchronous DRAM (SDRAM) controller. It begins with a general description and brief glossary and includes a description of signals involved in DRAM operations. The remainder of the chapter describes the programming model and signal timing, as well as the command set required for synchronous operations. It also includes examples to better understand how to configure the DRAM controller for synchronous operations.

NOTE

Unless otherwise noted, in this chapter clock refers to the system clock ($f_{\text{sys}/2}$).

The external data bus is shared between the FlexBus module and the SDRAM controller. When the SDRAM controller is in SDR mode (DRAMSEL = 1), the data bus is switched dynamically between the SDRAM controller and the FlexBus module. However, when the SDRAM controller is in DDR mode (DRAMSEL = 0), D[31:16] is dedicated to the SDRAM data bus and D[15:0] is dedicated to the FlexBus data bus.

In this chapter, the SDRAM data bus signals are named SD_D[31:0]. However, because these signals share external pins with the FlexBus, the pin names on the device are D[31:0].

18.1.1 Block Diagram

Block diagram of the SDRAM controller:

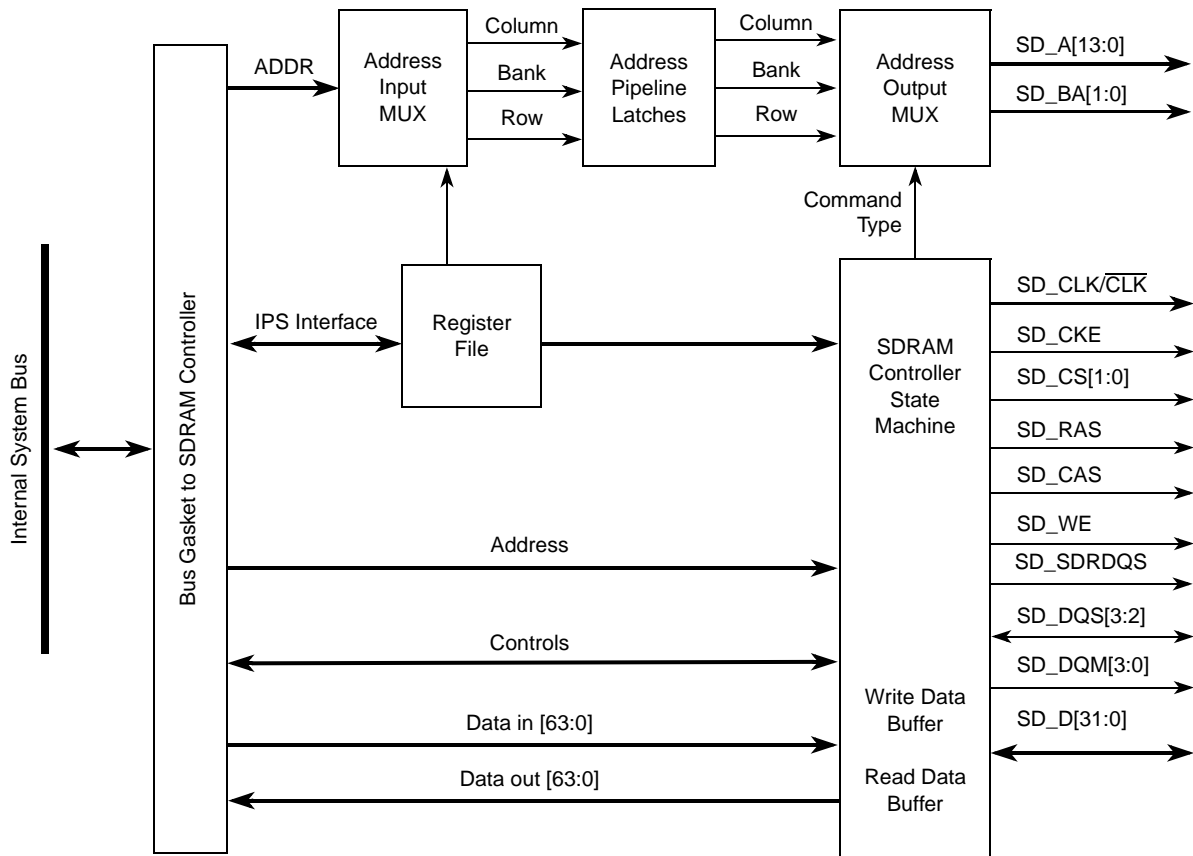


Figure 18-1. SDRAM Controller Block Diagram

18.1.2 Features

The SDRAM controller contains:

- Supports standard SDRAM (single data rate, or SDR) and dual data rate (DDR) SDRAM; one or the other, not mixed.
- Support for lower-power/mobile DDR SDRAM.
- Dynamic 16- or 32-bit fixed memory data port width.
- 16 bytes critical word first burst transfer. Supports sequential address order only.
- Up to 14 lines of row address, up to 12 (in 32-bit bus mode) or 13 (in 16-bit bus mode) column address lines, 2 bits of bank address, and two pinned-out chip selects. The maximum row bits plus column bits equals 24 in 32-bit bus mode or 25 in 16-bit bus mode.
- Minimum memory configuration of 8 MByte
 - 11 bit row address (RA), 8 bit column address (CA), 2 bit bank address (BA), 32-bit bus, one chip select

- 11 bit row address (RA), 9 bit column address (CA), 2 bit bank address (BA), 16-bit bus, one chip select
- Supports up to 512 MByte of memory.
 - 24/25 bits RA+CA, 2 bits BA, 32/16-bit bus, two chip selects
- Supports page mode for decreased latency and higher bandwidth; remembers one active row for each bank; four independent active rows per each chip select.
- Programmable refresh interval timer.
- Supports sleep mode and self-refresh mode.
- Error detect and parity check are not supported.
- The SDRAM controller does not include a dedicated I²C interface to access memory module (DIMM) serial presence detect EEPROM. If needed, this must be managed by one of the on-chip I²C channels external to the SDRAM controller.
- Read clock recovery block

18.1.3 Terminology

The following terminology is used in this chapter:

- SDRAM block: Any group of DRAM memories selected by one of the $\overline{\text{SD_CS}}$ signals. Therefore, the SDRAMC can support up to two independent memory blocks. The base address of each block is programmed in the SDRAM chip-select configuration registers.
- SDRAM bank: An internal partition in an SDRAM device. For example, a 64-Mbit SDRAM component might be configured as four 512K x 32 banks. Banks are selected through the SD_BA[1:0] signals.
- SDRAM: RAMs that operate like asynchronous DRAMs but with a synchronous clock, a pipelined, multiple-bank architecture, and a faster speed.

18.2 External Signal Description

This section introduces the signal names used in this chapter.

Table 18-1. SDRAM Interface—Detailed Signal Descriptions

Signal	I/O	Description
SD_A[13:0]	O	Memory multiplexed row/column address. Provides the row address for ACTV commands, and the column address and auto-precharge bit for READ/WRITE commands, to select one location out of the memory array in the respective bank. A10 is sampled during a precharge command to determine whether the precharge applies to one bank (A10 negated) or all banks (A10 asserted). If only one bank is to be precharged, the bank is selected by SD_BA[1:0]. The address outputs also provide the opcode during a MODE REGISTER SET command. SD_BA[1:0] signals define which mode register is loaded during the MODE REGISTER SET (MRS). A12 is used on device densities of 256 Mb and above.
		Timing Assertion/Negation — Occurs synchronously with SD_CLK

Table 18-1. SDRAM Interface—Detailed Signal Descriptions (continued)

Signal	I/O	Description	
SD_BA[1:0]	O	Memory bank address. Define which bank an ACTV, READ, WRITE, or PRECHARGE command is being applied. It is also used to select the SDRAM internal mode register during power-up initialization.	
		Timing	Assertion/Negation — Occurs synchronously with SD_CLK
SD_CAS	O	Column address strobe/command input. Along with $\overline{\text{SD_CS}}$, $\overline{\text{SD_RAS}}$, and $\overline{\text{SD_WE}}$, defines the current command.	
		State Meaning	See Table 18-12 for the SDRAM commands.
		Timing	Assertion/Negation — Occurs synchronously with SD_CLK
SD_RAS	O	Row address strobe/command input. Along with $\overline{\text{SD_CS}}$, $\overline{\text{SD_CAS}}$, and $\overline{\text{SD_WE}}$, defines the current command.	
		State Meaning	See Table 18-12 for SDRAM commands.
		Timing	Assertion/Negation — Occurs synchronously with SD_CLK.
SD_CKE	O	Clock enable. SD_CKE must be maintained high throughout READ and WRITE accesses. SD_CKE negates to put the SDRAM into low-power, self-refresh mode. Input buffers, excluding SD_CLK, $\overline{\text{SD_CLK}}$, and SD_CKE, are disabled during self-refresh.	
		State Meaning	Asserted — Activates internal clock signals and device input buffers and output drivers. Negated — Deactivates internal clock signals and device input buffers and output drivers.
		Timing	Assertion — Asynchronous for self-refresh exit and for output disable Negation — Occurs synchronously with SD_CLK
$\overline{\text{SD_CLK}}$ SD_CLK	O	SD_CLK and $\overline{\text{SD_CLK}}$ are differential clock outputs. All address and control output signals are sent on the crossing of the positive edge of SD_CLK and the negative edge of $\overline{\text{SD_CLK}}$. Output data is referenced to the crossing of SD_CLK and $\overline{\text{SD_CLK}}$ (both directions of crossing).	
		Timing	Command signals occur synchronously with the rising edge of this clock. Data signals can change on the rising and falling edge of the clock.
$\overline{\text{SD_CS}}$ [1:0]	O	$\overline{\text{SD_CS}}$ provides external bank selection on systems with multiple banks. $\overline{\text{SD_CS}}$ is considered part of the command code.	
		State Meaning	Asserted — Commands for the selected chip occur Negated — All commands are masked.
		Timing	Assertion/Negation — Occurs synchronously with SD_CLK
SD_DATA[31:0]	I/O	Data bus. In 16-bit DDR configuration, the memory device data bus is connected to SD_D[31:16] bits.	
		Timing	Assertion/Negation — Occurs on crossing of SD_CLK and $\overline{\text{SD_CLK}}$. High Impedance - Depending on the OE_RULE bit in SDCFG1, the SD_DATA bus can be in high impedance until a write occurs or only when a read occurs.

Table 18-1. SDRAM Interface—Detailed Signal Descriptions (continued)

Signal	I/O	Description
$\overline{\text{SD_DQM}}[3:0]$	O	Output mask signal for write data. During reads, $\overline{\text{SD_DQM}}$ may be driven high, low, or floating. The address correspondence: SD_DQM3 - SD_D[31:24] SD_DQM2 - SD_D[23:16] SD_DQM1 - SD_D[15:8] SD_DQM0 - SD_D[7:0]
		State Meaning Asserted — Data is written to SDRAM Negation — Data is masked
		Timing Assertion/Negation — Occurs on crossing of SD_CLK and $\overline{\text{SD_CLK}}$.
SD_DQS[3:2]	I/O	Data strobes that indicate valid read/write data. (Edge-aligned with read data, centered with write data.) The DQS frequency equals the memory clock frequency. Data is normally 1/4 memory clock period after a DQS transition. For DDR operation, there is data following each DQS edge (rising and falling); for SDR operation, valid data follows the rising edges only. The address correspondence: SD_DQS3 - SD_D[31:24] SD_DQS2 - SD_D[23:16] Note: If a read is attempted from a DDR SDRAM chip select when there is no memory to respond with the appropriate SD_DQS pulses, the bus cycle hangs. Because there is no high level bus monitor on the device, a reset is the only way to exit this error condition.
		State Meaning Asserted — Similar to a clock signal, the edges are more important than being asserted or negated. High impedance — Depending on the SDCFG1[OE_RULE] bit, the SD_DQS can be in high impedance until a write is occurring or only when a read is occurring.
		Timing Assertion/Negation — Occurs on crossing of SD_CLK and $\overline{\text{SD_CLK}}$.
SD_SDRDQS	O	SDR data strobe. Generated by the memory controller in SDR mode, to mimic the DQS generated by DDR memories during reads. It should be routed out and connected back to the SD_DQS inputs.
		State Meaning Asserted— Similar to a clock signal, the edges are more important than being asserted or negated.
		Timing Assertion/Negation—Occurs on crossing of SD_CLK and $\overline{\text{SD_CLK}}$.
$\overline{\text{SD_WE}}$	O	Command input. Along with $\overline{\text{SD_CS}}$, $\overline{\text{SD_CAS}}$, and $\overline{\text{SD_RAS}}$ defines the current command.
		State Meaning Please see Table 18-12 for SDRAM commands.
		Timing Assertion/Negation— Occurs synchronously with SD_CLK.

18.3 Interface Recommendations

18.3.1 Supported Memory Configurations

The SDRAM controller supports up to 14 row addresses and up to (13 in 16-bit bus mode) column addresses. However, the maximum row and column addresses are not simultaneously supported. The number of row and column addresses must be less than or equal to 24 (25 in 16-bit bus mode). In addition to row/column address lines, there are always two row bank address bits. Therefore, the greatest possible address space accessed using a single chip select is $2^{26} \times 32$ bit ($2^{27} \times 16$ bit) or 256 MBytes.

Table 18-5 and Table 18-6 show the address multiplexing used by the memory controller for different configurations. When the SDRAM controller receives the internal module enable, it latches the internal bus address lines IA[27:0] (IA equals internal address) and multiplexes them into row, column, and bank addresses (RA, CA, and BA respectively). In 32-bit bus mode, IA[9:2] are used for CA[7:0]. In 16-bit mode, IA[9:1] are used for CA[8:0]. IA[11:10] are always used for BA[1:0], and IA[23:12] are always used for RA[11:0]. IA[27:24] can be used for additional row or column address bits, as needed. The additional row- or column-address bits are programmed via the SDCR[ADDR_MUX] bits.

NOTE

When the SDRAMC is configured to support an external 32-bit data bus. It is not possible to connect a smaller device(s) to only part of the SDRAM's data bus. For example, if 16-bit wide devices are used, then user must use two 16-bit devices connected as a 32-bit port.

Table 18-2. Address Multiplexing for 32-bit Bus Mode

SDCR[ADDR_MUX]	Internal Address Bits [27:24]			
	IA[27]	IA[26]	IA[25]	IA[24]
00	CA12	CA11	CA9	CA8
01	CA11	CA9	CA8	RA12
10	CA9	CA8	RA13	RA12
11	Reserved, do not use.			

Table 18-3. SDRAM Address Multiplexing in 32-bit Bus Mode

Device	Configuration	Row bit x Col bit x Banks	SDCR [ADDR_ MUX]	Internal Address						
				27	26	25	24	23–12	11–10	9–2
64 Mbits	2M x 32 bit	11 x 8 x 4	00	— ^{1,2}	—	—	—	RA11-0	BA1-0	CA7-0
	4M x 16 bit	12 x 8 x 4	00	—	—	—	—			
	8M x 8 bit	12 x 9 x 4	00	—	—	—	CA8			
		13 x 8 x 4	01	—	—	—	RA12			
	16M x 4 bit	12 x 10 x 4	00	—	—	CA9	CA8			
		13 x 9 x 4	01	—	—	CA8	RA12			

Table 18-3. SDRAM Address Multiplexing in 32-bit Bus Mode (continued)

Device	Configuration	Row bit x Col bit x Banks	SDCR [ADDR_ MUX]	Internal Address						
				27	26	25	24	23–12	11–10	9–2
128 Mbits	4M x 32 bit	12 x 8 x 4	00	—	—	—	—	RA11-0	BA1-0	CA7-0
		12 x 9 x 4	00	—	—	—	CA8			
	8M x 16 bit	13 x 8 x 4	01	—	—	—	RA12			
		12 x 10 x 4	00	—	—	CA9	CA8			
		13 x 9 x 4	01	—	—	CA8	RA12			
		14 x 8 x 4	10	—	—	RA13	RA12			
	16M x 8 bit	12 x 11 x 4	00	—	CA11	CA9	CA8			
		13 x 10 x 4	01	—	CA9	CA8	RA12			
		14 x 9 x 4	10	—	CA8	RA13	RA12			
		12 x 11 x 4	00	—	CA11	CA9	CA8			
256 Mbits	8M x 32 bit	12 x 9 x 4	00	—	—	—	CA8	RA11-0	BA1-0	CA7-0
		13 x 8 x 4	01	—	—	—	RA12			
	16M x 16 bit	12 x 10 x 4	00	—	—	CA9	CA8			
		13 x 9 x 4	01	—	—	CA8	RA12			
		14 x 8 x 4	10	—	—	RA13	RA12			
		12 x 11 x 4	00	—	CA11	CA9	CA8			
	32M x 8 bit	13 x 10 x 4	01	—	CA9	CA8	RA12			
		14 x 9 x 4	10	—	CA8	RA13	RA12			
		12 x 12 x 4	00	CA12	CA11	CA9	CA8			
	64M x 4 bit	13 x 11 x 4	01	CA11	CA9	CA8	RA12			
		14 x 10 x 4	10	CA9	CA8	RA13	RA12			
		12 x 10 x 4	00	—	—	CA9	CA8			
512 Mbits	16M x 32 bit	13 x 9 x 4	01	—	—	CA8	RA12			
		14 x 8 x 4	10	—	—	RA13	RA12			
		12 x 11 x 4	00	—	CA11	CA9	CA8			
	32 M x 16 bit	13 x 10 x 4	01	—	CA9	CA8	RA12			
		14 x 9 x 4	10	—	CA8	RA13	RA12			
		12 x 12 x 4	00	CA12	CA11	CA9	CA8			
	64M x 8 bit	13 x 11 x 4	01	CA11	CA9	CA8	RA12			
		14 x 10 x 4	10	CA9	CA8	RA13	RA12			
		12 x 10 x 4	00	—	—	CA9	CA8			
		13 x 9 x 4	01	—	—	CA8	RA12			

Table 18-3. SDRAM Address Multiplexing in 32-bit Bus Mode (continued)

Device	Configuration	Row bit x Col bit x Banks	SDCR [ADDR_ MUX]	Internal Address						
				27	26	25	24	23–12	11–10	9–2
1 Gbits	32M x 32 bit	12 x 11 x 4	00	—	CA11	CA9	CA8	RA11-0	BA1-0	CA7-0
		13 x 10 x 4	01	—	CA9	CA8	RA12			
		14 x 9 x 4	10	—	CA8	RA13	RA12			
	64M x 16 bit	12 x 12 x 4	00	CA12	CA11	CA9	CA8			
		13 x 11 x 4	01	CA11	CA9	CA8	RA12			
		14 x 10 x 4	10	CA9	CA8	RA13	RA12			
2 Gbits	64M x 32 bit	12 x 12 x 4	00	CA12	CA11	CA9	CA8	RA11-0	BA1-0	CA7-0
		13 x 11 x 4	01	CA11	CA9	CA8	RA12			
		14 x 10 x 4	10	CA9	CA8	RA13	RA12			

¹ All SD_A[13:0] bits are generated on every access, but only the bits actually used by the memory are shown.

² All column address (CA) bits in this table are physical column address lines. The SDRAM controller inserts an extra bit CA10 to control the precharge option.

Table 18-4. Address Multiplexing for 16-bit Bus Mode

SDCR[ADDR_MUX]	Internal Address Bits [27:24]			
	IA[27]	IA[26]	IA[25]	IA[24]
00	CA13	CA12	CA11	CA9
01	CA12	CA11	CA9	RA12
10	CA11	CA9	RA13	RA12
11	Reserved. Do Not Use.			

Table 18-5. SDRAM-Address Multiplexing in 16-bit Bus Mode

Device	Configuration	Row bit x Col bit x Banks	SDCR [ADDR_ MUX]	Internal Address						
				27	26	25	24	23 – 12	11 – 10	9 – 1
64 Mbits	4M x 16 bit	11 x 9 x 4	00	— ^{1,2}	—	—	—	RA11-0	BA1-0	CA8-0
	8M x 8 bit	12 x 9 x 4	00	—	—	—	—			
	16M x 4 bit	12 x 10 x 4	00	—	—	—	CA9			
		13 x 9 x 4	01	—	—	—	RA12			

Table 18-5. SDRAM-Address Multiplexing in 16-bit Bus Mode (continued)

Device	Configuration	Row bit x Col bit x Banks	SDCR [ADDR_ MUX]	Internal Address						
				27	26	25	24	23 – 12	11 – 10	9 – 1
128 Mbits	8M x 16 bit	12 x 9 x 4	00	—	—	—	—	RA11-0	BA1-0	CA8-0
		12 x 10 x 4	00	—	—	—	CA9			
	16M x 8 bit	13 x 9 x 4	01	—	—	—	RA12			
		12 x 11 x 4	00	—	—	CA11	CA9			
		13 x 10 x 4	01	—	—	CA9	RA12			
		14 x 9 x 4	10	—	—	RA13	RA12			
256 Mbits	16M x 16 bit	12 x 10 x 4	00	—	—	—	CA9	RA11-0	BA1-0	CA8-0
		13 x 9 x 4	01	—	—	—	RA12			
	32M x 8 bit	12 x 11 x 4	00	—	—	CA11	CA9			
		13 x 10 x 4	01	—	—	CA9	RA12			
		14 x 9 x 4	10	—	—	RA13	RA12			
	64M x 4 bit	12 x 12 x 4	00	—	CA12	CA11	CA9			
		13 x 11 x 4	01	—	CA11	CA9	RA12			
		14 x 10 x 4	10	—	CA9	RA13	RA12			
		14 x 10 x 4	10	—	CA9	RA13	RA12			
512 Mbits	32 M x 16 bit	12 x 11 x 4	00	—	—	CA11	CA9	RA11-0	BA1-0	CA8-0
		13 x 10 x 4	01	—	—	CA9	RA12			
		14 x 9 x 4	10	—	—	RA13	RA12			
	64M x 8bit	12 x 12 x 4	00	—	CA12	CA11	CA9			
		13 x 11 x 4	01	—	CA11	CA9	RA12			
		14 x 10 x 4	10	—	CA9	RA13	RA12			
1 Gbits	64M x 16bit	12 x 12 x 4	00	—	CA12	CA11	CA9	RA11-0	BA1-0	CA8-0
		13 x 11 x 4	01	—	CA11	CA9	RA12			
		14 x 10 x 4	10	—	CA9	RA13	RA12			
2 Gbits	128M x16bit	12 x 13 x 4	00	CA13	CA12	CA11	CA9	RA11-0	BA1-0	CA8-0
		13 x 12 x 4	01	CA12	CA11	CA9	RA12			
		14 x 11 x 4	10	CA11	CA9	RA13	RA12			

¹ All SD_A[13:0] bits are generated on every access, but only the bits actually used by the memory are shown.

² All column address (CA) bits in this table are physical column address lines. The SDRAM controller inserts an extra bit CA10 to control the precharge option.

All memory devices of a single chip-select block must have the same configuration and row/column address width; however, this is not necessary between different blocks. If mixing different memory organizations in different blocks, the following guidelines ensure that every block is fully contiguous.

For 32-bit data bus configuration:

- If all devices' row address width is 12 bits, the column address can be ≥ 8 bits.
- If all devices' row address width is 13 bits, the column address can be ≥ 8 bits.
- If all devices' column address width is 8 bits, the row address can be ≥ 11 bits.
- The maximum row bits plus column bits equals 24.
- x8 and x16 data width memory devices can be mixed (but not in the same space).
- x32 data width memory devices cannot be mixed with any other width.

For 16-bit data bus configuration:

- If all devices' row address width is 12 bits, the column address can be ≥ 9 bits.
- If all devices' row address width is 13 bits, the column address can be ≥ 9 bits.
- If all devices' column address width is 9 bits, the row address can be ≥ 11 bits.
- The maximum row bits plus column bits equals 25.
- x16 data width memory devices cannot be mixed with any other width.

18.3.2 SDRAM SDR Connections

Figure 18-2 shows a block diagram using 32-bit wide SDR SDRAM (such as Micron MT48LC4M32B2) and flash (such as Spansion AM29LV160D). SDR design requires special timing consideration for the SD_DQS[3:2] signals. For reads from DDR SDRAMs, the memory drives the DQS pins so that the data lines and DQS signals have concurrent edges. The SDRAMC is designed to latch data 1/4 clock after the SD_DQS[3:2] edge. For DDR SDRAM, this ensures that the latch time is in the middle of the data valid window.

The SDRAMC also uses the SD_DQS[3:2] signals to determine when read data can be latched for SDR SDRAM; however, SDR memories do not provide DQS outputs. Instead the SDRAMC provides a SD_SDRDQS output routed back into the controller as SD_DQS[3:2]. The SD_SDRDQS signal should be routed such that the valid data from the SDRAM reaches the controller at the same time or before the SD_SDRDQS reaches the SD_DQS[3:2] inputs.

When routing SD_SDRDQS the outbound trace length should be matched to the SD_CLK trace length. This aligns SD_SDRDQS to the SD_CLK as if the memory had generated the DQS pulse. The inbound trace should be routed along the data path, which should synchronize the SD_DQS so that the data is latched in the middle of the data valid window.

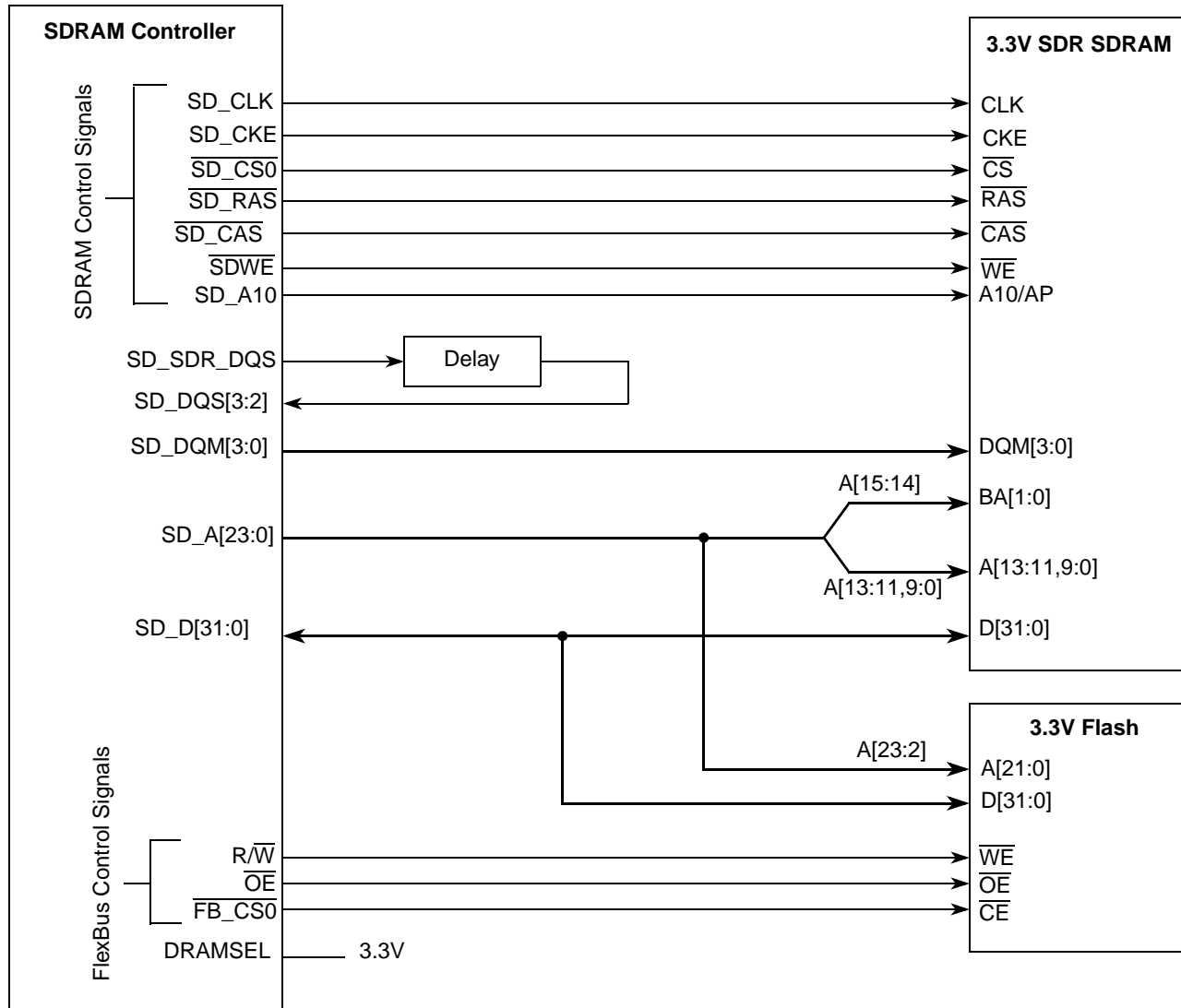


Figure 18-2. Example 3.3V, 32-bit SDR SDRAM System

18.3.3 SDRAM DDR Component Connections

Figure 18-3 shows a block diagram using 16-bit wide DDR SDRAM (such as Micron MT46V8M16) and flash (such as Spansion AM29DBB160G).

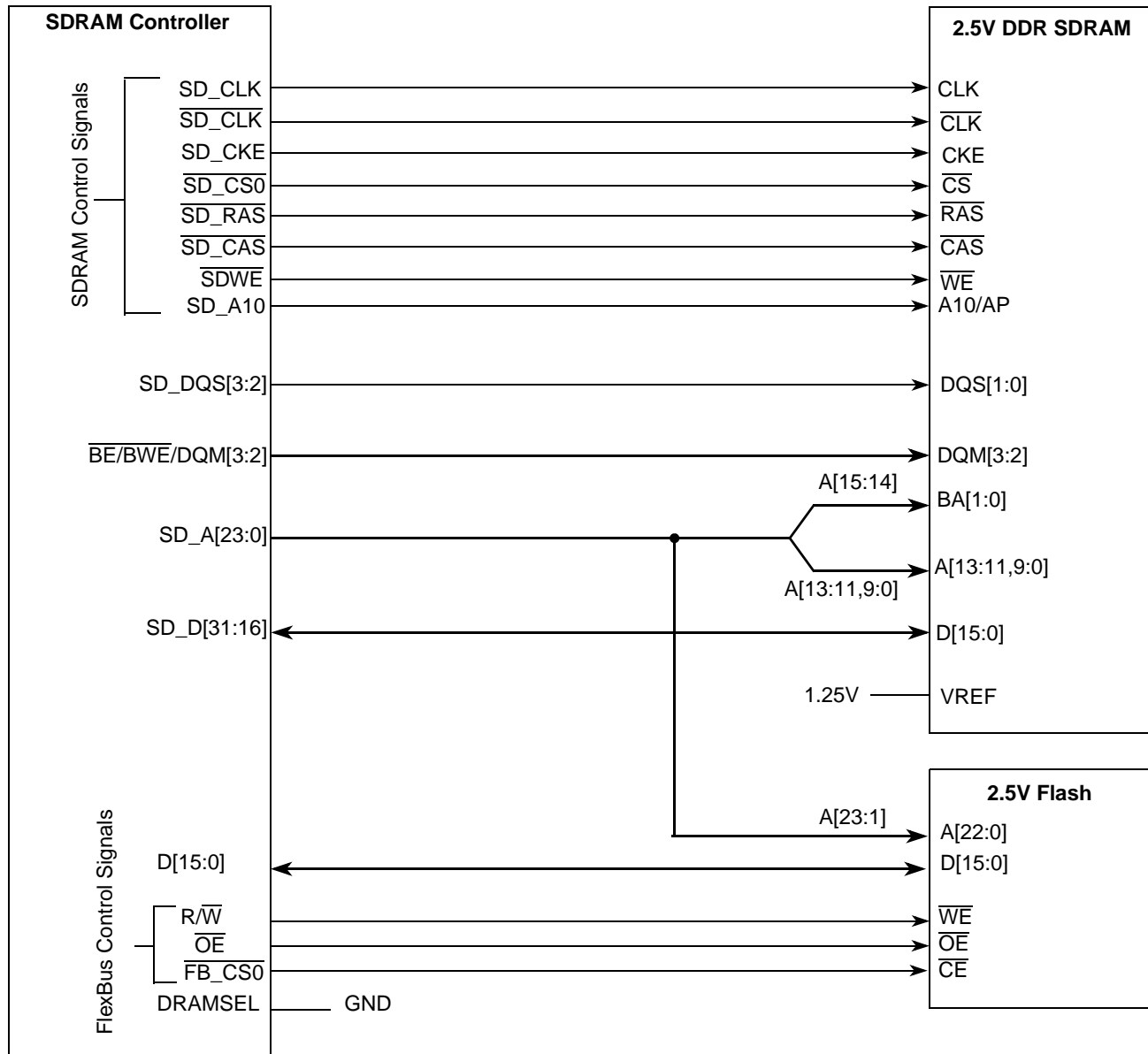


Figure 18-3. Example 2.5V, 16-bit DDR SDRAM System

18.3.4 DDR SDRAM Layout Considerations

Due to the critical timing for DDR SDRAM, a number of considerations should be taken into account during PCB layout:

- Minimize overall trace lengths.

- Each DQS, DM, and DQ group must have identical loading and similar routing to maintain timing integrity.
- The loading and routing of SD_DQS must match those of SD_D.
- Control and clock signals are routed point-to-point.
- Trace length for clock, address, and command signals should match.
- Route DDR signals on layers adjacent to the ground plane.
- Use a VREF plane under the SDRAM.
- VREF is decoupled from SDVDD and VSS.
- To avoid crosstalk, address and command signals must remain separate from data and data strobes.
- Use different resistor packs for command/address and data/data strobes.
- Series termination should be used to help match output driver impedance to trace impedance. (Driver impedance is affected by drive strength.) Typically, a $50\ \Omega$ system with a $22\ \Omega$ series resistor is a good starting point, but this should be analyzed based on actual board design and loading.
- Series termination should be between the processor and memory, but closest to the processor.
- The SD_CLK and $\overline{\text{SD_CLK}}$ signals can be terminated with a single termination resistor between the two clock phases. A $100 - 120\ \Omega$ resistor produces effective termination for the differential SD_CLK. Placement of the terminator should be physically close to the input receiver on the SDRAM(s).

If using a SDRAM DIMM, such as a 144-pin DDR2 SO-DIMM, termination on the CLK lines is not recommended, as clock line termination is already populated on the DIMM module. Additional termination on the motherboard (main board) may cause undersired effects.

- $0.1\ \mu\text{F}$ decoupling for every termination resistor pack.

NOTE

Only series termination is supported on this device, which is different than typical DDR designs.

18.3.4.1 Termination Example

Figure 18-4 shows the recommended termination circuitry for DDR SDRAM signals.

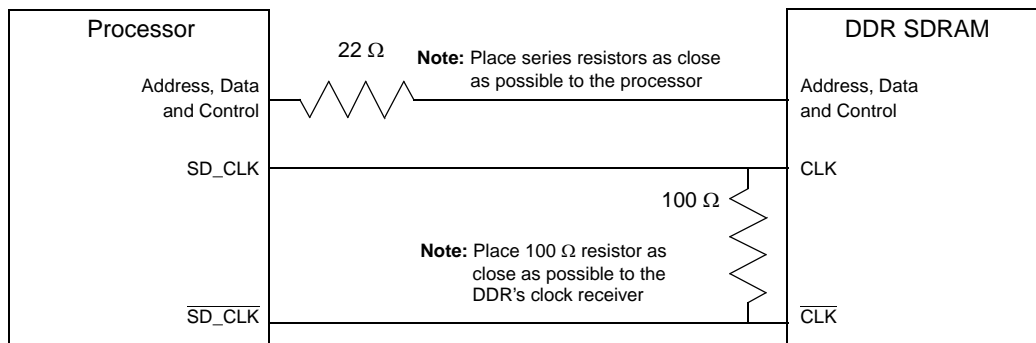


Figure 18-4. DDR SDRAM Termination Circuit

18.4 Memory Map/Register Definition

The SDRAM controller and its associated logic contain two sets of programming registers:

- SDRAM controller's control and configuration registers
- Chip-select configuration control registers

NOTE

The slew rate for the SDRAM pins is controlled by a register in the GPIO module. See [Section 13.3.7, “SDRAM Mode Select Control Register \(MSCR_SDRAM\),”](#) for more details.

[Table 18-6](#) shows the SDRAM controller control and configuration registers. Unspecified memory spaces are reserved for future use. Access to reserved space is prohibited. It is recommended to write 0 to reserved space. Reads from a write-only bit return 0.

Table 18-6. SDRAMC Memory Map

Address	Register	Width (bits)	Access	Reset Value	Section/Page
0xFC0A_8000	SDRAM Mode/Extended Mode Register (SDMR)	32	R/W	0x0000_0000	18.4.1/18-14
0xFC0A_8004	SDRAM Control Register (SDCR)	32	R/W	0x0000_0000	18.4.2/18-15
0xFC0A_8008	SDRAM Configuration Register 1 (SDCFG1)	32	R/W	0x0000_0000	18.4.3/18-17
0xFC0A_800C	SDRAM Configuration Register 2 (SDCFG2)	32	R/W	0x0000_0000	18.4.4/18-19
0xFC0A_8110	SDRAM Chip Select 0 Configuration (SDCS0)	32	R/W	0x0000_0000	18.4.5/18-20
0xFC0A_8114	SDRAM Chip Select 1 Configuration (SDCS1)	32	R/W	0x0000_0000	18.4.5/18-20

18.4.1 SDRAM Mode/Extended Mode Register (SDMR)

The SDMR ([Figure 18-5](#)) writes to the mode and extended mode registers physically residing within the SDRAM chips. These registers must be programmed during SDRAM initialization. See [Section 18.6, “Initialization/Application Information”](#) for more information on the initialization sequence.

Address: 0xFC0A_8000 (SDMR)

Access: SDCR[MODE_EN] = 0 User read-only
SDCR[MODE_EN] = 1 User read/write

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	BK				AD												0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
W																	CMD															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Figure 18-5. SDRAM-Mode/Extended-Mode Register (SDMR)

Table 18-7. SDMR Field Descriptions

Field	Description
31–30 BK	Bank address. Driven onto SD_BA[1:0] along with a LMR/LEMR command. All SDRAM chip selects are asserted simultaneously. SDCR[CKE] must be set before attempting to generate an LMR/LEMR command. The SD_BA[1:0] value is used to select between LMR and LEMR commands. 00 Load mode register command (LMR) 01 Load extended mode register command (LEMR) for non-mobile DDR devices 10 Load extended mode register command (LEMR) for mobile DDR devices 11 Reserved
29–18 AD	Address. Driven onto SD_A[11:0] along with an LMR/LEMR command. The AD value is stored as the mode (or extended mode) register data.
17	Reserved, must be cleared.
16 CMD	Command. This bit is write-only and always returns a 0 when read. 1 Generate an LMR/LEMR command 0 Do not generate any command
15–0	Reserved, must be cleared.

18.4.2 SDRAM Control Register (SDCR)

The SDCR (Figure 18-6) controls SDRAMC operating modes, including refresh count and address line muxing.

Address: 0xFC0A_8004 (SDCR)

Access: User read/write

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
R	MODE_EN	CKE	DDR_MODE	REF_EN	0	0	ADDR_MUX		0	OE_RULE	REF_CNT					
W																
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	0	0	MEM_PS	0	DQS_OE		0	0	0	0	0	0	0	0	0	0
W														IREF	IPALL	
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Figure 18-6. SDRAM Control Register (SDCR)

Table 18-8. SDCR Field Descriptions

Field	Description
31 MODE_EN	SDRAM mode register programming enable. 0 SDMR locked, cannot be written. 1 SDMR enabled, can be written. Note: MODE_EN must be cleared during normal operation,
30 CKE	Clock enable. CKE must be set to perform normal read and write operations. Clear CKE to put the memory in self-refresh or power-down mode. 0 SD_CKE is negated (low) 1 SD_CKE is asserted (high)

Table 18-8. SDCR Field Descriptions (continued)

Field	Description
29 DDR_MODE	DDR mode select. 0 SDR mode 1 DDR mode
28 REF_EN	Refresh enable. 0 Automatic refresh disabled 1 Automatic refresh enabled
27–26	Reserved, must be cleared.
25–24 ADDR_MUX	Controls the use of internal address bits A[27:24] as row or column bits on the SD_A bus. See Table 18-4 , and Table 18-5 .
23	Reserved, must be cleared.
22 OE_RULE	Drive rule selection. 0 Tri-state except to write. SD_D and SD_DQS are only driven when necessary to perform a write command. 1 Drive except to read. SD_D and SD_DQS are only tristated when necessary to perform a read command. When not being driven for a write cycle, SD_D hold the most recent value and SD_DQS are driven low. This mode is intended for minimal applications only, to prevent floating signals and allow unterminated board traces. However, terminated wiring is always recommended over unterminated.
21–16 REF_CNT	The average periodic interval at which the controller generates refresh commands to memory; measured in increments of $64 \times \text{SD_CLK}$ period. $\text{REF_CNT} = (\text{t}_{\text{REFI}} / (\text{t}_{\text{CK}} \times 64)) - 1$, rounded down to the next integer value. If the SDRAM data sheet does not define t_{REFI} , it can be calculated by $\text{t}_{\text{REFI}} = \text{t}_{\text{REF}} / \text{\#rows}$.
15–14	Reserved, must be cleared.
13 MEM_PS	Memory data port size. 0 32-bit data bus 1 16-bit data bus
12	Reserved, must be cleared.
11–10 DQS_OE	DQS output enable. Each DQS_OE bit is a master enable for the corresponding SD_DQS n signal. DQS_OE[1] (SDCR[11]) enables SD_DQS3 and DQS_OE[0] (SDCR[10]) enables SD_DQS2. 0 SD_DQS n can never drive. Use this value in SDR mode or in DDR mode with a single DQS memory. Some 32-bit DDR devices have only a single DQS pin. Enable one of the SD_DQS n signals and disable the other. Then, short both pins external to the device. 1 SD_DQS n can drive as necessary, depending on commands and SDCR[OE_RULE] setting. DDR only.
9–3	Reserved, must be cleared.
2 IREF	Initiate refresh command. Used to force a software-initiated refresh command. This bit is write-only, reads return zero. 0 Do not generate a refresh command. 1 Generate a refresh command. All $\overline{\text{SD_CS}}_n$ signals are asserted simultaneously. SDCR[CKE] must be set before attempting to generate a software refresh command. Note: A software requested refresh is completely independent of the periodic refresh interval counter. Software refresh is only possible when MODE_EN is set.

Table 18-8. SDCR Field Descriptions (continued)

Field	Description
1 IPALL	<p>Initiate precharge all command. Used to force a software-initiated precharge all command. This bit is write-only, reads return zero.</p> <p>0 Do not generate a precharge command.</p> <p>1 Generate a precharge all command. All $\overline{SD_CSn}$ signals are asserted simultaneously. SDCR[CKE] must be set before generating a software precharge command.</p> <p>Note: Software precharge is only possible when MODE_EN is set.</p> <p>Note: Do not set IREF and IPALL at the same time.</p>
0	Reserved, should be cleared.

18.4.3 SDRAM Configuration Register 1 (SDCFG1)

The 32-bit read/write SDRAM configuration register 1 (SDCFG1) stores necessary delay values between specific SDRAM commands. During initialization, software loads values to the register according to the selected SD_CLK frequency and SDRAM information obtained from the data sheet. This register resets only by a power-up reset signal.

The read and write latency fields govern the relative timing of commands and data and must be exact values. All other fields govern the relative timing from one command to another; they have minimum values, but any larger value is also legal (but with decreased performance).

The minimum values of certain fields can be different for SDR, DDR SDRAM, even if the data sheet timing is the same, because:

- In SDR mode, the memory controller counts the delay in SD_CLK
- In DDR mode, the memory controller counts the delay in 2 x SD_CLK (also referred to as SD_CLK2)
- SD_CLK—memory controller clock—is the speed of the SDRAM interface and is equal to the internal bus clock.
- SD_CLK2—double frequency of SD_CLK—DDR uses both edges of the bus-frequency clock (SD_CLK) to read/write data

NOTE

In all calculations for setting the fields of this register, convert time units to clock units and round up to the nearest integer.

Address: 0xFC0A_8008 (SDCFG1)

Access: User read/write

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
R	SRD2RWP				0	SWT2RWP				RD_LAT				0	ACT2RW	
W																
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	0	PRE2ACT			REF2ACT				0	WT_LAT			0	0	0	0
W																
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Figure 18-7. SDRAM Configuration Register 1 (SDCFG1)

Table 18-9. SDCFG1 Field Descriptions

Field	Description
31–28 SRD2RWP	Single read to read/write/precharge delay. Limiting case is read to write. SDR: $SRD2RWP = CL + t_{HZ} + 2$ DDR: $SRD2RWP = CL + 1$ t_{HZ} is the time the data bus uses to return to hi-impedance after a read and is found in the SDRAM device specifications. Note: Count value is in SD_CLK periods for SDR and DDR mode.
27	Reserved, must be cleared.
26–24 SWT2RWP	Single write to read/write/precharge delay. Limiting case is write to precharge. SDR: $SWT2RWP = t_{WR}$ DDR: $SWT2RWP = t_{WR} + 1$ Note: Count value is in SD_CLK periods for SDR and DDR mode.
23–20 RD_LAT	Read CAS Latency. Read command to read data available delay counter. For DDR: If CL = 2, write 0x6 If CL = 2.5, write 0x7 For SDR: If CL = 2, write 0x2 If CL = 3, write 0x3 Note: The recommended values are just a starting point and may need to be adjusted depending on the trace length for the data and DQS lines. CL = 2.5 is not supported for SDR. SDR: Count value is in SD_CLK periods. DDR: Count value is in SD_CLK2 periods.
19	Reserved, must be cleared.
18–16 ACT2RW	Active to read/write delay. Active command to any following read- or write-delay counter. Suggested value = $(t_{RCD} \times f_{SD_CLK}) - 1$ (Round up to nearest integer) Example: If $t_{RCD} = 20ns$ and $f_{SD_CLK} = 99\text{ MHz}$ Suggested value = $(20ns \times 99\text{ MHz}) - 1 = 0.98$; round to 1. Note: Count value is in SD_CLK periods for SDR and DDR modes.

Table 18-9. SDCFG1 Field Descriptions (continued)

Field	Description
15	Reserved, must be cleared.
14–12 PRE2ACT	<p>Precharge to active delay. Precharge command to following active command delay counter.</p> <p>Suggested value = $(t_{RP} \times f_{SD_CLK}) - 1$ (Round up to nearest integer) Example: If $t_{RP} = 20\text{ns}$ and $f_{SD_CLK} = 99\text{ MHz}$ Suggested value = $(20\text{ns} \times 99\text{ MHz}) - 1 = 0.98$; round to 1.</p> <p>Note: Count value is in SD_CLK periods for SDR and DDR modes.</p>
11–8 REF2ACT	<p>Refresh to active delay. Refresh command to following active or refresh command delay counter.</p> <p>SDR/DDR: $\text{REF2ACT} = (t_{RFC} \times f_{SD_CLK}) - 1$ (Round up to nearest integer) Example (for SDR/DDR): If $t_{RFC} = 75\text{ns}$ and $f_{SD_CLK} = 99\text{ MHz}$ Suggested value = $(75\text{ns} \times 99\text{ MHz}) - 1 = 6.425$; round to 7.</p> <p>Note: Count value is in SD_CLK periods for SDR and DDR modes.</p>
7	Reserved, must be cleared.
6–4 WT_LAT	<p>Write latency. Write command to write data delay counter.</p> <p>SDR: write 0x0 DDR: write 0x3</p> <p>Note: SDR mode: Count value is in SD_CLK periods. DDR mode: Count value is in SD_CLK2 periods.</p>
3–0	Reserved, must be cleared.

18.4.4 SDRAM Configuration Register 2 (SDCFG2)

The 32-bit read/write configuration register 2 stores delay values necessary between specific SDRAM commands. During initialization, software loads values to the register according to the SDRAM information obtained from the data sheet. This register is reset only by a power-up reset signal.

The burst length (BL) field must be exact. All other fields govern the relative timing from one command to another, they have minimum values but any larger value is also legal (but with decreased performance).

All delays in this register are expressed in SD_CLK. In all calculations for setting the fields of this register, convert time units to clock units and round up to the nearest integer.

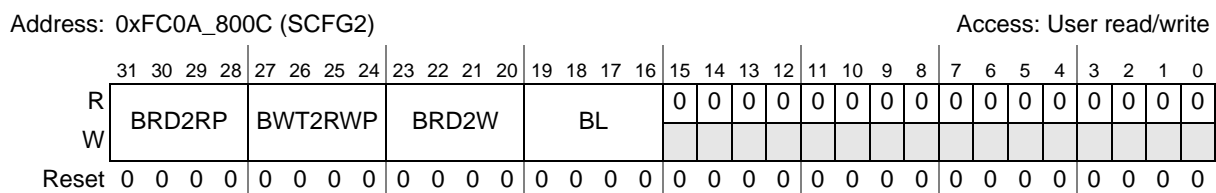


Figure 18-8. SDRAM Configuration Register 2 (SDCFG2)

Table 18-10. SDCFG2 Field Descriptions

Field	Description
31–28 BRD2RP	Burst read to read/precharge delay. Limiting case is read to read. SDR: $BRD2RP = BurstLength + 1$ DDR: $BRD2RP = BurstLength/2 + 1$
27–24 BWT2RWP	Burst write to read/write/precharge delay. Limiting case is write to precharge. SDR: $BWT2RWP = BurstLength + t_{WR} - 2$ DDR: $BWT2RWP = BurstLength/2 + t_{WR}$
23–20 BRD2W	Burst read to write delay. SDR: $BRD2W = CL + BurstLength + t_{HZ}$ DDR: $BRD2W = CL + BurstLength/2 - 1$
19–16 BL	Burst length. $BL = BurstLength - 1$ Note: Burst length depends on port size: 32-bit bus (SDCR[MEM_PS] = 0), burst length is 4. Write BL = 3.. If 16-bit bus (SDCR[MEM_PS] = 1), burst length is 8. Write BL = 7.
15–0	Reserved, must be cleared.

18.4.5 SDRAM Chip Select Configuration Registers (SDCS_n)

These registers define base address and space size of each chip select.

NOTE

Because the SDRAM module is one of the slaves connected to the crossbar switch, it is only accessible within a certain memory range. The only applicable address ranges for which the chip-selects can be active are 0x4000_0000 – 0x7FFF_FFFF. Be sure to set the SDCS_n registers appropriately.

NOTE

The user should not probe memory on a DDR chip select to determine if memory is connected. If a read is attempted from a DDR SDRAM chip select when there is no memory to respond with the appropriate DQS pulses, the bus cycle hangs. Because no high level bus monitor exists on the device, a reset is the only way to exit the error condition.

Address: 0xFC0A_8110 (SDCS0)
0xFC0A_8114 (SDCS1)

Access: User read/write

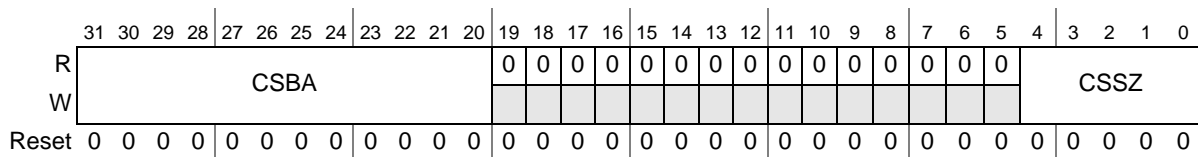
Figure 18-9. SRAM Chip Select Configuration Register (SDCS_n)

Table 18-11. SDCSn Field Descriptions

Field	Description																																																						
31–20 CSBA	Chip-select base address. Because the SDRAM module is one of the slaves connected to the crossbar switch, it is only accessible within a certain memory range. The only applicable address ranges for which the chip-selects can be active are 0x4000_0000 – 0x7FFF_FFFF. Therefore, the possible range for this field is 0x400 – 0x7FF.																																																						
19–5	Reserved, must be cleared.																																																						
4–0 CSSZ	Chip select size. <table><tr><th>CSSZ</th><th>Size</th><th>Address Lines to Compare</th><th>CSSZ</th><th>Size</th><th>Address Lines to Compare</th></tr><tr><td>00000</td><td>Disabled</td><td>—</td><td>11000</td><td>32 MByte</td><td>A[31:25]</td></tr><tr><td>00001–10001</td><td>Reserved</td><td>Reserved</td><td>11001</td><td>64 MByte</td><td>A[31:26]</td></tr><tr><td>10010</td><td>Reserved</td><td>Reserved</td><td>11010</td><td>128 MByte</td><td>A[31:27]</td></tr><tr><td>10011</td><td>1 MByte</td><td>A[31:20]</td><td>11011</td><td>256 MByte</td><td>A[31:28]</td></tr><tr><td>10100</td><td>2 MByte</td><td>A[31:21]</td><td>11100</td><td>512 MByte</td><td>A[31:29]</td></tr><tr><td>10101</td><td>4 MByte</td><td>A[31:22]</td><td>11101</td><td>1 GByte</td><td>A[31:30]</td></tr><tr><td>10110</td><td>8 MByte</td><td>A[31:23]</td><td>11110</td><td>2 GByte</td><td>A31</td></tr><tr><td>10111</td><td>16 MByte</td><td>A[31:24]</td><td>11111</td><td>4 GByte</td><td>Ignore A[31:20]</td></tr></table>	CSSZ	Size	Address Lines to Compare	CSSZ	Size	Address Lines to Compare	00000	Disabled	—	11000	32 MByte	A[31:25]	00001–10001	Reserved	Reserved	11001	64 MByte	A[31:26]	10010	Reserved	Reserved	11010	128 MByte	A[31:27]	10011	1 MByte	A[31:20]	11011	256 MByte	A[31:28]	10100	2 MByte	A[31:21]	11100	512 MByte	A[31:29]	10101	4 MByte	A[31:22]	11101	1 GByte	A[31:30]	10110	8 MByte	A[31:23]	11110	2 GByte	A31	10111	16 MByte	A[31:24]	11111	4 GByte	Ignore A[31:20]
CSSZ	Size	Address Lines to Compare	CSSZ	Size	Address Lines to Compare																																																		
00000	Disabled	—	11000	32 MByte	A[31:25]																																																		
00001–10001	Reserved	Reserved	11001	64 MByte	A[31:26]																																																		
10010	Reserved	Reserved	11010	128 MByte	A[31:27]																																																		
10011	1 MByte	A[31:20]	11011	256 MByte	A[31:28]																																																		
10100	2 MByte	A[31:21]	11100	512 MByte	A[31:29]																																																		
10101	4 MByte	A[31:22]	11101	1 GByte	A[31:30]																																																		
10110	8 MByte	A[31:23]	11110	2 GByte	A31																																																		
10111	16 MByte	A[31:24]	11111	4 GByte	Ignore A[31:20]																																																		

Any chip-select can be enabled or disabled, independent of others. Any chip-select can be allocated any size of address space from 1M to 4G, independent of others. Any chip-select address space can begin at any size-aligned base address, independent of others.

For contiguous memory with different sizes of memory blocks, place largest block at the lowest address and place smaller blocks in descending size order at ascending base addresses.

For example, assume a system with 2 chip selects: CS0=16M, CS1=256M:

CS0CFG = 0x4F000017 = enable 16M @ 0x4F000000-0x4FFFFFFF

CS1CFG = 0x5000001B = enable 256M @ 0x50000000-0x5FFFFFFF

This gives 272 MB total memory, at 0x4F000000-0x5FFFFFFF.

18.5 Functional Description

18.5.1 SDRAM Commands

When an internal bus master accesses SDRAM address space, the memory controller generates the corresponding SDRAM command. [Table 18-12](#) lists SDRAM commands supported by the memory controller.

Table 18-12. SDRAM Commands

Function	Symbol	CKE	$\overline{\text{CS}}$	$\overline{\text{RAS}}$	$\overline{\text{CAS}}$	$\overline{\text{WE}}$	BA[1:0]	A[10]	Other A
Command Inhibit	INH	H	H	X	X	X	X	X	X
No Operation	NOP	H	L	H	H	H	X	X	X
Row and Bank Active	ACTV	H	L	L	H	H	V	V	V
Read	READ	H	L	H	L	H	V	L	V
Write	WRITE	H	L	H	L	L	V	L	V
Burst Terminate (SDR/DDR only)	BST	H	L	H	H	L	X	X	X
Precharge All Banks	PALL	H	L	L	H	L	X	H	X
Precharge Selected Bank	PRE	H	L	L	H	L	V	L	X
Load Mode Register	LMR	H	L	L	L	L	LL	V	V
Load Extended Mode Register	LEMR	H	L	L	L	L	LH	V	V
Auto Refresh	REF	H	L	L	L	H	X	X	X
Self Refresh	SREF	H→L	L	L	L	H	X	X	X
Power Down	PDWN	H→L	H	X	X	X	X	X	X
H = High L = Low V = Valid X = Don't care									

Many commands require a delay before the next command may be issued; sometimes the delay depends on the type of the next command. These delay requirements are managed by the values programmed in the memory controller configuration registers (SDCFG1, SDCFG2).

18.5.1.1 Row and Bank Active Command (ACTV)

The ACTV command is responsible for latching the row and bank address and activating the specified row bank of a memory block. After the row is activated, it can be accessed using subsequent read and write commands.

NOTE

The SDRAMC supports one active row for each chip select block. See [Section 18.6.1, “Page Management,”](#) for more information.

18.5.1.2 Read Command (READ)

When the SDRAMC receives a read request via the internal bus, it first checks the row and bank of the new access. If the address falls within the active row of an active bank, it is a page hit, and the read is issued as soon as possible (pending any delays required by previous commands). If the address is within an inactive bank, the memory controller issues an ACTV followed by the read command. If the address is not within the active row of an active bank, the memory controller issues a pre command to close the active

row. Then, the SDRAMC issues ACTV to activate the necessary row and bank for the new access, followed by the read to the SDRAM.

The PALL/PRE and ACTV commands (if necessary) can sometimes be issued in parallel with an on-going data movement.

To truncate a burst read when only a single read is needed, the memory controller issues the burst-terminate command. With SDR memory, the data masks are negated throughout the entire read size. With DDR memory, the data masks are asserted high throughout the entire read size; but DDR memory ignores the data masks during reads.

18.5.1.3 Write Command (WRITE)

When the memory controller receives a write request via the internal bus, it first checks the row and bank of the new access. If the address falls within the active row of an active bank, it is a page hit, and the WRITE is issued as soon as possible (pending any delays required by previous commands). If the address is within the inactive bank, the memory controller issues an ACTV followed by the write command. If the address is not within the active row of an active bank, the memory controller issues a PRE command to close the active row. Then, the SDRAMC issues ACTV to activate the necessary row and bank for the new access, followed by the WRITE command to the SDRAM.

The PALL/PRE and ACTV commands (if necessary) can sometimes be issued in parallel with an on-going data movement.

In SDR mode, the memory controller issues the burst terminate command to truncate burst write for a single write. This is not the case for DDR system. With SDR and DDR memory, a read command can be issued overlapping the masked beats at the end of a previous single write of the case \overline{CS} ; the read command aborts the remaining (unnecessary) write beats.

18.5.1.4 Burst-Terminate Command (BST)

SDRAMs are burst-only devices, but provide mechanisms to truncate a burst if all of the beats are not needed. The burst-terminate command truncates read bursts (SDR and DDR) and write bursts (SDR). To truncate a burst write for DDR, the read command can abort the remaining unnecessary write beats. This method also works when in SDR mode. The most recently registered read or write command prior to the burst terminate command is truncated. The active page remains open.

18.5.1.5 Precharge-All-Banks (PALL) and Selected-Bank (PRE) Commands

The precharge command puts SDRAM into an idle state. The SDRAM must be in this idle state before a REF, LMR, LEMR, or ACTV command to open a new row within a particular bank can be issued.

The memory controller issues the precharge command only when necessary for one of these conditions:

- Access to a new row
- Refresh interval elapsed
- Software commanded precharge during device initialization

NOTE

A precharge is required after DRAMs also have a maximum bank-open period. The memory controller does not time the bank-open period because the refresh interval is always less.

18.5.1.6 Load Mode/Extended Mode Register Command (LMR, LEMR)

All SDRAM devices contain mode registers that configure the timing and burst mode for the SDRAM. These commands access the mode registers that physically reside within the SDRAM devices. During the LMR or LEMR command, SDRAM latches the address and bank buses to load the values into the selected mode register.

NOTE

The LMR and LEMR commands are only used during SDRAM initialization.

Use the following steps to write the mode register and extended mode register:

1. Set the SDCR[MODE_EN] bit.
2. Write the SDMR[BA] bits to select the mode register.
3. Write the desired mode register value to the SDMR[ADDR]. Do not overwrite the SDMR[BA] values. This step can be performed in the same register write in step 2.
4. Set the SDMR[CMD] bit.
5. For DDR, step 2 to 4 should be performed twice. The first is for the extended-mode register, and the last is for the mode register.
6. Clear the SDCR[MODE_EN] bit.

18.5.1.6.1 Mode Register Definition

Figure 18-10 shows the mode register definition. This is the SDRAM's mode register, not the SDRAMC's mode/extended mode register (SDMR) defined in [Section 18.4.1, “SDRAM Mode/Extended Mode Register \(SDMR\).”](#) Refer to device data sheet for detailed description.

	BA1	BA0	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0
Field	0	0	OP_MODE				CL			BT	BLEN			

Figure 18-10. Mode Register

Table 18-13. Mode Register Field Descriptions

Field	Description
BA1–BA0	Bank address. These must be zero to select the mode register.
A11–A7 OP_MODE	Operating mode. xx000 Standard Operation (SDR only) 00000 Normal Operation (DDR) 00010 Reset DLL (DDR) Else Reserved
A6–A4 CL	CAS latency. Delay in clocks from issuing a READ to valid data out. Check the SDRAM manufacturer's spec because the CL settings supported can vary from memory to memory.

Table 18-13. Mode Register Field Descriptions (continued)

Field	Description
A3 BT	Burst type. 0 Sequential 1 Interleaved. This setting should not be used because the SDRAMC does not support interleaved bursts.
A2–A0 BLN	Burst length. Determines the number of column locations that are accessed for a given READ or WRITE command. 000 One. This setting is not valid for DDR. 001 Two 010 Four 011 Eight Else Reserved

18.5.1.6.2 Extended Mode Register Definition

Figure 18-11 shows the extended-mode register used by DDR SDRAMs. This is the SDRAM's extended mode register, not the SDRAMC's mode/extended-mode register (SDMR) defined in [Section 18.4.1](#), “SDRAM Mode/Extended Mode Register (SDMR).” Refer to device data sheet for detailed description.

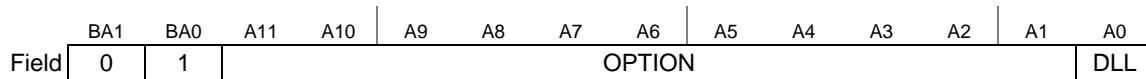


Figure 18-11. Extended Mode Register

Table 18-14. Extended-Mode Register Field Descriptions

Field	Description
BA1–BA0	Bank address. These must be set to 01 to select the extended mode register.
A11–A1 OPTION	Option. These bits are not defined by the DDR specification. Each DDR SDRAM manufacturer can use these bits to implement optional features. Check with the SDRAM manufacturer to determine if any optional features have been implemented. For normal operation all bits must be cleared.
A0 DLL	Delay locked loop. Controls enabling of the delay locked loop circuitry used for DDR timing. 0 Enabled 1 Disabled

18.5.1.7 Auto-Refresh Command (REF)

The memory controller issues auto-refresh commands according to the SDCR[REF_CNT] value. Each time the programmed refresh interval elapses, the memory controller issues a PALL command followed by a REF command.

If a memory access is in progress at the time the refresh interval elapses, the memory controller schedules the refresh after the transfer finishes; the interval timer continues counting so the average refresh rate is constant.

After REF command, the SDRAM is in an idle state and waits for an ACTV command.

18.5.1.8 Self-Refresh (SREF) and Power Down (PDWN) Commands

The memory controller issues a PDWN or a SREF command if the SDCR[CKE] bit is cleared. If the SDCR[REF_EN] bit is set when CKE is negated, the controller issues a SREF command; if the REF_EN bit is cleared, the controller issues a PDWN command. The REF_EN bit may be changed in the same register write that changes the CKE bit; the controller acts upon the new value of the REF_EN bit.

Like an auto-refresh command, the controller automatically issues a PALL command before the self-refresh command.

The memory reactivates from power-down or self-refresh mode by setting the CKE bit.

If a normal refresh interval elapses while the memory is in self-refresh mode, a PALL and REF performs when the memory reactivates. If the memory is put into and brought out of self-refresh all within a single-refresh interval, the next automatic refresh occurs on schedule.

In self-refresh mode, memory does not require an external clock. The SD_CLK can be stopped for maximum power savings. If the memory controller clock is stopped, the refresh-interval timer must be reset before the memory is reactivated (if periodic refresh is to be resumed). The refresh-interval timer resets by clearing the REF_EN bit. This can be done at any time while the memory is in self-refresh mode, before or after the memory controller clock is stopped/restarted, but *not* with the same control register write that clears CKE; this would put the memory in power down mode. To restart periodic refresh when the memory reactivates, the REF_EN bit must be reasserted; this can be done before the memory reactivates or in the same control register write that sets CKE to exit self-refresh mode.

18.5.2 Read Clock Recovery (RCR) Block

The RCR block allows the external DDR memory devices to generate clock pulses (strokes) that define the data valid window for each DDR data cycle. The RCR delay block compensates for each byte lane and generates an internal read strobe targeted to the center of the data valid window provided by the external DDR memories.

Figure 18-12 displays a simple timing diagram that illustrates the end result of the RCR delay.

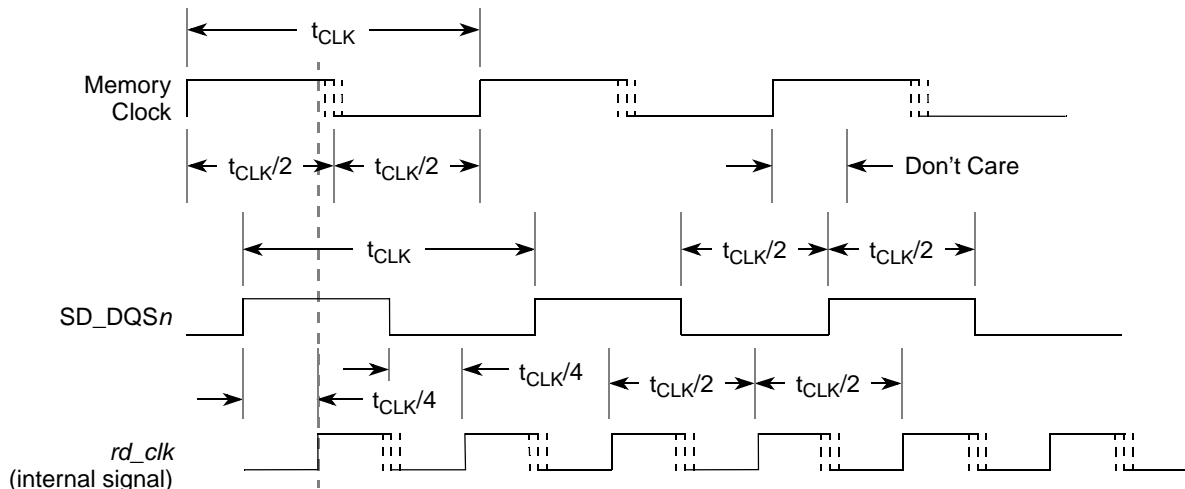


Figure 18-12. Frequency Doubler Block Diagram

Dual data rate (DDR) memories provide data strobe (DQS) timing reference signals in parallel with read data. However, these strobe signals cannot directly clock the data because the strobe edges are aligned with the edges of the data valid window, not the center. The RCR delay module is responsible for delaying the received DQS edges to achieve data-center alignment instead of data-edge alignment. There are two data valid windows per memory clock period with DDR, so the nominal delay of read clocks from DQS is 1/4 memory clock period.

Single data rate (SDR) memories do not use or provide DQS signals. In SDR mode, the SDRAM controller provides an SDRDQS signal that can be driven off-chip and routed back into the DQS inputs. The center of the data valid window is guaranteed relative to the memory clock at the memory devices.

The round-trip SDRDQS-to-DQS delay must match the memory clock output + read data input + round-trip time-of-flight delay so that the received DQS edges have a known phase relationship to the received data. The SDRDQS signal is generated with a 1/4 memory clock period lead time, to compensate for the 1/4 memory clock period delay of DQS through the RCR delay module.

The RCR delay module maintains the 1/4 memory clock period delay of the DQS signals across the full range of silicon process, voltage, and temperature conditions.

The RD_CLK is an internal reconstructed clock derived from DQS. It is twice the frequency of DQS, with the rising edge shifted 1/4 memory clock period after the DQS edge to align with the nominal center of the data valid window.

18.6 Initialization/Application Information

SDRAMs have a prescribed initialization sequence. The following section details the memory initialization steps for DDR SDRAM. The sequence might change slightly from device-to-device. Refer to the device datasheet as the most relevant reference.

1. After reset is deactivated, pause for the amount of time indicated in SDRAM specification. Usually 100µs or 200µs.
2. Configure pin multiplex control for shared $\overline{\text{SD_CS}}$ pins in GPIO module.
3. Configure the slew rate for the SDRAM external pins in the pin multiplexing and control module's MSCR_SDRAM register.
4. Write the base address and mask registers (SDBAR0, SDBAR1, SDMR0, and SDMR1) to setup the address space for each chip-select.
5. Program SDRAM configuration registers (SDCFG1 and SDCFG2) with correct delay and timing values.
6. Issue a PALL command. Initialize the SDRAM control register (SDCR) with SDCR[IPALL] set. The SDCR[REF and IREF] bits should remain cleared for this step.
7. Initialize the SDRAM's extended mode register to enable the DLL. See [Section 18.5.1.6, "Load Mode/Extended Mode Register Command \(LMR, LEMR\),"](#) for instructions on issuing a LEMR command.

8. Initialize the SDRAM's mode register and reset the DLL using the LMR command. See [Section 18.5.1.6, "Load Mode/Extended Mode Register Command \(LMR, LEMR\),"](#) for more instruction on issuing a LMR command. During this step the OP_MODE field of the mode register should be set to normal operation/reset DLL.
9. Pause for the DLL lock time specified by the memory.
10. Issue a second PALL command. Initialize the SDRAM control register (SDCR) with SDCR[IPALL] set. The SDCR[REF and IREF] bits should remain cleared for this step.
11. Refresh the SDRAM. The SDRAM specification should indicate many refresh cycles performed before issuing an LMR command. Write to the SDCR with the IREF bit set (SDCR[REF and IPALL] must be cleared). This forces a refresh of the SDRAM each time the IREF bit is set. Repeat this step until the specified number of refresh cycles have been completed.
12. Initialize the SDRAM's mode register using the LMR command. See [Section 18.5.1.6, "Load Mode/Extended Mode Register Command \(LMR, LEMR\),"](#) for more instruction on issuing an LMR command. During this step the OP_MODE field of the mode register should be set to normal operation.
13. Set SDCR[REF] to enable automatic refreshing, and clear SDCR[MODE_EN] to lock the SDRAM. SDCR[IREF and IPALL] remain cleared.

18.6.1 Page Management

SDRAM devices have four internal banks. A particular row and bank of memory must be activated to allow read and write accesses. The SDRAM controller supports paging mode to maximize the memory access throughout. During operation, the SDRAM controller maintains an open page for each $\overline{SD_CS}$ block. An open page is composed of the active rows in the internal banks. Each internal bank has its own active row.

The physical page size of a $\overline{SD_CS}$ block is equal to the space size divided by the number of rows; but the page may not be contiguous in the internal address space because SDRAMs can have a different row address open in each bank and the internal address bits (A[27:24] and A[9:2]) or (A[27:24] and A[9:1]) used for memory column addresses are not consecutive.

Because the column address may split across two portions of the internal address, the contiguous page size is (number of contiguous columns per bank) \times (number of bits). This gives a contiguous page size of 1 KBytes. However, the total (possibly fragmented) page size is (number of banks) \times (number of columns) \times (number of bits).

If a new access does not fall in the open row of an open bank of a $\overline{SD_CS}$ block, the open row must be closed (PRE) and the new row must be opened (ACTV), then the READ or WRITE command can proceed. An ACTV command activates only one bank at one time. If another read or write falls in an inactive bank, another ACTV is needed, but no precharge is needed. If a read or write falls in any open row of any active banks of a page, no PRE or ACTV is needed; the read or write command can be issued immediately.

A page is kept open until one of the following conditions occurs:

- An access outside the open page.
- A refresh cycle is started.

All $\overline{\text{SD_CS}}$ blocks are refreshed at the same time. The refresh closes all banks of every SDRAM block.

18.6.2 Transfer Size

In the SDRAMC, the internal data bus is 32 bits wide, while the SDRAM external interface bus is 32 or 16 bits wide. Therefore, each internal data beat requires one or two memory data beats. The SDRAM controller manages the size translation (packing/unpacking) between internal and external DRAM buses.

The burst size is the processor standard 16 bytes: Four beats of 4 bytes on the internal bus, four beats of 4 bytes (32-bit mode), or eight beats of 2 bytes (16-bit mode) on the memory bus. The SDRAM controller follows the critical beat first, sequential transfer format required.

The burst size and transfer order must be programmed in the SDRAM mode registers during initialization; the burst size also must be programmed in the memory controller (SDCFG2 register).

Chapter 19

Fast Ethernet Controller (FEC)

19.1 Introduction

This chapter provides a feature-set overview, a functional block diagram, and transceiver connection information for the 10 and 100 Mbps MII (media independent interface), as well as the 7-wire serial interface. Additionally, detailed descriptions of operation and the programming model are included.

19.1.1 Overview

The Ethernet media access controller (MAC) supports 10 and 100 Mbps Ethernet/IEEE 802.3 networks. An external transceiver interface and transceiver function are required to complete the interface to the media. The FEC supports three different standard MAC-PHY (physical) interfaces for connection to an external Ethernet transceiver. The FEC supports the 10/100 Mbps MII and the 10 Mbps-only 7-wire interface.

NOTE

The module must be configured to enable the peripheral function of the appropriate pins (refer to [Chapter 13, “General Purpose I/O Module”](#)) prior to configuring the FEC.

19.1.2 Block Diagram

[Figure 19-1](#) shows the block diagram of the FEC. The FEC is implemented with a combination of hardware and microcode. The off-chip (Ethernet) interfaces are compliant with industry and IEEE 802.3 standards.

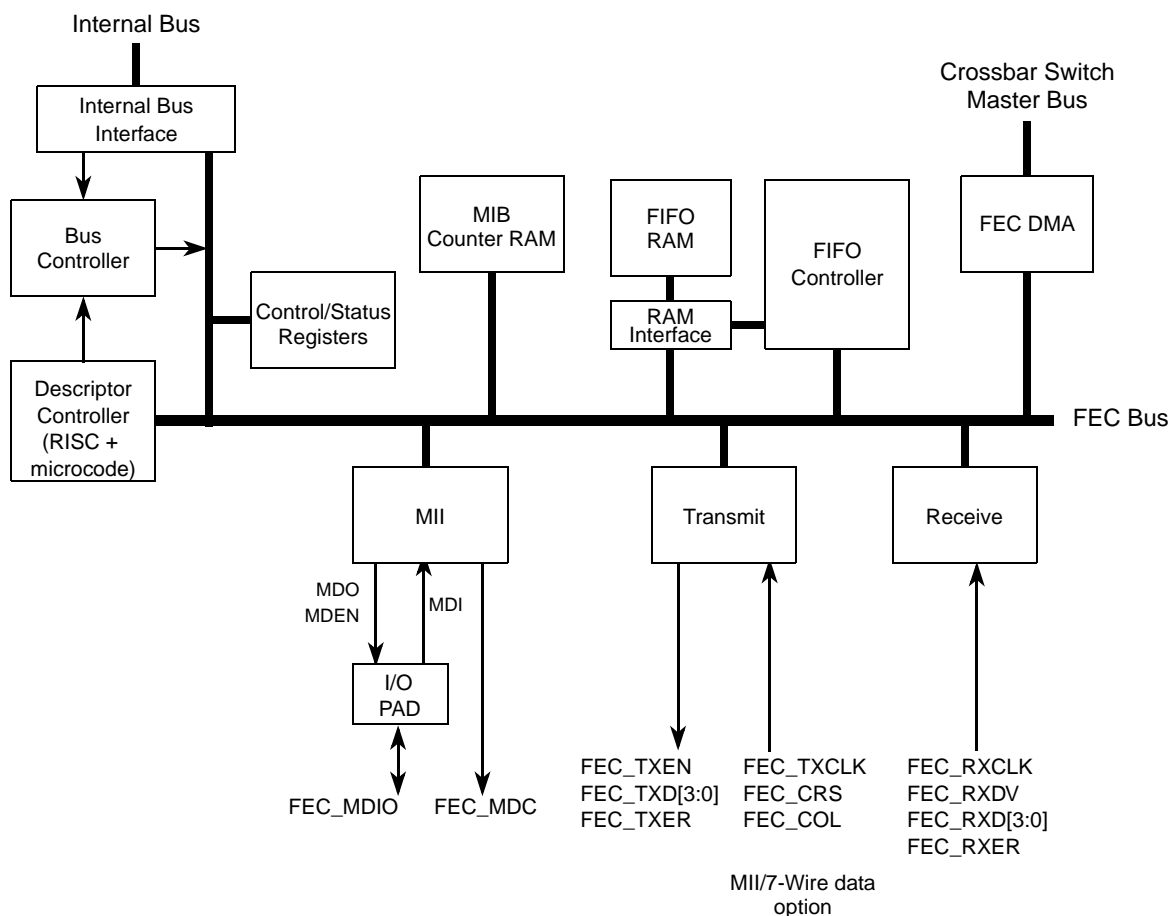


Figure 19-1. FEC Block Diagram

The descriptor controller is a RISC-based controller providing these functions in the FEC:

- Initialization (those internal registers not initialized by you or hardware)
- High level control of the DMA channels (initiating DMA transfers)
- Interpreting buffer descriptors
- Address recognition for receive frames
- Random number generation for transmit collision backoff timer

NOTE

DMA references in this section refer to the FEC's DMA engine. This DMA engine transfers FEC data only and is not related to the eDMA controller described in [Chapter 16, “Enhanced Direct Memory Access \(eDMA\),”](#) nor to the DMA timers described in [Chapter 22, “DMA Timers \(DTIM0–DTIM3\).”](#)

The RAM is the focal point of all data flow in the Fast Ethernet controller and divides into transmit and receive FIFOs. The FIFO boundaries are programmable using the FRSR register. User data flows to/from the DMA block from/to the receive/transmit FIFOs. Transmit data flows from the transmit FIFO into the transmit block, and receive data flows from the receive block into the receive FIFO.

You control the FEC by writing into control registers located in each block. The CSR (control and status registers) block provides global control (Ethernet reset and enable) and interrupt managing registers.

The MII block provides a serial channel for control/status communication with the external physical layer device (transceiver). This serial channel consists of the FEC_MDC (management data clock) and FEC_MDIO (management data input/output) lines of the MII interface.

The FEC DMA block (not to be confused with the device's eDMA controller) provides multiple channels allowing transmit data, transmit descriptor, receive data and receive descriptor accesses to run independently.

The transmit and receive blocks provide the Ethernet MAC functionality (with some assist from microcode).

The message information block (MIB) maintains counters for a variety of network events and statistics. It is not necessary for operation of the FEC, but provides valuable counters for network management. The counters supported are the RMON (RFC 1757) Ethernet Statistics group and some of the IEEE 802.3 counters. See [Section 19.4.1, “MIB Block Counters Memory Map,”](#) for more information.

19.1.3 Features

The FEC incorporates the following features:

- Support for three different Ethernet physical interfaces:
 - 100-Mbps IEEE 802.3 MII
 - 10-Mbps IEEE 802.3 MII
 - 10-Mbps 7-wire interface (industry standard)
- IEEE 802.3 full duplex flow control
- Programmable max frame length supports IEEE 802.1 VLAN tags and priority
- Support for full-duplex operation (200 Mbps throughput) with a minimum internal bus clock rate of 50 MHz
- Support for half-duplex operation (100 Mbps throughput) with a minimum internal bus clock rate of 50 MHz
- Retransmission from transmit FIFO following a collision (no processor bus utilization)

- Automatic internal flushing of the receive FIFO for runts (collision fragments) and address recognition rejects (no processor bus utilization)
- Address recognition
 - Frames with broadcast address may be always accepted or always rejected
 - Exact match for single 48-bit individual (unicast) address
 - Hash (64-bit hash) check of individual (unicast) addresses
 - Hash (64-bit hash) check of group (multicast) addresses
 - Promiscuous mode

19.2 Modes of Operation

The primary operational modes are described in this section.

19.2.1 Full and Half Duplex Operation

Full duplex mode is for use on point-to-point links between switches or end node to switch. Half duplex mode works in connections between an end node and a repeater or between repeaters. TCR[FDEN] controls duplex mode selection.

When configured for full duplex mode, flow control may be enabled. Refer to the TCR[RFC_PAUSE, TFC_PAUSE] bits, the RCR[FCE] bit, and [Section 19.5.11, “Full Duplex Flow Control,”](#) for more details.

19.2.2 Interface Options

The following interface options are supported. A detailed discussion of the interface configurations is provided in [Section 19.5.6, “Network Interface Options.”](#)

19.2.2.1 10 Mbps and 100 Mbps MII Interface

The IEEE 802.3 standard defines the media independent interface (MII) for 10/100 Mbps operation. The MAC-PHY interface may be configured to operate in MII mode by setting RCR[MII_MODE].

FEC_TXCLK and FEC_RXCLK pins driven by the external transceiver determine the operation speed. The transceiver auto-negotiates the speed or software controls it via the serial management interface (FEC_MDC/FEC_MDIO pins) to the transceiver. Refer to the MMFR and MSCR register descriptions, as well as the section on the MII, for a description of how to read and write registers in the transceiver via this interface.

19.2.2.2 10 Mbps 7-Wire Interface Operation

The FEC supports 7-wire interface used by many 10 Mbps Ethernet transceivers. The RCR[MII_MODE] bit controls this functionality. If this bit is cleared, MII mode is disabled and the 10 Mbps 7-wire mode is enabled.

19.2.3 Address Recognition Options

The address options supported are promiscuous, broadcast reject, individual address (hash or exact match), and multicast hash match. Address recognition options are discussed in detail in [Section 19.5.9, “Ethernet Address Recognition.”](#)

19.2.4 Internal Loopback

Internal loopback mode is selected via RCR[LOOP]. Loopback mode is discussed in detail in [Section 19.5.14, “MII Internal and External Loopback.”](#)

19.3 External Signal Description

[Table 19-1](#) describes the various FEC signals, as well as indicating which signals work in available modes.

Table 19-1. FEC Signal Descriptions

Signal Name	MII	7-wire	Description
FEC_COL	X	X	Asserted upon detection of a collision and remains asserted while the collision persists. This signal is not defined for full-duplex mode.
FEC_CRS	X	—	When asserted, indicates that transmit or receive medium is not idle.
FEC_MDC	X	—	Output clock which provides a timing reference to the PHY for data transfers on the FEC_MDIO signal.
FEC_MDIO	X	—	Transfers control information between the external PHY and the media-access controller. Data is synchronous to FEC_MDC. This signal is an input after reset. When the FEC is operated in 10Mbps 7-wire interface mode, this signal should be connected to VSS.
FEC_RXCLK	X	X	Provides a timing reference for FEC_RXDV, FEC_RXD[3:0], and FEC_RXER.
FEC_RXDV	X	X	Asserting the FEC_RXDV input indicates that the PHY has valid nibbles present on the MII. FEC_RXDV should remain asserted from the first recovered nibble of the frame through to the last nibble. Assertion of FEC_RXDV must start no later than the SFD and exclude any EOF.
FEC_RXD0	X	X	This pin contains the Ethernet input data transferred from the PHY to the media-access controller when FEC_RXDV is asserted.
FEC_RXD1	X	—	This pin contains the Ethernet input data transferred from the PHY to the media access controller when FEC_RXDV is asserted.
FEC_RXD[3:2]	X	—	These pins contain the Ethernet input data transferred from the PHY to the media access controller when FEC_RXDV is asserted.
FEC_RXER	X	—	When asserted with FEC_RXDV, indicates that the PHY has detected an error in the current frame. When FEC_RXDV is not asserted FEC_RXER has no effect.
FEC_TXCLK	X	X	Input clock which provides a timing reference for FEC_TXEN, FEC_TXD[3:0] and FEC_TXER.
FEC_TXD0	X	X	The serial output Ethernet data and is only valid during the assertion of FEC_TXEN.
FEC_TXD1	X	—	This pin contains the serial output Ethernet data and is valid only during assertion of FEC_TXEN.
FEC_TXD[3:2]	X	—	These pins contain the serial output Ethernet data and are valid only during assertion of FEC_TXEN.

Table 19-1. FEC Signal Descriptions (continued)

Signal Name	MII	7-wire	Description
FEC_TXEN	X	X	Indicates when valid nibbles are present on the MII. This signal is asserted with the first nibble of a preamble and is negated before the first FEC_TXCLK following the final nibble of the frame.
FEC_TXER	X	—	When asserted for one or more clock cycles while FEC_TXEN is also asserted, the PHY sends one or more illegal symbols. FEC_TXER has no effect at 10 Mbps or when FEC_TXEN is negated.

19.4 Memory Map/Register Definition

The FEC is programmed by a combination of control/status registers (CSRs) and buffer descriptors. The CSRs control operation modes and extract global status information. The descriptors pass data buffers and related buffer information between the hardware and software.

Each FEC implementation requires a 1-Kbyte memory map space, which is divided into two sections of 512 bytes each for:

- Control/status registers
- Event/statistic counters held in the MIB block

Table 19-2 defines the top level memory map.

Table 19-2. Module Memory Map

Address	Function
0xFC03_0000 – FC03_01FF	Control/Status Registers
0xFC03_0200 – FC03_02FF	MIB Block Counters

Table 19-3 shows the FEC register memory map.

Table 19-3. FEC Register Memory Map

Address	Register	Width (bits)	Access	Reset Value	Section/Page
0xFC03_0004	Interrupt Event Register (EIR)	32	R/W	0x0000_0000	19.4.2/19-9
0xFC03_0008	Interrupt Mask Register (EIMR)	32	R/W	0x0000_0000	19.4.3/19-11
0xFC03_0010	Receive Descriptor Active Register (RDAR)	32	R/W	0x0000_0000	19.4.4/19-11
0xFC03_0014	Transmit Descriptor Active Register (TDAR)	32	R/W	0x0000_0000	19.4.5/19-12
0xFC03_0024	Ethernet Control Register (ECR)	32	R/W	0xF000_0000	19.4.6/19-13
0xFC03_0040	MII Management Frame Register (MMFR)	32	R/W	Undefined	19.4.7/19-13
0xFC03_0044	MII Speed Control Register (MSCR)	32	R/W	0x0000_0000	19.4.8/19-15
0xFC03_0064	MIB Control/Status Register (MIBC)	32	R/W	0x0000_0000	19.4.9/19-16
0xFC03_0084	Receive Control Register (RCR)	32	R/W	0x05EE_0001	19.4.10/19-16
0xFC03_00C4	Transmit Control Register (TCR)	32	R/W	0x0000_0000	19.4.11/19-17

Table 19-3. FEC Register Memory Map (continued)

Address	Register	Width (bits)	Access	Reset Value	Section/Page
0xFC03_00E4	Physical Address Low Register (PALR)	32	R/W	Undefined	19.4.12/19-18
0xFC03_00E8	Physical Address High Register (PAUR)	32	R/W	See Section	19.4.13/19-19
0xFC03_00EC	Opcode/Pause Duration (OPD)	32	R/W	See Section	19.4.14/19-19
0xFC03_0118	Descriptor Individual Upper Address Register (IAUR)	32	R/W	Undefined	19.4.15/19-20
0xFC03_011C	Descriptor Individual Lower Address Register (IALR)	32	R/W	Undefined	19.4.16/19-20
0xFC03_0120	Descriptor Group Upper Address Register (GAUR)	32	R/W	Undefined	19.4.17/19-21
0xFC03_0124	Descriptor Group Lower Address Register (GALR)	32	R/W	Undefined	19.4.18/19-21
0xFC03_0144	Transmit FIFO Watermark (TFWR)	32	R/W	0x0000_0000	19.4.19/19-21
0xFC03_014C	FIFO Receive Bound Register (FRBR)	32	R	0x0000_0600	19.4.20/19-22
0xFC03_0150	FIFO Receive FIFO Start Register (FRSR)	32	R	0x0000_0500	19.4.21/19-22
0xFC03_0180	Pointer to Receive Descriptor Ring (ERDSR)	32	R/W	Undefined	19.4.22/19-23
0xFC03_0184	Pointer to Transmit Descriptor Ring (ETDSR)	32	R/W	Undefined	19.4.23/19-23
0xFC03_0188	Maximum Receive Buffer Size (EMRBR)	32	R/W	Undefined	19.4.24/19-24

19.4.1 MIB Block Counters Memory Map

The MIB counters memory map ([Table 19-4](#)) defines the locations in the MIB RAM space where hardware-maintained counters reside. The counters are divided into two groups:

- RMON counters include the Ethernet statistics counters defined in RFC 1757
- A counter is included to count truncated frames since only frame lengths up to 2047 bytes are supported

The transmit and receive RMON counters are independent, which ensures accurate network statistics when operating in full duplex mode.

The included IEEE counters support the mandatory and recommended counter packages defined in Section 5 of ANSI/IEEE Std. 802.3 (1998 edition). The FEC supports IEEE Basic Package objects, but these do not require counters in the MIB block. In addition, some of the recommended package objects supported do not require MIB counters. Counters for transmit and receive full duplex flow control frames are also included.

Table 19-4. MIB Counters Memory Map

Address	Register
0xFC03_0200	Count of frames not counted correctly (RMON_T_DROP)
0xFC03_0204	RMON Tx packet count (RMON_T_PACKETS)
0xFC03_0208	RMON Tx broadcast packets (RMON_T_BC_PKT)
0xFC03_020C	RMON Tx multicast packets (RMON_T_MC_PKT)

Table 19-4. MIB Counters Memory Map (continued)

Address	Register
0xFC03_0210	RMON Tx packets with CRC/align error (RMON_T_CRC_ALIGN)
0xFC03_0214	RMON Tx packets < 64 bytes, good CRC (RMON_T_UNDERSIZE)
0xFC03_0218	RMON Tx packets > MAX_FL bytes, good CRC (RMON_T_OVERSIZE)
0xFC03_021C	RMON Tx packets < 64 bytes, bad CRC (RMON_T_FRAG)
0xFC03_0220	RMON Tx packets > MAX_FL bytes, bad CRC (RMON_T_JAB)
0xFC03_0224	RMON Tx collision count (RMON_T_COL)
0xFC03_0228	RMON Tx 64 byte packets (RMON_T_P64)
0xFC03_022C	RMON Tx 65 to 127 byte packets (RMON_T_P65TO127)
0xFC03_0230	RMON Tx 128 to 255 byte packets (RMON_T_P128TO255)
0xFC03_0234	RMON Tx 256 to 511 byte packets (RMON_T_P256TO511)
0xFC03_0238	RMON Tx 512 to 1023 byte packets (RMON_T_P512TO1023)
0xFC03_023C	RMON Tx 1024 to 2047 byte packets (RMON_T_P1024TO2047)
0xFC03_0240	RMON Tx packets with > 2048 bytes (RMON_T_P_GTE2048)
0xFC03_0244	RMON Tx Octets (RMON_T_OCTETS)
0xFC03_0248	Count of transmitted frames not counted correctly (IEEE_T_DROP)
0xFC03_024C	Frames transmitted OK (IEEE_T_FRAME_OK)
0xFC03_0250	Frames transmitted with single collision (IEEE_T_1COL)
0xFC03_0254	Frames transmitted with multiple collisions (IEEE_T_MCOL)
0xFC03_0258	Frames transmitted after deferral delay (IEEE_T_DEF)
0xFC03_025C	Frames transmitted with late collision (IEEE_T_LCOL)
0xFC03_0260	Frames transmitted with excessive collisions (IEEE_T_EXCOL)
0xFC03_0264	Frames transmitted with Tx FIFO underrun (IEEE_T_MACERR)
0xFC03_0268	Frames transmitted with carrier sense error (IEEE_T_CSERR)
0xFC03_026C	Frames transmitted with SQE error (IEEE_T_SQE)
0xFC03_0270	Flow control pause frames transmitted (IEEE_T_FDXFC)
0xFC03_0274	Octet count for frames transmitted without error (IEEE_T_OCTETS_OK)
0xFC03_0280	Count of received frames not counted correctly (RMON_R_DROP)
0xFC03_0284	RMON Rx packet count (RMON_R_PACKETS)
0xFC03_0288	RMON Rx broadcast packets (RMON_R_BC_PKT)
0xFC03_028C	RMON Rx multicast packets (RMON_R_MC_PKT)
0xFC03_0290	RMON Rx packets with CRC/Align error (RMON_R_CRC_ALIGN)
0xFC03_0294	RMON Rx packets < 64 bytes, good CRC (RMON_R_UNDERSIZE)
0xFC03_0298	RMON Rx packets > MAX_FL bytes, good CRC (RMON_R_OVERSIZE)

Table 19-4. MIB Counters Memory Map (continued)

Address	Register
0xFC03_029C	RMON Rx packets < 64 bytes, bad CRC (RMON_R_FRAG)
0xFC03_02A0	RMON Rx packets > MAX_FL bytes, bad CRC (RMON_R_JAB)
0xFC03_02A4	Reserved (RMON_R_RESVD_0)
0xFC03_02A8	RMON Rx 64 byte packets (RMON_R_P64)
0xFC03_02AC	RMON Rx 65 to 127 byte packets (RMON_R_P65TO127)
0xFC03_02B0	RMON Rx 128 to 255 byte packets (RMON_R_P128TO255)
0xFC03_02B4	RMON Rx 256 to 511 byte packets (RMON_R_P256TO511)
0xFC03_02B8	RMON Rx 512 to 1023 byte packets (RMON_R_P512TO1023)
0xFC03_02BC	RMON Rx 1024 to 2047 byte packets (RMON_R_P1024TO2047)
0xFC03_02C0	RMON Rx packets with > 2048 bytes (RMON_R_P_GTE2048)
0xFC03_02C4	RMON Rx octets (RMON_R_OCTETS)
0xFC03_02C8	Count of received frames not counted correctly (IEEE_R_DROP)
0xFC03_02CC	Frames received OK (IEEE_R_FRAME_OK)
0xFC03_02D0	Frames received with CRC error (IEEE_R_CRC)
0xFC03_02D4	Frames received with alignment error (IEEE_R_ALIGN)
0xFC03_02D8	Receive FIFO overflow count (IEEE_R_MACERR)
0xFC03_02DC	Flow control pause frames received (IEEE_R_FDXFC)
0xFC03_02E0	Octet count for frames received without error (IEEE_R_OCTETS_OK)

19.4.2 Ethernet Interrupt Event Register (EIR)

When an event occurs that sets a bit in EIR, an interrupt occurs if the corresponding bit in the interrupt mask register (EIMR) is also set. Writing a 1 to an EIR bit clears it; writing 0 has no effect. This register is cleared upon hardware reset.

These interrupts can be divided into operational interrupts, transceiver/network error interrupts, and internal error interrupts. Interrupts which may occur in normal operation are GRA, TXF, TXB, RXF, RXB, and MII. Interrupts resulting from errors/problems detected in the network or transceiver are HBERR, BABR, BABT, LC, and RL. Interrupts resulting from internal errors are HBERR and UN.

Some of the error interrupts are independently counted in the MIB block counters:

- HBERR - IEEE_T_SQE
- BABR - RMON_R_OVERSIZE (good CRC), RMON_R_JAB (bad CRC)
- BABT - RMON_T_OVERSIZE (good CRC), RMON_T_JAB (bad CRC)
- LATE_COL - IEEE_T_LCOL
- COL_RETRY_LIM - IEEE_T_EXCOL
- XFIFO_UN - IEEE_T_MACERR

Software may choose to mask off these interrupts because these errors are visible to network management via the MIB counters.

Address: 0xFC03_0004

Access: User read/write

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
R	HB ERR	BABR	BABT	GRA	TXF	TXB	RXF	RXB	MII	EB ERR	LC	RL	UN	0	0	0
W	w1c	w1c	w1c	w1c	w1c	w1c	w1c	w1c	w1c	w1c	w1c	w1c	w1c			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
W																
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Figure 19-2. Ethernet Interrupt Event Register (EIR)

Table 19-5. EIR Field Descriptions

Field	Description
31 HBERR	Heartbeat error. Indicates TCR[HBC] is set and that the COL input was not asserted within the heartbeat window following a transmission.
30 BABR	Babbling receive error. Indicates a frame was received with length in excess of RCR[MAX_FL] bytes.
29 BABT	Babbling transmit error. Indicates the transmitted frame length exceeds RCR[MAX_FL] bytes. Usually this condition is caused by a frame that is too long is placed into the transmit data buffer(s). Truncation does not occur.
28 GRA	Graceful stop complete. Indicates the graceful stop is complete. During graceful stop the transmitter is placed into a pause state after completion of the frame currently being transmitted. This bit is set by one of three conditions: 1) A graceful stop initiated by the setting of the TCR[GTS] bit is now complete. 2) A graceful stop initiated by the setting of the TCR[TFC_PAUSE] bit is now complete. 3) A graceful stop initiated by the reception of a valid full duplex flow control pause frame is now complete. Refer to Section 19.5.11, "Full Duplex Flow Control."
27 TXF	Transmit frame interrupt. Indicates a frame has been transmitted and the last corresponding buffer descriptor has been updated.
26 TXB	Transmit buffer interrupt. Indicates a transmit buffer descriptor has been updated.
25 RXF	Receive frame interrupt. Indicates a frame has been received and the last corresponding buffer descriptor has been updated.
24 RXB	Receive buffer interrupt. Indicates a receive buffer descriptor not the last in the frame has been updated.
23 MII	MII interrupt. Indicates the MII has completed the data transfer requested.
22 EBERR	Ethernet bus error. Indicates a system bus error occurred when a DMA transaction is underway. When the EBERR bit is set, ECR[ETHER_EN] is cleared, halting frame processing by the FEC. When this occurs, software needs to ensure that the FIFO controller and DMA also soft reset.
21 LC	Late collision. Indicates a collision occurred beyond the collision window (slot time) in half duplex mode. The frame truncates with a bad CRC and the remainder of the frame is discarded.

Table 19-5. EIR Field Descriptions (continued)

Field	Description
20 RL	Collision retry limit. Indicates a collision occurred on each of 16 successive attempts to transmit the frame. The frame is discarded without being transmitted and transmission of the next frame commences. This error can only occur in half duplex mode.
19 UN	Transmit FIFO underrun. Indicates the transmit FIFO became empty before the complete frame was transmitted. A bad CRC is appended to the frame fragment and the remainder of the frame is discarded.
18–0	Reserved, must be cleared.

19.4.3 Interrupt Mask Register (EIMR)

The EIMR register controls which interrupt events are allowed to generate actual interrupts. All implemented bits in this CSR are read/write. A hardware reset clears this register. If the corresponding bits in the EIR and EIMR registers are set, an interrupt is generated. The interrupt signal remains asserted until a 1 is written to the EIR bit (write 1 to clear) or a 0 is written to the EIMR bit.

Address: 0xFC03_0008

Access: User read/write

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
R	HB	BABR	BABT	GRA	TXF	TXB	RXF	RXB	MII	EB	LC	RL	UN	0	0	0
W	ERR									ERR						
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
W																
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Figure 19-3. Ethernet Interrupt Mask Register (EIMR)

Table 19-6. EIMR Field Descriptions

Field	Description
31–19 See Figure 19-3 and Table 19-5	Interrupt mask. Each bit corresponds to an interrupt source defined by the EIR register. The corresponding EIMR bit determines whether an interrupt condition can generate an interrupt. At every processor clock, the EIR samples the signal generated by the interrupting source. The corresponding EIR bit reflects the state of the interrupt signal even if the corresponding EIMR bit is set. 0 The corresponding interrupt source is masked. 1 The corresponding interrupt source is not masked.
18–0	Reserved, must be cleared.

19.4.4 Receive Descriptor Active Register (RDAR)

RDAR is a command register, written by the user, indicating the receive descriptor ring is updated (the driver produced empty receive buffers with the empty bit set).

When the register is written, the RDAR bit is set. This is independent of the data actually written by the user. When set, the FEC polls the receive descriptor ring and processes receive frames (provided

ECR[ETHER_EN] is also set). After the FEC polls a receive descriptor whose empty bit is not set, FEC clears the RDAR bit and ceases receive descriptor ring polling until the user sets the bit again, signifying that additional descriptors are placed into the receive descriptor ring.

The RDAR register is cleared at reset and when ECR[ETHER_EN] is cleared.

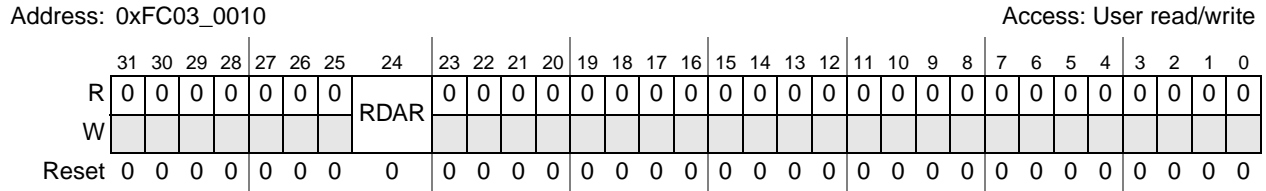


Figure 19-4. Receive Descriptor Active Register (RDAR)

Table 19-7. RDAR Field Descriptions

Field	Description
31–25	Reserved, must be cleared.
24 RDAR	Set to 1 when this register is written, regardless of the value written. Cleared by the FEC device when no additional empty descriptors remain in the receive ring. Also cleared when ECR[ETHER_EN] is cleared.
23–0	Reserved, must be cleared.

19.4.5 Transmit Descriptor Active Register (TDAR)

The TDAR is a command register which the user writes to indicate the transmit descriptor ring is updated (transmit buffers have been produced by the driver with the ready bit set in the buffer descriptor).

When the register is written, the TDAR bit is set. This value is independent of the data actually written by the user. When set, the FEC polls the transmit descriptor ring and processes transmit frames (provided ECR[ETHER_EN] is also set). After the FEC polls a transmit descriptor that is a ready bit not set, FEC clears the TDAR bit and ceases transmit descriptor ring polling until the user sets the bit again, signifying additional descriptors are placed into the transmit descriptor ring.

The TDAR register is cleared at reset, when ECR[ETHER_EN] is cleared, or when ECR[RESET] is set.

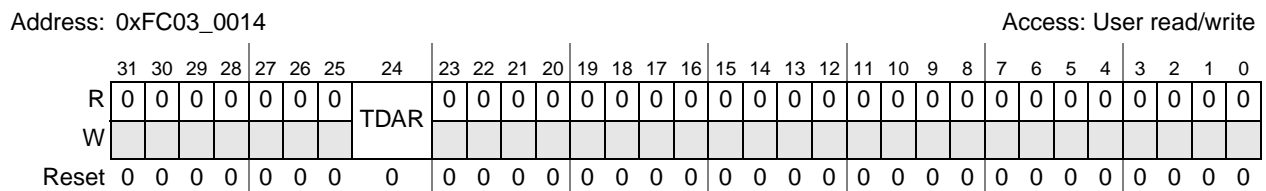


Figure 19-5. Transmit Descriptor Active Register (TDAR)

Table 19-8. TDAR Field Descriptions

Field	Description
31–25	Reserved, must be cleared.

Table 19-8. TDAR Field Descriptions (continued)

Field	Description
24 TDAR	Set to 1 when this register is written, regardless of the value written. Cleared by the FEC device when no additional ready descriptors remain in the transmit ring. Also cleared when ECR[ETHER_EN] is cleared.
23–0	Reserved, must be cleared.

19.4.6 Ethernet Control Register (ECR)

ECR is a read/write user register, though hardware may alter fields in this register as well. The ECR enables/disables the FEC.

Address: 0xFC03_0024

Access: User read/write

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
W																																
Reset	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

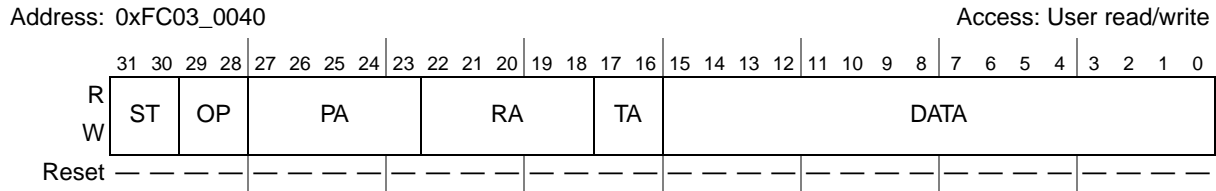
Figure 19-6. Ethernet Control Register (ECR)

Table 19-9. ECR Field Descriptions

Field	Description
31–2	Reserved, must be cleared.
1 ETHER_EN	When this bit is set, FEC is enabled, and reception and transmission are possible. When this bit is cleared, reception immediately stops and transmission stops after a bad CRC is appended to any currently transmitted frame. The buffer descriptor(s) for an aborted transmit frame are not updated after clearing this bit. When ETHER_EN is cleared, the DMA, buffer descriptor, and FIFO control logic are reset, including the buffer descriptor and FIFO pointers. Hardware alters the ETHER_EN bit under the following conditions: <ul style="list-style-type: none"> • ECR[RESET] is set by software, in which case ETHER_EN is cleared • An error condition causes the EIR[EBERR] bit to set, in which case ETHER_EN is cleared
0 RESET	When this bit is set, the equivalent of a hardware reset is performed but it is local to the FEC. ECR[ETHER_EN] is cleared and all other FEC registers take their reset values. Also, any transmission/reception currently in progress is abruptly aborted. This bit is automatically cleared by hardware during the reset sequence. The reset sequence takes approximately eight internal bus clock cycles after this bit is set.

19.4.7 MII Management Frame Register (MMFR)

The MMFR is user-accessible and does not reset to a defined value. The MMFR register is used to communicate with the attached MII compatible PHY device(s), providing read/write access to their MII registers. Performing a write to the MMFR causes a management frame to be sourced unless the MSCR is programmed to 0. If MSCR is cleared while MMFR is written and then MSCR is written with a non-zero value, an MII frame is generated with the data previously written to the MMFR. This allows MMFR and MSCR to be programmed in either order if MSCR is currently zero.

**Figure 19-7. MII Management Frame Register (MMFR)****Table 19-10. MMFR Field Descriptions**

Field	Description
31–30 ST	Start of frame delimiter. These bits must be programmed to 0b01 for a valid MII management frame.
29–28 OP	Operation code. 00 Write frame operation, but not MII compliant. 01 Write frame operation for a valid MII management frame. 10 Read frame operation for a valid MII management frame. 11 Read frame operation, but not MII compliant.
27–23 PA	PHY address. This field specifies one of up to 32 attached PHY devices.
22–18 RA	Register address. This field specifies one of up to 32 registers within the specified PHY device.
17–16 TA	Turn around. This field must be programmed to 10 to generate a valid MII management frame.
15–0 DATA	Management frame data. This is the field for data to be written to or read from the PHY register.

To perform a read or write operation on the MII Management Interface, write the MMFR register. To generate a valid read or write management frame, ST field must be written with a 01 pattern, and the TA field must be written with a 10. If other patterns are written to these fields, a frame is generated, but does not comply with the IEEE 802.3 MII definition.

To generate an IEEE 802.3-compliant MII Management Interface write frame (write to a PHY register), the user must write {01 01 PHYAD REGAD 10 DATA} to the MMFR register. Writing this pattern causes the control logic to shift out the data in the MMFR register following a preamble generated by the control state machine. During this time, contents of the MMFR register are altered as the contents are serially shifted and are unpredictable if read by the user. After the write management frame operation completes, the MII interrupt is generated. At this time, contents of the MMFR register match the original value written.

To generate an MII management interface read frame (read a PHY register), the user must write {01 10 PHYAD REGAD 10 XXXX} to the MMFR register (the content of the DATA field is a don't care). Writing this pattern causes the control logic to shift out the data in the MMFR register following a preamble generated by the control state machine. During this time, contents of the MMFR register are altered as the contents are serially shifted and are unpredictable if read by the user. After the read management frame operation completes, the MII interrupt is generated. At this time, the contents of the MMFR register match

the original value written except for the DATA field whose contents are replaced by the value read from the PHY register.

If the MMFR register is written while frame generation is in progress, the frame contents are altered. Software must use the MII interrupt to avoid writing to the MMFR register while frame generation is in progress.

19.4.8 MII Speed Control Register (MSCR)

The MSCR provides control of the MII clock (FEC_MDC pin) frequency and allows a preamble drop on the MII management frame.

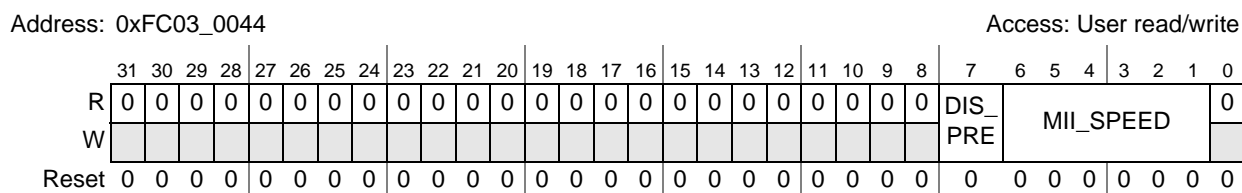


Figure 19-8. MII Speed Control Register (MSCR)

Table 19-11. MSCR Field Descriptions

Field	Description
31–8	Reserved, must be cleared.
7 DIS_PRE	Setting this bit causes the preamble (32 ones) not to be prepended to the MII management frame. The MII standard allows the preamble to be dropped if the attached PHY device(s) does not require it.
6–1 MII_SPEED	Controls the frequency of the MII management interface clock (FEC_MDC) relative to the internal bus clock. A value of 0 in this field turns off the FEC_MDC and leaves it in low voltage state. Any non-zero value results in the FEC_MDC frequency of $1/(\text{MII_SPEED} \times 2)$ of the internal bus frequency.
0	Reserved, must be cleared.

The MII_SPEED field must be programmed with a value to provide an FEC_MDC frequency of less than or equal to 2.5 MHz to be compliant with the IEEE 802.3 MII specification. The MII_SPEED must be set to a non-zero value to source a read or write management frame. After the management frame is complete, the MSCR register may optionally be set to 0 to turn off the FEC_MDC. The FEC_MDC generated has a 50% duty cycle except when MII_SPEED changes during operation (change takes effect following a rising or falling edge of FEC_MDC).

If the internal bus clock is 25 MHz, programming this register to 0x0000_0005 results in an FEC_MDC as stated the equation below.

$$25 \text{ MHz} \times \frac{1}{5 \times 2} = 2.5 \text{ MHz} \quad \text{Eqn. 19-1}$$

A table showing optimum values for MII_SPEED as a function of internal bus clock frequency is provided below.

Table 19-12. Programming Examples for MSCR

Internal FEC Clock Frequency	MSCR[MII_SPEED]	FEC_MDC frequency
25 MHz	0x5	2.50 MHz
33 MHz	0x7	2.36 MHz
40 MHz	0x8	2.50 MHz
50 MHz	0xA	2.50 MHz
66 MHz	0xE	2.36 MHz

19.4.9 MIB Control Register (MIBC)

The MIBC is a read/write register controlling and observing the state of the MIB block. User software accesses this register if there is a need to disable the MIB block operation. For example, to clear all MIB counters in RAM:

1. Disable the MIB block
2. Clear all the MIB RAM locations
3. Enable the MIB block

The MIB_DIS bit is reset to 1. See [Table 19-4](#) for the locations of the MIB counters.

Address: 0xFC03_0064

Access: User read/write

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	MIB_DIS	MIB_IDLE	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	
W																																
Reset	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	

Figure 19-9. MIB Control Register (MIBC)

Table 19-13. MIBC Field Descriptions

Field	Description
31 MIB_DIS	A read/write control bit. If set, the MIB logic halts and not update any MIB counters.
30 MIB_IDLE	A read-only status bit. If set the MIB block is not currently updating any MIB counters.
29–0	Reserved.

19.4.10 Receive Control Register (RCR)

RCR controls the operational mode of the receive block and must be written only when ECR[ETHER_EN] is cleared (initialization time).

Address: 0xFC03_0084

Access: User read/write

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
R	0	0	0	0	0	MAX_FL										
W																
Reset	0	0	0	0	0	1	0	1	1	1	1	0	1	1	1	0

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	0	0	0	0	0	0	0	0	0	0	FCE	BC_REJ	PROM	MII_MODE	DRT	LOOP
W																
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1

Figure 19-10. Receive Control Register (RCR)

Table 19-14. RCR Field Descriptions

Field	Description
31–27	Reserved, must be cleared.
26–16 MAX_FL	Maximum frame length. Resets to decimal 1518. Length is measured starting at DA and includes the CRC at the end of the frame. Transmit frames longer than MAX_FL causes the BABT interrupt to occur. Receive frames longer than MAX_FL causes the BABR interrupt to occur and sets the LG bit in the end of frame receive buffer descriptor. The recommended default value to be programmed is 1518 or 1522 if VLAN tags are supported.
15–6	Reserved, must be cleared.
5 FCE	Flow control enable. If asserted, the receiver detects PAUSE frames. Upon PAUSE frame detection, the transmitter stops transmitting data frames for a given duration.
4 BC_REJ	Broadcast frame reject. If asserted, frames with DA (destination address) equal to FFFF_FFFF_FFFF are rejected unless the PROM bit is set. If BC_REJ and PROM are set, frames with broadcast DA are accepted and the M (MISS) is set in the receive buffer descriptor.
3 PROM	Promiscuous mode. All frames are accepted regardless of address matching.
2 MII_MODE	Media independent interface mode. Selects the external interface mode for transmit and receive blocks. 0 7-wire mode (used only for serial 10 Mbps) 1 MII mode
1 DRT	Disable receive on transmit. 0 Receive path operates independently of transmit (use for full duplex or to monitor transmit activity in half duplex mode). 1 Disable reception of frames while transmitting (normally used for half duplex mode).
0 LOOP	Internal loopback. If set, transmitted frames are looped back internal to the device and transmit output signals are not asserted. The internal bus clock substitutes for the FEC_TXCLK when LOOP is asserted. DRT must be set to 0 when setting LOOP.

19.4.11 Transmit Control Register (TCR)

TCR is read/write and configures the transmit block. This register is cleared at system reset. Bits 2 and 1 must be modified only when ECR[ETHER_EN] is cleared.

Address: 0xFC03_00C4

Access: User read/write

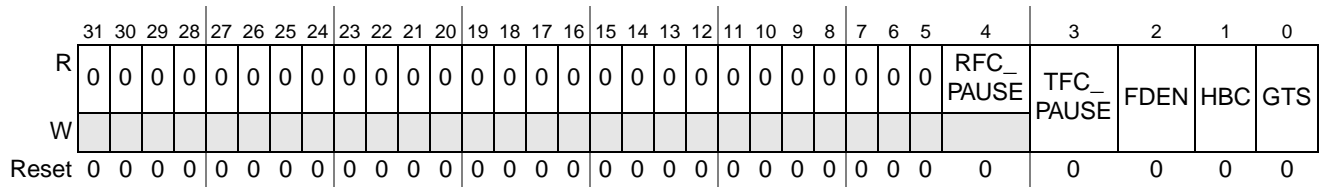


Figure 19-11. Transmit Control Register (TCR)

Table 19-15. TCR Field Descriptions

Field	Description
31–5	Reserved, must be cleared.
4 RFC_PAUSE	Receive frame control pause. This read-only status bit is asserted when a full duplex flow control pause frame is received and the transmitter pauses for the duration defined in this pause frame. This bit automatically clears when the pause duration is complete.
3 TFC_PAUSE	Transmit frame control pause. Transmits a PAUSE frame when asserted. When this bit is set, the MAC stops transmission of data frames after the current transmission is complete. At this time, GRA interrupt in the EIR register is asserted. With transmission of data frames stopped, MAC transmits a MAC Control PAUSE frame. Next, the MAC clears the TFC_PAUSE bit and resumes transmitting data frames. If the transmitter pauses due to user assertion of GTS or reception of a PAUSE frame, the MAC may continue transmitting a MAC Control PAUSE frame.
2 FDEN	Full duplex enable. If set, frames transmit independent of carrier sense and collision inputs. This bit should only be modified when ECR[ETHER_EN] is cleared.
1 HBC	Heartbeat control. If set, the heartbeat check performs following end of transmission and the HB bit in the status register is set if the collision input does not assert within the heartbeat window. This bit should only be modified when ECR[ETHER_EN] is cleared.
0 GTS	Graceful transmit stop. When this bit is set, MAC stops transmission after any frame currently transmitted is complete and GRA interrupt in the EIR register is asserted. If frame transmission is not currently underway, the GRA interrupt is asserted immediately. After transmission finishes, clear GTS to restart. The next frame in the transmit FIFO is then transmitted. If an early collision occurs during transmission when GTS is set, transmission stops after the collision. The frame is transmitted again after GTS is cleared. There may be old frames in the transmit FIFO that transmit when GTS is reasserted. To avoid this, clear ECR[ETHER_EN] following the GRA interrupt.

19.4.12 Physical Address Lower Register (PALR)

PALR contains the lower 32 bits (bytes 0,1,2,3) of the 48-bit address used in the address recognition process to compare with the DA (destination address) field of receive frames with an individual DA. In addition, this register is used in bytes 0 through 3 of the 6-byte source address field when transmitting PAUSE frames. This register is not reset and you must initialize it.

Address: 0xFC03_00E4

Access: User read/write

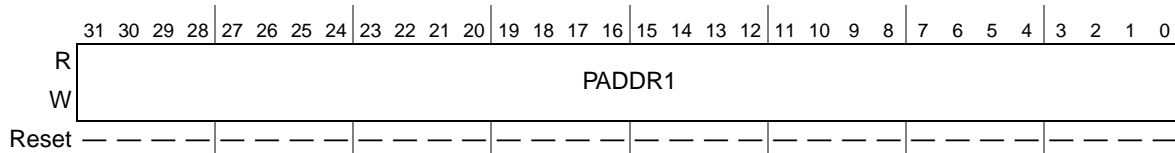


Figure 19-12. Physical Address Lower Register (PALR)

Table 19-16. PALR Field Descriptions

Field	Description
31–0 PADDR1	Bytes 0 (bits 31:24), 1 (bits 23:16), 2 (bits 15:8), and 3 (bits 7:0) of the 6-byte individual address are used for exact match and the source address field in PAUSE frames.

19.4.13 Physical Address Upper Register (PAUR)

PAUR contains the upper 16 bits (bytes 4 and 5) of the 48-bit address used in the address recognition process to compare with the DA (destination address) field of receive frames with an individual DA. In addition, this register is used in bytes 4 and 5 of the 6-byte Source Address field when transmitting PAUSE frames. Bits 15:0 of PAUR contain a constant type field (0x8808) for transmission of PAUSE frames. The upper 16 bits of this register are not reset and you must initialize it.

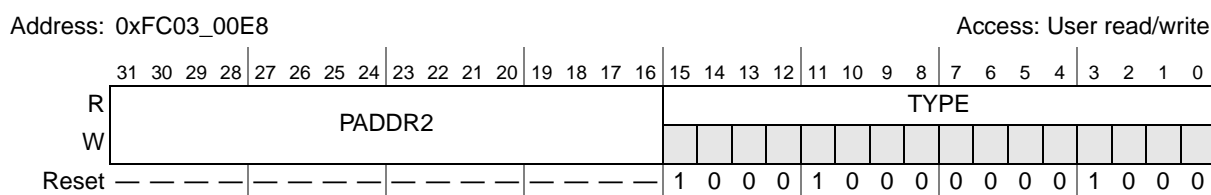


Figure 19-13. Physical Address Upper Register (PAUR)

Table 19-17. PAUR Field Descriptions

Field	Description
31–16 PADDR2	Bytes 4 (bits 31:24) and 5 (bits 23:16) of the 6-byte individual address used for exact match, and the source address field in PAUSE frames.
15–0 TYPE	Type field in PAUSE frames. These 16 read-only bits are a constant value of 0x8808.

19.4.14 Opcode/Pause Duration Register (OPD)

The OPD is read/write accessible. This register contains the 16-bit opcode and 16-bit pause duration fields used in transmission of a PAUSE frame. The opcode field is a constant value, 0x0001. When another node detects a PAUSE frame, that node pauses transmission for the duration specified in the pause duration field. The lower 16 bits of this register are not reset and you must initialize them.

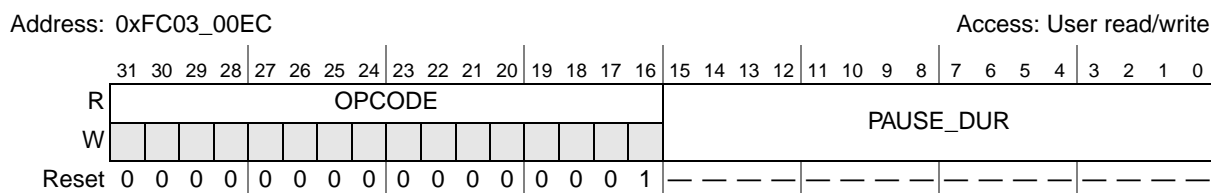


Figure 19-14. Opcode/Pause Duration Register (OPD)

Table 19-18. OPD Field Descriptions

Field	Description
31–16 OPCODE	Opcode field used in PAUSE frames. These read-only bits are a constant, 0x0001.
15–0 PAUSE_DUR	Pause Duration field used in PAUSE frames.

19.4.15 Descriptor Individual Upper Address Register (IAUR)

IAUR contains the upper 32 bits of the 64-bit individual address hash table. The address recognition process uses this table to check for a possible match with the destination address (DA) field of receive frames with an individual DA. This register is not reset and you must initialize it.

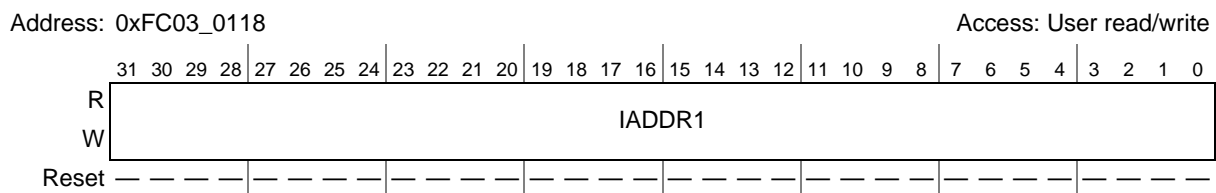


Figure 19-15. Descriptor Individual Upper Address Register (IAUR)

Table 19-19. IAUR Field Descriptions

Field	Description
31–0 IADDR1	The upper 32 bits of the 64-bit hash table used in the address recognition process for receive frames with a unicast address. Bit 31 of IADDR1 contains hash index bit 63. Bit 0 of IADDR1 contains hash index bit 32.

19.4.16 Descriptor Individual Lower Address Register (IALR)

IALR contains the lower 32 bits of the 64-bit individual address hash table. The address recognition process uses this table to check for a possible match with the DA field of receive frames with an individual DA. This register is not reset and you must initialize it.



Figure 19-16. Descriptor Individual Lower Address Register (IALR)

Table 19-20. IALR Field Descriptions

Field	Description
31–0 IADDR2	The lower 32 bits of the 64-bit hash table used in the address recognition process for receive frames with a unicast address. Bit 31 of IADDR2 contains hash index bit 31. Bit 0 of IADDR2 contains hash index bit 0.

19.4.17 Descriptor Group Upper Address Register (GAUR)

GAUR contains the upper 32 bits of the 64-bit hash table used in the address recognition process for receive frames with a multicast address. You must initialize this register.

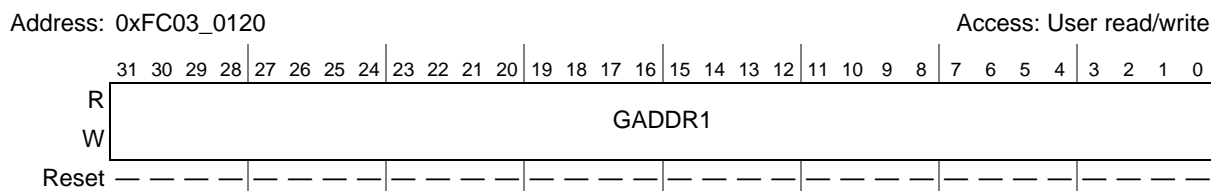


Figure 19-17. Descriptor Group Upper Address Register (GAUR)

Table 19-21. GAUR Field Descriptions

Field	Description
31–0 GADDR1	The GADDR1 register contains the upper 32 bits of the 64-bit hash table used in the address recognition process for receive frames with a multicast address. Bit 31 of GADDR1 contains hash index bit 63. Bit 0 of GADDR1 contains hash index bit 32.

19.4.18 Descriptor Group Lower Address Register (GALR)

GALR contains the lower 32 bits of the 64-bit hash table used in the address recognition process for receive frames with a multicast address. You must initialize this register.

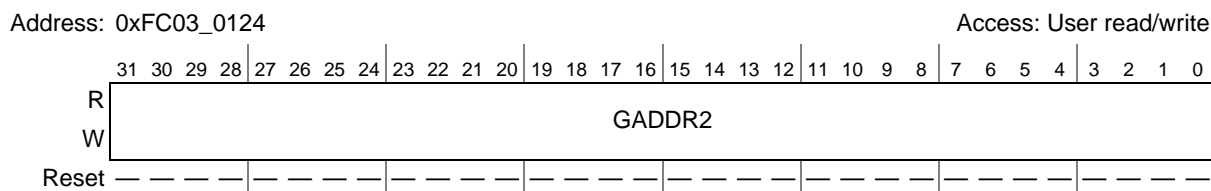


Figure 19-18. Descriptor Group Lower Address Register (GALR)

Table 19-22. GALR Field Descriptions

Field	Description
31–0 GADDR2	The GADDR2 register contains the lower 32 bits of the 64-bit hash table used in the address recognition process for receive frames with a multicast address. Bit 31 of GADDR2 contains hash index bit 31. Bit 0 of GADDR2 contains hash index bit 0.

19.4.19 Transmit FIFO Watermark Register (TFWR)

The TFWR controls the amount of data required in the transmit FIFO before transmission of a frame can begin. This allows you to minimize transmit latency (TFWR = 00 or 01) or allow for larger bus access latency (TFWR = 11) due to contention for the system bus. Setting the watermark to a high value minimizes the risk of transmit FIFO underrun due to contention for the system bus. The byte counts associated with the TFWR field may need to be modified to match a given system requirement (worst case bus access latency by the transmit data DMA channel).

Address: 0xFC03_0144

Access: User read/write

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
W																																
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Figure 19-19. Transmit FIFO Watermark Register (TFWR)

Table 19-23. TFWR Field Descriptions

Field	Description
31–2	Reserved, must be cleared.
1–0 TFWR	Number of bytes written to transmit FIFO before transmission of a frame begins 00 64 bytes written 01 64 bytes written 10 128 bytes written 11 192 bytes written

19.4.20 FIFO Receive Bound Register (FRBR)

FRBR indicates the upper address bound of the FIFO RAM. Drivers can use this value, along with the FRSR, to appropriately divide the available FIFO RAM between the transmit and receive data paths.

Address: 0xFC03_014C

Access: User read-only

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1									0	0
W																																
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	0	0	0	0	0	0	0	0	0

Figure 19-20. FIFO Receive Bound Register (FRBR)

Table 19-24. FRBR Field Descriptions

Field	Description
31–10	Reserved, read as 0 (except bit 10, which is read as 1).
9–2 R_BOUND	Read-only. Highest valid FIFO RAM address.
1–0	Reserved, read as 0.

19.4.21 FIFO Receive Start Register (FRSR)

FRSR indicates the starting address of the receive FIFO. FRSR marks the boundary between the transmit and receive FIFOs. The transmit FIFO uses addresses from the start of the FIFO to the location four bytes before the address programmed into the FRSR. The receive FIFO uses addresses from FRSR to FRBR inclusive.

Hardware initializes the FRSR register at reset. FRSR only needs to be written to change the default value.

Address: 0xFC03_0150

Access: User read/write

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0		
R	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	R_FSTART										0	0
W																																		
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	1	0	0	0	0	0	0	0	0		

Figure 19-21. FIFO Receive Start Register (FRSR)

Table 19-25. FRSR Field Descriptions

Field	Description
31–11	Reserved, must be cleared.
10	Reserved, must be set.
9–2 R_FSTART	Address of first receive FIFO location. Acts as delimiter between receive and transmit FIFOs. For proper operation, ensure that R_FSTART is set to 0x48 or greater.
1–0	Reserved, must be cleared.

19.4.22 Receive Descriptor Ring Start Register (ERDSR)

ERDSR points to the start of the circular receive buffer descriptor queue in external memory. This pointer must be 32-bit aligned; however, it is recommended it be made 128-bit aligned (evenly divisible by 16).

This register is not reset and must be initialized prior to operation.

Address: 0xFC03_0180

Access: User read/write

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	R_DES_START																														0	0
W																																
Reset	— — — —				— — — —				— — — —				— — — —				— — — —				— — — —				— — — —							

Figure 19-22. Ethernet Receive Descriptor Ring Start Register (ERDSR)

Table 19-26. ERDSR Field Descriptions

Field	Description
31–2 R_DES_START	Pointer to start of receive buffer descriptor queue.
1–0	Reserved, must be cleared.

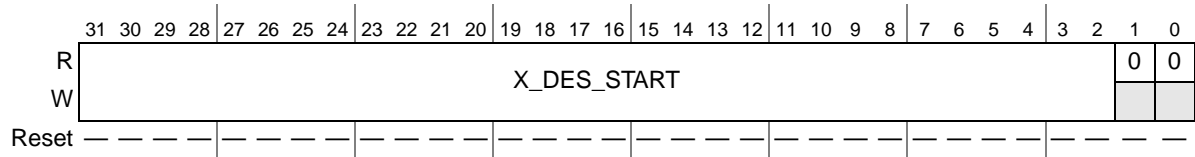
19.4.23 Transmit Buffer Descriptor Ring Start Registers (ETSDR)

ETSDR provides a pointer to the start of the circular transmit buffer descriptor queue in external memory. This pointer must be 32-bit aligned; however, it is recommended it be made 128-bit aligned (evenly divisible by 16). You should write zeros to bits 1 and 0. Hardware ignores non-zero values in these two bit positions.

This register is undefined at reset and must be initialized prior to operation.

Address: 0xFC03_0184

Access: User read/write

**Figure 19-23. Transmit Buffer Descriptor Ring Start Register (ETDSR)****Table 19-27. ETDSR Field Descriptions**

Field	Description
31–2 X_DES_START	Pointer to start of transmit buffer descriptor queue.
1–0	Reserved, must be cleared.

19.4.24 Receive Buffer Size Register (EMRBR)

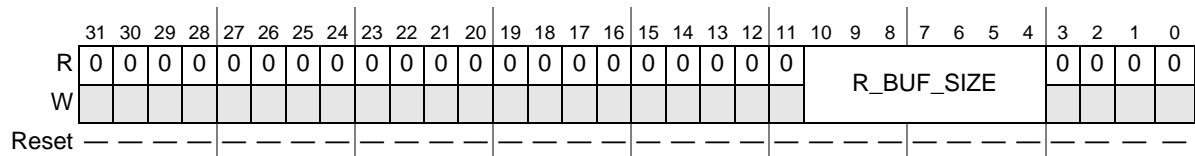
The EMRBR is a user-programmable register that dictates the maximum size of all receive buffers. This value should take into consideration that the receive CRC is always written into the last receive buffer. To allow one maximum size frame per buffer, EMRBR must be set to RCR[MAX_FL] or larger. To properly align the buffer, EMRBR must be evenly divisible by 16. To ensure this, bits 3–0 are forced low.

To minimize bus utilization (descriptor fetches), it is recommended that EMRBR be greater than or equal to 256 bytes.

The EMRBR register is undefined at reset and must be initialized by the user.

Address: 0xFC03_0188

Access: User read/write

**Figure 19-24. Receive Buffer Size Register (EMRBR)****Table 19-28. EMRBR Field Descriptions**

Field	Description
31–11	Reserved, must be cleared.
10–4 R_BUF_SIZE	Maximum size of receive buffer size in bytes. To minimize bus utilization (descriptor fetches), set this field to 256 bytes (0x10) or larger. 0x10 256 + 15 bytes (minimum size recommended) 0x11 272 + 15 bytes ... 0x7F 2032 + 15 bytes. The FEC writes up to 2047 bytes in the receive buffer. If data larger than 2047 is received, the FEC truncates it and shows 0x7FF in the receive descriptor
3–0	Reserved, must be cleared.

19.5 Functional Description

This section describes the operation of the FEC, beginning with the buffer descriptors, the hardware and software initialization sequence, then the software (Ethernet driver) interface for transmitting and receiving frames.

Following the software initialization and operation sections are sections providing a detailed description of the functions of the FEC.

19.5.1 Buffer Descriptors

This section provides a description of the operation of the driver/DMA via the buffer descriptors. It is followed by a detailed description of the receive and transmit descriptor fields.

19.5.1.1 Driver/DMA Operation with Buffer Descriptors

The data for the FEC frames resides in one or more memory buffers external to the FEC. Associated with each buffer is a buffer descriptor (BD), which contains a starting address (32-bit aligned pointer), data length, and status/control information (which contains the current state for the buffer). To permit maximum user flexibility, the BDs are also located in external memory and are read by the FEC DMA engine.

Software produces buffers by allocating/initializing memory and initializing buffer descriptors. Setting the RxBD[E] or TxBD[R] bit produces the buffer. Software writing to TDAR or RDAR tells the FEC that a buffer is placed in external memory for the transmit or receive data traffic, respectively. The hardware reads the BDs and consumes the buffers after they have been produced. After the data DMA is complete and the DMA engine writes the buffer descriptor status bits, hardware clears RxBD[E] or TxBD[R] to signal the buffer has been consumed. Software may poll the BDs to detect when the buffers are consumed or may rely on the buffer/frame interrupts. The driver may process these buffers, and they can return to the free list.

The ECR[ETHER_EN] bit operates as a reset to the BD/DMA logic. When ECR[ETHER_EN] is cleared, the DMA engine BD pointers are reset to point to the starting transmit and receive BDs. The buffer descriptors are not initialized by hardware during reset. At least one transmit and receive buffer descriptor must be initialized by software before ECR[ETHER_EN] is set.

The buffer descriptors operate as two separate rings. ERDSR defines the starting address for receive BDs and ETDSR defines the starting address for transmit BDs. The wrap (W) bit defines the last buffer descriptor in each ring. When W is set, the next descriptor in the ring is at the location pointed to by ERDSR and ETDSR for the receive and transmit rings, respectively. Buffer descriptor rings must start on a 32-bit boundary; however, it is recommended they are made 128-bit aligned.

19.5.1.1.1 Driver/DMA Operation with Transmit BDs

Typically, a transmit frame is divided between multiple buffers. An example is to have an application payload in one buffer, TCP header in a second buffer, IP header in a third buffer, and Ethernet/IEEE 802.3 header in a fourth buffer. The Ethernet MAC does not prepend the Ethernet header (destination address, source address, length/type field(s)), so the driver must provide this in one of the transmit buffers. The

Ethernet MAC can append the Ethernet CRC to the frame. TxBD[TC], which must be set by the driver, determines whether the MAC or driver appends the CRC.

The driver (TxBD software producer) should set up Tx BDs so a complete transmit frame is given to the hardware at once. If a transmit frame consists of three buffers, the BDs should be initialized with pointer, length, and control (W, L, TC, ABC) and then the TxBD[R] bit should be set in reverse order (third, second, then first BD) to ensure that the complete frame is ready in memory before the DMA begins. If the TxBDs are set up in order, the DMA controller could DMA the first BD before the second was made available, potentially causing a transmit FIFO underrun.

In the FEC, the driver notifies the DMA that new transmit frame(s) are available by writing to TDAR. When this register is written to (data value is not significant) the FEC, RISC tells the DMA to read the next transmit BD in the ring. After started, the RISC + DMA continues to read and interpret transmit BDs in order and DMA the associated buffers until a transmit BD is encountered with the R bit cleared. At this point, the FEC polls this BD one more time. If the R bit is cleared the second time, RISC stops the transmit descriptor read process until software sets up another transmit frame and writes to TDAR.

When the DMA of each transmit buffer is complete, the DMA writes back to the BD to clear the R bit, indicating that the hardware consumer is finished with the buffer.

19.5.1.1.2 Driver/DMA Operation with Receive BDs

Unlike transmit, the length of the receive frame is unknown by the driver ahead of time. Therefore, the driver must set a variable to define the length of all receive buffers. In the FEC, this variable is written to the EMRBR register.

The driver (RxBD software producer) should set up some number of empty buffers for the Ethernet by initializing the address field and the E and W bits of the associated receive BDs. The hardware (receive DMA) consumes these buffers by filling them with data as frames are received and clearing the E bit and writing to the L bit (1 indicates last buffer in frame), the frame status bits (if L is set), and the length field.

If a receive frame spans multiple receive buffers, the L bit is only set for the last buffer in the frame. For non-last buffers, the length field in the receive BD is written by the DMA (at the same time the E bit is cleared) with the default receive buffer length value. For end-of-frame buffers, the receive BD is written with L set and information written to the status bits (M, BC, MC, LG, NO, CR, OV, TR). Some of the status bits are error indicators which, if set, indicate the receive frame should be discarded and not given to higher layers. The frame status/length information is written into the receive FIFO following the end of the frame (as a single 32-bit word) by the receive logic. The length field for the end of frame buffer is written with the length of the entire frame, not only the length of the last buffer.

For simplicity, the driver may assign a large enough default receive buffer length to contain an entire frame, keeping in mind that a malfunction on the network or out-of-spec implementation could result in giant frames. Frames of 2K (2048) bytes or larger are truncated by the FEC at 2047 bytes so software never sees a receive frame larger than 2047 bytes.

Similar to transmit, the FEC polls the receive descriptor ring after the driver sets up receive BDs and writes to the RDAR register. As frames are received, the FEC fills receive buffers and updates the associated BDs, then reads the next BD in the receive descriptor ring. If the FEC reads a receive BD and finds the E bit

cleared, it polls this BD once more. If RxBD[E] is clear a second time, FEC stops reading receive BDs until the driver writes to RDAR.

19.5.1.2 Ethernet Receive Buffer Descriptor (RxBD)

In the RxBD, the user initializes the E and W bits in the first longword and the pointer in the second longword. When the buffer has been DMA'd, the Ethernet controller modifies the E, L, M, BC, MC, LG, NO, CR, OV, and TR bits and writes the length of the used portion of the buffer in the first longword. The M, BC, MC, LG, NO, CR, OV, and TR bits in the first longword of the buffer descriptor are only modified by the Ethernet controller when the L bit is set.

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Offset + 0	E	RO1	W	RO2	L	—	—	M	BC	MC	LG	NO	—	CR	OV	TR
Offset + 2	Data Length															
Offset + 4	Rx Data Buffer Pointer - A[31:16]															
Offset + 6	Rx Data Buffer Pointer - A[15:0]															

Figure 19-25. Receive Buffer Descriptor (RxBD)

Table 19-29. Receive Buffer Descriptor Field Definitions

Word	Field	Description
Offset + 0	15 E	Empty. Written by the FEC (=0) and user (=1). 0 The data buffer associated with this BD is filled with received data, or data reception has aborted due to an error condition. The status and length fields have been updated as required. 1 The data buffer associated with this BD is empty, or reception is currently in progress.
Offset + 0	14 RO1	Receive software ownership. This field is reserved for use by software. This read/write bit is not modified by hardware, nor does its value affect hardware.
Offset + 0	13 W	Wrap. Written by user. 0 The next buffer descriptor is found in the consecutive location 1 The next buffer descriptor is found at the location defined in ERDSR.
Offset + 0	12 RO2	Receive software ownership. This field is reserved for use by software. This read/write bit is not modified by hardware, nor does its value affect hardware.
Offset + 0	11 L	Last in frame. Written by the FEC. 0 The buffer is not the last in a frame. 1 The buffer is the last in a frame.
Offset + 0	10–9	Reserved, must be cleared.
Offset + 0	8 M	Miss. Written by the FEC. This bit is set by the FEC for frames accepted in promiscuous mode, but flagged as a miss by the internal address recognition. Therefore, while in promiscuous mode, you can use the M-bit to quickly determine whether the frame was destined to this station. This bit is valid only if the L-bit is set and the PROM bit is set. 0 The frame was received because of an address recognition hit. 1 The frame was received because of promiscuous mode.
Offset + 0	7 BC	Set if the DA is broadcast (FFFF_FFFF_FFFF).

Table 19-29. Receive Buffer Descriptor Field Definitions (continued)

Word	Field	Description
Offset + 0	6 MC	Set if the DA is multicast and not BC.
Offset + 0	5 LG	Rx frame length violation. Written by the FEC. A frame length greater than RCR[MAX_FL] was recognized. This bit is valid only if the L-bit is set. The receive data is not altered in any way unless the length exceeds 2047 bytes.
Offset + 0	4 NO	Receive non-octet aligned frame. Written by the FEC. A frame that contained a number of bits not divisible by 8 was received, and the CRC check that occurred at the preceding byte boundary generated an error. This bit is valid only if the L-bit is set. If this bit is set, the CR bit is not set.
Offset + 0	3	Reserved, must be cleared.
Offset + 0	2 CR	Receive CRC error. Written by the FEC. This frame contains a CRC error and is an integral number of octets in length. This bit is valid only if the L-bit is set.
Offset + 0	1 OV	Overrun. Written by the FEC. A receive FIFO overrun occurred during frame reception. If this bit is set, the other status bits, M, LG, NO, CR, and CL lose their normal meaning and are zero. This bit is valid only if the L-bit is set.
Offset + 0	0 TR	Set if the receive frame is truncated (frame length > 2047 bytes). If the TR bit is set, the frame must be discarded and the other error bits must be ignored as they may be incorrect.
Offset + 2	15–0 Data Length	Data length. Written by the FEC. Data length is the number of octets written by the FEC into this BD's data buffer if L equals 0 (the value is equal to EMRBR), or the length of the frame including CRC if L is set. It is written by the FEC once as the BD is closed.
Offset + 4	15–0 A[31:16]	RX data buffer pointer, bits [31:16] ¹
Offset + 6	15–0 A[15:0]	RX data buffer pointer, bits [15:0]

¹ The receive buffer pointer, containing the address of the associated data buffer, must always be evenly divisible by 16. The buffer must reside in memory external to the FEC. The Ethernet controller never modifies this value.

NOTE

When the software driver sets an E bit in one or more receive descriptors, the driver should follow with a write to RDAR.

19.5.1.3 Ethernet Transmit Buffer Descriptor (TxBD)

Data is presented to the FEC for transmission by arranging it in buffers referenced by the channel's TxBDs. The Ethernet controller confirms transmission by clearing the ready bit (TxBD[R]) when DMA of the buffer is complete. In the TxBD, the user initializes the R, W, L, and TC bits and the length (in bytes) in the first longword and the buffer pointer in the second longword.

The FEC clears the R bit when the buffer is transferred. Status bits for the buffer/frame are not included in the transmit buffer descriptors. Transmit frame status is indicated via individual interrupt bits (error conditions) and in statistic counters in the MIB block. See [Section 19.4.1, “MIB Block Counters Memory Map,”](#) for more details.

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Offset + 0	R	TO1	W	TO2	L	TC	ABC	—	—	—	—	—	—	—	—	—
Offset + 2	Data Length															
Offset + 4	Tx Data Buffer Pointer - A[31:16]															
Offset + 6	Tx Data Buffer Pointer - A[15:0]															

Figure 19-26. Transmit Buffer Descriptor (TxBd)**Table 19-30. Transmit Buffer Descriptor Field Definitions**

Word	Field	Description
Offset + 0	15 R	Ready. Written by the FEC and you. 0 The data buffer associated with this BD is not ready for transmission. You are free to manipulate this BD or its associated data buffer. The FEC clears this bit after the buffer has been transmitted or after an error condition is encountered. 1 The data buffer, prepared for transmission by you, has not been transmitted or currently transmits. You may write no fields of this BD after this bit is set.
Offset + 0	14 TO1	Transmit software ownership. This field is reserved for software use. This read/write bit is not modified by hardware nor does its value affect hardware.
Offset + 0	13 W	Wrap. Written by user. 0 The next buffer descriptor is found in the consecutive location 1 The next buffer descriptor is found at the location defined in ETDSR.
Offset + 0	12 TO2	Transmit software ownership. This field is reserved for use by software. This read/write bit is not modified by hardware nor does its value affect hardware.
Offset + 0	11 L	Last in frame. Written by user. 0 The buffer is not the last in the transmit frame 1 The buffer is the last in the transmit frame
Offset + 0	10 TC	Transmit CRC. Written by user (only valid if L is set). 0 End transmission immediately after the last data byte 1 Transmit the CRC sequence after the last data byte
Offset + 0	9 ABC	Append bad CRC. Written by user (only valid if L is set). 0 No effect 1 Transmit the CRC sequence inverted after the last data byte (regardless of TC value)
Offset + 0	8–0	Reserved, must be cleared.
Offset + 2	15–0 Data Length	Data length, written by user. Data length is the number of octets the FEC should transmit from this BD's data buffer. It is never modified by the FEC.
Offset + 4	15–0 A[31:16]	Tx data buffer pointer, bits [31:16] ¹
Offset + 6	15–0 A[15:0]	Tx data buffer pointer, bits [15:0]

¹ The transmit buffer pointer, containing the address of the associated data buffer, must always be evenly divisible by 4. The buffer must reside in memory external to the FEC. This value is never modified by the Ethernet controller.

NOTE

After the software driver has set up the buffers for a frame, it should set up the corresponding BDs. The last step in setting up the BDs for a transmit frame is setting the R bit in the first BD for the frame. The driver must follow that with a write to TDAR that triggers the FEC to poll the next BD in the ring.

19.5.2 Initialization Sequence

This section describes which registers are reset due to hardware reset, which are reset by the FEC RISC, and what locations you must initialize prior to enabling the FEC.

19.5.2.1 Hardware Controlled Initialization

In the FEC, hardware resets registers and control logic that generate interrupts. A hardware reset negates output signals and resets general configuration bits.

Other registers reset when the ECR[ETHER_EN] bit is cleared (which is accomplished by a hard reset or software to halt operation). By clearing ECR[ETHER_EN], configuration control registers such as the TCR and RCR are not reset, but the entire data path is reset.

Table 19-31. ECR[ETHER_EN] De-Assertion Effect on FEC

Register/Machine	Reset Value
XMIT block	Transmission is aborted (bad CRC appended)
RECV block	Receive activity is aborted
DMA block	All DMA activity is terminated
RDAR	Cleared
TDAR	Cleared
Descriptor Controller block	Halt operation

19.5.3 User Initialization (Prior to Setting ECR[ETHER_EN])

You need to initialize portions the FEC prior to setting the ECR[ETHER_EN] bit. The exact values depend on the particular application. The sequence is not important.

[Table 19-32](#) defines Ethernet MAC registers requiring initialization.

Table 19-32. User Initialization (Before ECR[ETHER_EN])

Description
Initialize EIMR
Clear EIR (write 0xFFFF_FFFF)
TFWR (optional)
IALR / IAUR
GAUR / GALR

Table 19-32. User Initialization (Before ECR[ETHER_EN]) (continued)

Description
PALR / PAUR (only needed for full duplex flow control)
OPD (only needed for full duplex flow control)
RCR
TCR
MSCR (optional)
Clear MIB_RAM

Table 19-33 defines FEC FIFO/DMA registers that require initialization.

Table 19-33. FEC User Initialization (Before ECR[ETHER_EN])

Description
Initialize FRSR (optional)
Initialize EMRBR
Initialize ERDSR
Initialize ETDSR
Initialize (Empty) Transmit Descriptor ring
Initialize (Empty) Receive Descriptor ring

19.5.4 Microcontroller Initialization

In the FEC, the descriptor control RISC initializes some registers after ECR[ETHER_EN] is asserted. After the microcontroller initialization sequence is complete, hardware is ready for operation.

Table 19-34 shows microcontroller initialization operations.

Table 19-34. Microcontroller Initialization

Description
Initialize BackOff Random Number Seed
Activate Receiver
Activate Transmitter
Clear Transmit FIFO
Clear Receive FIFO
Initialize Transmit Ring Pointer
Initialize Receive Ring Pointer
Initialize FIFO Count Registers

19.5.5 User Initialization (After Setting ECR[ETHER_EN])

After setting ECR[ETHER_EN], you can set up the buffer/frame descriptors and write to TDAR and RDAR. Refer to [Section 19.5.1, “Buffer Descriptors,”](#) for more details.

19.5.6 Network Interface Options

The FEC supports an MII interface for 10/100 Mbps Ethernet and a 7-wire serial interface for 10 Mbps Ethernet. The RCR[MII_MODE] bit select the interface mode. In MII mode (RCR[MII_MODE] set), there are 18 signals defined by the IEEE 802.3 standard and supported by the EMAC. [Table 19-35](#) shows these signals.

Table 19-35. MII Mode

Signal Description	EMAC pin
Transmit Clock	FEC_TXCLK
Transmit Enable	FEC_TXEN
Transmit Data	FEC_TXD[3:0]
Transmit Error	FEC_TXER
Collision	FEC_COL
Carrier Sense	FEC_CRS
Receive Clock	FEC_RXCLK
Receive Data Valid	FEC_RXDV
Receive Data	FEC_RXD[3:0]
Receive Error	FEC_RXER
Management Data Clock	FEC_MDC
Management Data Input/Output	FEC_MDIO

The 7-wire serial mode interface (RCR[MII_MODE] cleared) is generally referred to as AMD mode. [Table 19-36](#) shows the 7-wire mode connections to the external transceiver.

Table 19-36. 7-Wire Mode Configuration

Signal description	EMAC Pin
Transmit Clock	FEC_TXCLK
Transmit Enable	FEC_TXEN
Transmit Data	FEC_TXD[0]
Collision	FEC_COL
Receive Clock	FEC_RXCLK

Table 19-36. 7-Wire Mode Configuration (continued)

Signal description	EMAC Pin
Receive Data Valid	FEC_RXDV
Receive Data	FEC_RXD[0]

19.5.7 FEC Frame Transmission

The Ethernet transmitter is designed to work with almost no intervention from software. After ECR[ETHER_EN] is set and data appears in the transmit FIFO, the Ethernet MAC can transmit onto the network. The Ethernet controller transmits bytes least significant bit (lsb) first.

When the transmit FIFO fills to the watermark (defined by TFWR), MAC transmit logic asserts FEC_TXEN and starts transmitting the preamble (PA) sequence, the start frame delimiter (SFD), and then the frame information from the FIFO. However, the controller defers the transmission if the network is busy (FEC_CRS is asserted). Before transmitting, the controller waits for carrier sense to become inactive, then determines if carrier sense stays inactive for 60 bit times. If so, transmission begins after waiting an additional 36 bit times (96 bit times after carrier sense originally became inactive). See [Section 19.5.15.1, “Transmission Errors,”](#) for more details.

If a collision occurs during transmission of the frame (half duplex mode), the Ethernet controller follows the specified backoff procedures and attempts to retransmit the frame until the retry limit is reached. The transmit FIFO stores at least the first 64 bytes of the transmit frame, so they do not have to be retrieved from system memory in case of a collision. This improves bus utilization and latency in case immediate retransmission is necessary.

When all the frame data is transmitted, FCS (frame check sequence) or 32-bit cyclic redundancy check (CRC) bytes are appended if the TC bit is set in the transmit frame control word. If the ABC bit is set in the transmit frame control word, a bad CRC is appended to the frame data regardless of the TC bit value. Following the transmission of the CRC, the Ethernet controller writes the frame status information to the MIB block. Transmit logic automatically pads short frames (if the TC bit in the transmit buffer descriptor for the end of frame buffer is set).

Settings in the EIMR determine interrupts generated to the buffer (TXB) and frame (TFINT).

The transmit error interrupts are HBERR, BABT, LATE_COL, COL_RETRY_LIM, and XFIFO_UN. If the transmit frame length exceeds MAX_FL bytes, BABT interrupt is asserted. However, the entire frame is transmitted (no truncation).

To pause transmission, set TCR[GTS] (graceful transmit stop). The FEC transmitter stops immediately if transmission is not in progress; otherwise, it continues transmission until the current frame finishes or terminates with a collision. After the transmitter has stopped, the GRA (graceful stop complete) interrupt is asserted. If TCR[GTS] is cleared, the FEC resumes transmission with the next frame.

19.5.7.1 Duplicate Frame Transmission

The FEC fetches transmit buffer descriptors (TxBDs) and the corresponding transmit data continuously until the transmit FIFO is full. It does not determine whether the TxBD to be fetched is already being

processed internally (as a result of a wrap). As the FEC nears the end of the transmission of one frame, it begins to DMA the data for the next frame. To remain one BD ahead of the DMA, it also fetches the TxBD for the next frame. It is possible that the FEC fetches from memory a BD that has already been processed but not yet written back (it is read a second time with the R bit remains set). In this case, the data is fetched and transmitted again.

Using at least three TxBDs fixes this problem for large frames, but not for small frames. To ensure correct operation for large or small frames, one of the following must be true:

- The FEC software driver ensures that there is always at least one TxBD with the ready bit cleared.
- Every frame uses more than one TxBD and every TxBD but the last is written back immediately after the data is fetched.
- The FEC software driver ensures a minimum frame size, n . The minimum number of TxBDs is then $(\text{Tx FIFO Size} \div (n + 4))$ rounded up to the nearest integer (though the result cannot be less than three). The default Tx FIFO size is 192 bytes; this size is programmable.

19.5.8 FEC Frame Reception

The FEC receiver works with almost no intervention from the host and can perform address recognition, CRC checking, short frame checking, and maximum frame length checking. The Ethernet controller receives serial data lsb first.

When the driver enables the FEC receiver by setting ECR[ETHER_EN], it immediately starts processing receive frames. When FEC_RXDV is asserted, the receiver first checks for a valid PA/SFD header. If the PA/SFD is valid, it is stripped and the receiver processes the frame. If a valid PA/SFD is not found, the frame is ignored.

In serial mode, the first 16 bit times of RX_D0 following assertion of FEC_RXDV are ignored. Following the first 16 bit times, the data sequence is checked for alternating 1/0s. If a 11 or 00 data sequence is detected during bit times 17 to 21, the remainder of the frame is ignored. After bit time 21, the data sequence is monitored for a valid SFD (11). If a 00 is detected, the frame is rejected. When a 11 is detected, the PA/SFD sequence is complete.

In MII mode, the receiver checks for at least one byte matching the SFD. Zero or more PA bytes may occur, but if a 00 bit sequence is detected prior to the SFD byte, the frame is ignored.

After the first 6 bytes of the frame are received, the FEC performs address recognition on the frame.

After a collision window (64 bytes) of data is received and if address recognition has not rejected the frame, the receive FIFO signals the frame is accepted and may be passed on to the DMA. If the frame is a runt (due to collision) or is rejected by address recognition, the receive FIFO is notified to reject the frame. Therefore, no collision fragments are presented to you except late collisions, which indicate serious LAN problems.

During reception, the Ethernet controller checks for various error conditions and after the entire frame is written into the FIFO, a 32-bit frame status word is written into the FIFO. This status word contains the M, BC, MC, LG, NO, CR, OV, and TR status bits, and the frame length. See [Section 19.5.15.2, “Reception Errors,”](#) for more details.

Receive buffer (RXB) and frame interrupts (RFINT) may be generated if enabled by the EIMR register. A receive error interrupt is a babbling receiver error (BABR). Receive frames are not truncated if they exceed the max frame length (MAX_FL); however, the BABR interrupt occurs and the LG bit in the receive buffer descriptor (RxBD) is set. See [Section 19.5.1.2, “Ethernet Receive Buffer Descriptor \(RxBD\),”](#) for more details.

When the receive frame is complete, the FEC sets the L-bit in the RxBD, writes the other frame status bits into the RxBD, and clears the E-bit. The Ethernet controller next generates a maskable interrupt (RFINT bit in EIR, maskable by RFIEN bit in EIMR), indicating that a frame is received and is in memory. The Ethernet controller then waits for a new frame.

19.5.9 Ethernet Address Recognition

The FEC filters the received frames based on destination address (DA) type — individual (unicast), group (multicast), or broadcast (all-ones group address). The difference between an individual address and a group address is determined by the I/G bit in the destination address field. A flowchart for address recognition on received frames appears in the figures below.

Address recognition is accomplished through the use of the receive block and microcode running on the microcontroller. The flowchart shown in [Figure 19-27](#) illustrates the address recognition decisions made by the receive block, while [Figure 19-28](#) illustrates the decisions made by the microcontroller.

If the DA is a broadcast address and broadcast reject (RCR[BC_REJ]) is cleared, then the frame is accepted unconditionally, as shown in [Figure 19-27](#). Otherwise, if the DA is not a broadcast address, then the microcontroller runs the address recognition subroutine, as shown in [Figure 19-28](#).

If the DA is a group (multicast) address and flow control is disabled, then the microcontroller performs a group hash table lookup using the 64-entry hash table programmed in GAUR and GALR. If a hash match occurs, the receiver accepts the frame.

If flow control is enabled, the microcontroller does an exact address match check between the DA and the designated PAUSE DA (01:80:C2:00:00:01). If the receive block determines the received frame is a valid PAUSE frame, the frame is rejected. The receiver detects a PAUSE frame with the DA field set to the designated PAUSE DA or the unicast physical address.

If the DA is the individual (unicast) address, the microcontroller performs an individual exact match comparison between the DA and 48-bit physical address that you program in the PALR and PAUR registers. If an exact match occurs, the frame is accepted; otherwise, the microcontroller does an individual hash table lookup using the 64-entry hash table programmed in registers, IAUR and IALR. In the case of an individual hash match, the frame is accepted. Again, the receiver accepts or rejects the frame based on PAUSE frame detection, shown in [Figure 19-27](#).

If neither a hash match (group or individual) nor an exact match (group or individual) occur, and if promiscuous mode is enabled (RCR[PROM] set), the frame is accepted and the MISS bit in the receive buffer descriptor is set; otherwise, the frame is rejected.

Similarly, if the DA is a broadcast address, broadcast reject (RCR[BC_REJ]) is asserted, and promiscuous mode is enabled, the frame is accepted and the MISS bit in the receive buffer descriptor is set; otherwise, the frame is rejected.

In general, when a frame is rejected, it is flushed from the FIFO.

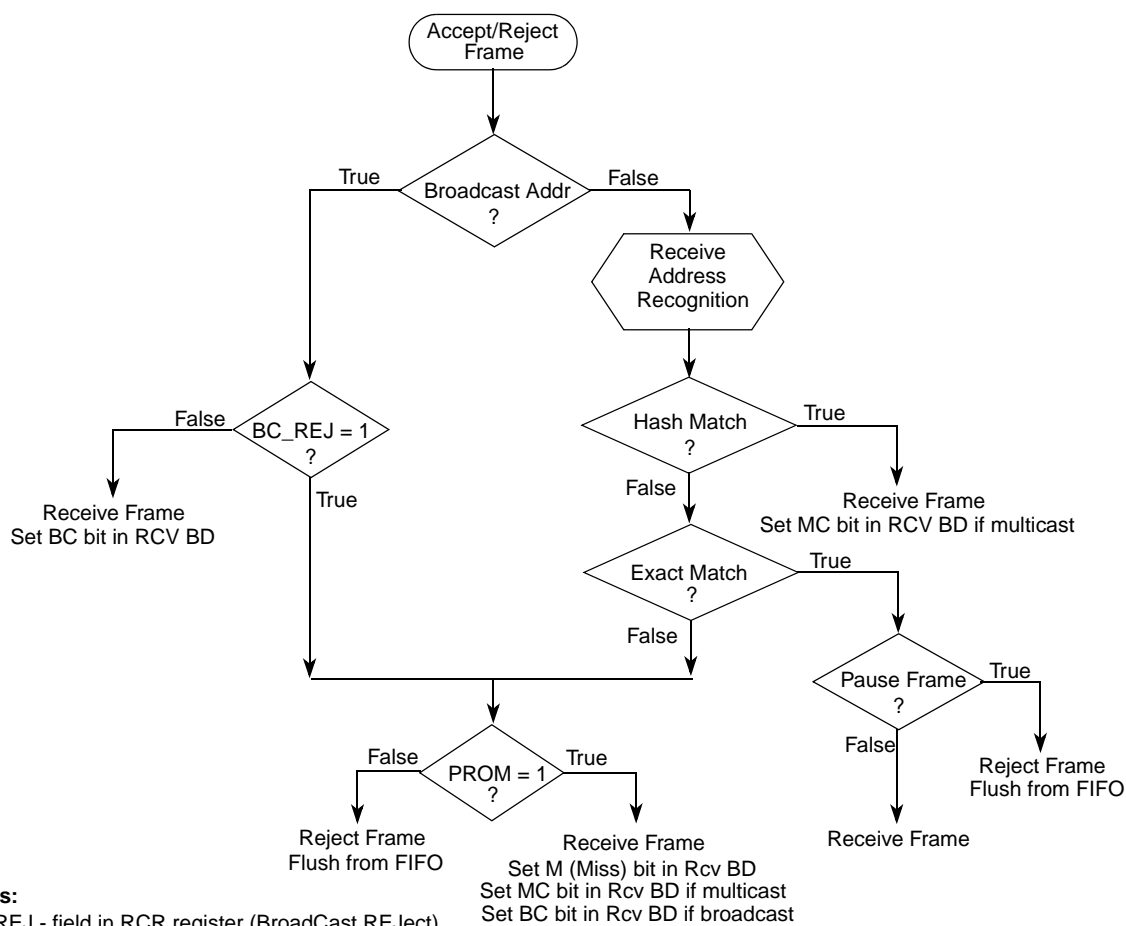
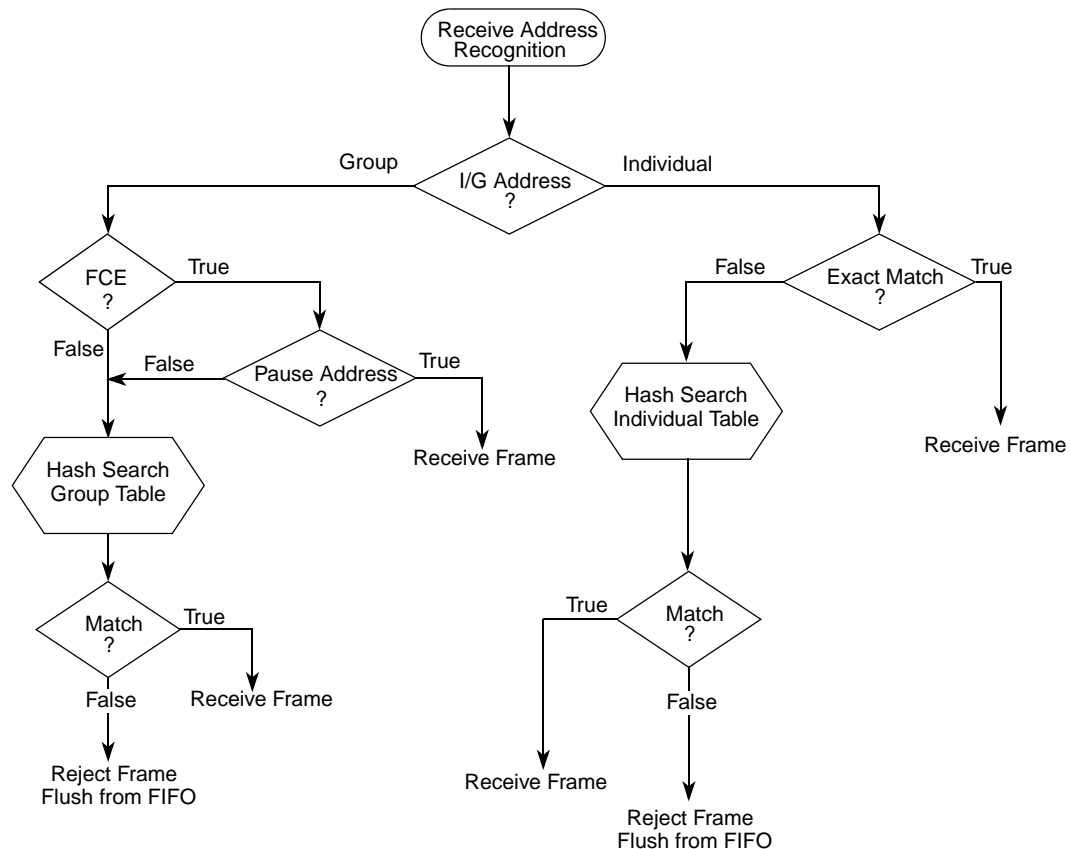


Figure 19-27. Ethernet Address Recognition—Receive Block Decisions

**Notes:**

FCE - field in RCR register (flow control enable)

I/G - Individual/Group bit in destination address (lsb in first byte received in MAC frame)

Figure 19-28. Ethernet Address Recognition—Microcode Decisions

19.5.10 Hash Algorithm

The hash table algorithm used in the group and individual hash filtering operates as follows. The 48-bit destination address is mapped into one of 64 bits, represented by 64 bits stored in GAUR, GALR (group address hash match), or IAUR, IALR (individual address hash match). This mapping is performed by passing the 48-bit address through the on-chip 32-bit CRC generator and selecting the six most significant bits of the CRC-encoded result to generate a number between 0 and 63. The msb of the CRC result selects GAUR (msb = 1) or GALR (msb = 0). The five least significant bits of the hash result select the bit within the selected register. If the CRC generator selects a bit set in the hash table, the frame is accepted; otherwise, it is rejected.

For example, if eight group addresses are stored in the hash table and random group addresses are received, the hash table prevents roughly 56/64 (87.5%) of the group address frames from reaching memory. Those that do reach memory must be further filtered by the processor to determine if they truly contain one of the eight desired addresses.

The effectiveness of the hash table declines as the number of addresses increases.

The user must initialize the hash table registers. Use this CRC32 polynomial to compute the hash:

$$X^{32} + X^{26} + X^{23} + X^{22} + X^{16} + X^{12} + X^{11} + X^{10} + X^8 + X^7 + X^5 + X^4 + X^2 + X + 1$$

Eqn. 19-2

Table 19-37 contains example destination addresses and corresponding hash values.

Table 19-37. Destination Address to 6-Bit Hash

48-bit DA	6-bit Hash (in hex)	Hash Decimal Value
65FF_FFFF_FFFF	0x0	0
55FF_FFFF_FFFF	0x1	1
15FF_FFFF_FFFF	0x2	2
35FF_FFFF_FFFF	0x3	3
B5FF_FFFF_FFFF	0x4	4
95FF_FFFF_FFFF	0x5	5
D5FF_FFFF_FFFF	0x6	6
F5FF_FFFF_FFFF	0x7	7
DBFF_FFFF_FFFF	0x8	8
FBFF_FFFF_FFFF	0x9	9
BBFF_FFFF_FFFF	0xA	10
8BFF_FFFF_FFFF	0xB	11
0BFF_FFFF_FFFF	0xC	12
3BFF_FFFF_FFFF	0xD	13
7BFF_FFFF_FFFF	0xE	14
5BFF_FFFF_FFFF	0xF	15
27FF_FFFF_FFFF	0x10	16
07FF_FFFF_FFFF	0x11	17
57FF_FFFF_FFFF	0x12	18
77FF_FFFF_FFFF	0x13	19
F7FF_FFFF_FFFF	0x14	20
C7FF_FFFF_FFFF	0x15	21
97FF_FFFF_FFFF	0x16	22
A7FF_FFFF_FFFF	0x17	23
99FF_FFFF_FFFF	0x18	24
B9FF_FFFF_FFFF	0x19	25
F9FF_FFFF_FFFF	0x1A	26
C9FF_FFFF_FFFF	0x1B	27

Table 19-37. Destination Address to 6-Bit Hash (continued)

48-bit DA	6-bit Hash (in hex)	Hash Decimal Value
59FF_FFFF_FFFF	0x1C	28
79FF_FFFF_FFFF	0x1D	29
29FF_FFFF_FFFF	0x1E	30
19FF_FFFF_FFFF	0x1F	31
D1FF_FFFF_FFFF	0x20	32
F1FF_FFFF_FFFF	0x21	33
B1FF_FFFF_FFFF	0x22	34
91FF_FFFF_FFFF	0x23	35
11FF_FFFF_FFFF	0x24	36
31FF_FFFF_FFFF	0x25	37
71FF_FFFF_FFFF	0x26	38
51FF_FFFF_FFFF	0x27	39
7FFF_FFFF_FFFF	0x28	40
4FFF_FFFF_FFFF	0x29	41
1FFF_FFFF_FFFF	0x2A	42
3FFF_FFFF_FFFF	0x2B	43
BFFF_FFFF_FFFF	0x2C	44
9FFF_FFFF_FFFF	0x2D	45
DFFF_FFFF_FFFF	0x2E	46
EFFF_FFFF_FFFF	0x2F	47
93FF_FFFF_FFFF	0x30	48
B3FF_FFFF_FFFF	0x31	49
F3FF_FFFF_FFFF	0x32	50
D3FF_FFFF_FFFF	0x33	51
53FF_FFFF_FFFF	0x34	52
73FF_FFFF_FFFF	0x35	53
23FF_FFFF_FFFF	0x36	54
13FF_FFFF_FFFF	0x37	55
3DFF_FFFF_FFFF	0x38	56
0DFF_FFFF_FFFF	0x39	57
5DFF_FFFF_FFFF	0x3A	58
7DFF_FFFF_FFFF	0x3B	59

Table 19-37. Destination Address to 6-Bit Hash (continued)

48-bit DA	6-bit Hash (in hex)	Hash Decimal Value
FDFF_FFFF_FFFF	0x3C	60
DDFF_FFFF_FFFF	0x3D	61
9DFF_FFFF_FFFF	0x3E	62
BDFF_FFFF_FFFF	0x3F	63

19.5.11 Full Duplex Flow Control

Full-duplex flow control allows you to transmit pause frames and to detect received pause frames. Upon detection of a pause frame, MAC data frame transmission stops for a given pause duration.

To enable PAUSE frame detection, the FEC must operate in full-duplex mode (TCR[FDEN] set) with flow control (RCR[FCE] set). The FEC detects a pause frame when the fields of the incoming frame match the pause frame specifications, as shown in [Table 19-38](#). In addition, the receive status associated with the frame should indicate that the frame is valid.

Table 19-38. PAUSE Frame Field Specification

48-bit Destination Address	0x0180_C200_0001 or Physical Address
48-bit Source Address	Any
16-bit Type	0x8808
16-bit Opcode	0x0001
16-bit PAUSE Duration	0x0000 – 0xFFFF

The receiver and microcontroller modules perform PAUSE frame detection. The microcontroller runs an address recognition subroutine to detect the specified pause frame destination address, while the receiver detects the type and opcode pause frame fields. On detection of a pause frame, TCR[GTS] is set by the FEC internally. When transmission has paused, the EIR[GRA] interrupt is asserted and the pause timer begins to increment. The pause timer uses the transmit backoff timer hardware for tracking the appropriate collision backoff time in half-duplex mode. The pause timer increments once every slot time, until OPD[PAUSE_DUR] slot times have expired. On OPD[PAUSE_DUR] expiration, TCR[GTS] is cleared allowing MAC data frame transmission to resume. The receive flow control pause status bit (TCR[RFC_PAUSE]) is set while the transmitter pauses due to reception of a pause frame.

To transmit a pause frame, the FEC must operate in full-duplex mode and you must set flow control pause (TCR[TFC_PAUSE]). After TCR[TFC_PAUSE] is set, the transmitter sets TCR[GTS] internally. When the transmission of data frames stops, the EIR[GRA] (graceful stop complete) interrupt asserts and the pause frame is transmitted. TCR[TFC_PAUSE,GTS] are then cleared internally.

You must specify the desired pause duration in the OPD register.

When the transmitter pauses due to receiver/microcontroller pause frame detection, TCR[TFC_PAUSE] may remain set and cause the transmission of a single pause frame. In this case, the EIR[GRA] interrupt is not asserted.

19.5.12 Inter-Packet Gap (IPG) Time

The minimum inter-packet gap time for back-to-back transmission is 96 bit times. After completing a transmission or after the backoff algorithm completes, the transmitter waits for carrier sense to be negated before starting its 96 bit time IPG counter. Frame transmission may begin 96 bit times after carrier sense is negated if it stays negated for at least 60 bit times. If carrier sense asserts during the last 36 bit times, it is ignored and a collision occurs.

The receiver accepts back-to-back frames with a minimum spacing of at least 28 bit times. If an inter-packet gap between receive frames is less than 28 bit times, the receiver may discard the following frame.

19.5.13 Collision Managing

If a collision occurs during frame transmission, the Ethernet controller continues the transmission for at least 32 bit times, transmitting a JAM pattern consisting of 32 ones. If the collision occurs during the preamble sequence, a JAM pattern is sent after the end of the preamble sequence.

If a collision occurs within 512 bit times (one slot time), the retry process is initiated. The transmitter waits a random number of slot times. If a collision occurs after 512 bit times, then no retransmission is performed and the end of frame buffer is closed with a Late Collision (LC) error indication.

19.5.14 MII Internal and External Loopback

Internal and external loopback are supported by the Ethernet controller. In loopback mode, both of the FIFOs are used and the FEC actually operates in a full-duplex fashion. Internal and external loopback are configured using combinations of the RCR[LOOP, DRT] and TCR[FDEN] bits.

Set FDEN for internal and external loopback.

For internal loopback, set RCR[LOOP] and clear RCR[DRT]. FEC_TXEN and FEC_TXER do not assert during internal loopback. During internal loopback, the transmit/receive data rate is higher than in normal operation because the transmit and receive blocks use the internal bus clock instead of the clocks from the external transceiver. This causes an increase in the required system bus bandwidth for transmit and receive data being DMA'd to/from external memory. It may be necessary to pace the frames on the transmit side and/or limit the size of the frames to prevent transmit FIFO underruns and receive FIFO overflows.

For external loopback, clear RCR[LOOP] and RCR[DRT], and configure the external transceiver for loopback.

19.5.15 Ethernet Error-Managing Procedure

The Ethernet controller reports frame reception and transmission error conditions using the MIB block counters, the FEC RxBDs, and the EIR register.

19.5.15.1 Transmission Errors

19.5.15.1.1 Transmitter Underrun

If this error occurs, the FEC sends 32 bits that ensure a CRC error and stops transmitting. All remaining buffers for that frame are then flushed and closed, and EIR[UN] is set. The FEC then continues to the next transmit buffer descriptor and begin transmitting the next frame. The UN interrupt is asserted if enabled in the EIMR register.

19.5.15.1.2 Retransmission Attempts Limit Expired

When this error occurs, the FEC terminates transmission. All remaining buffers for that frame are flushed and closed, and EIR[RL] is set. The FEC then continues to the next transmit buffer descriptor and begins transmitting the next frame. The RL interrupt is asserted if enabled in the EIMR register.

19.5.15.1.3 Late Collision

When a collision occurs after the slot time (512 bits starting at the Preamble), the FEC terminates transmission. All remaining buffers for that frame are flushed and closed, and EIR[LC] is set. The FEC then continues to the next transmit buffer descriptor and begin transmitting the next frame. The LC interrupt is asserted if enabled in the EIMR register.

19.5.15.1.4 Heartbeat

Some transceivers have a self-test feature called heartbeat or signal quality error. To signify a good self-test, the transceiver indicates a collision to the FEC within four microseconds after completion of a frame transmitted by the Ethernet controller. This indication of a collision does not imply a real collision error on the network, but is rather an indication that the transceiver continues to function properly. This is the heartbeat condition.

If TCR[HBC] is set and the heartbeat condition is not detected by the FEC after a frame transmission, a heartbeat error occurs. When this error occurs, the FEC closes the buffer, sets EIR[HB], and generates the HBERR interrupt if it is enabled.

19.5.15.2 Reception Errors

19.5.15.2.1 Overrun Error

If the receive block has data to put into the receive FIFO and the receive FIFO is full, FEC sets RxBD[OV]. All subsequent data in the frame is discarded and subsequent frames may also be discarded until the receive FIFO is serviced by the DMA and space is made available. At this point the receive frame/status word is written into the FIFO with the OV bit set. The driver must discard this frame.

19.5.15.2.2 Non-Octet Error (Dribbling Bits)

The Ethernet controller manages up to seven dribbling bits when the receive frame terminates past a non-octet aligned boundary. Dribbling bits are not used in the CRC calculation. If there is a CRC error, the frame non-octet aligned (NO) error is reported in the RxBD. If there is no CRC error, no error is reported.

19.5.15.2.3 CRC Error

When a CRC error occurs with no dribble bits, FEC closes the buffer and sets RxBD[CR]. CRC checking cannot be disabled, but the CRC error can be ignored if checking is not required.

19.5.15.2.4 Frame Length Violation

When the receive frame length exceeds MAX_FL bytes the BABR interrupt is generated, and RxBD[LG] is set. The frame is not truncated unless the frame length exceeds 2047 bytes.

19.5.15.2.5 Truncation

When the receive frame length exceeds 2047 bytes, frame is truncated and RxBD[TR] is set.

Chapter 20

Watchdog Timer Module

20.1 Introduction

The watchdog timer (WDT) is a 16-bit timer used to help software recover from runaway code. The watchdog timer has a free-running down-counter (watchdog counter) that generates a reset on underflow. To prevent a reset, software must periodically restart the countdown by servicing the watchdog.

20.1.1 Low-Power Mode Operation

This subsection describes the operation of the watchdog module in low-power modes and halted mode of operation (by issuing a HALT instruction). Low-power modes are described in [Chapter 8, “Power Management.”](#) [Table 20-1](#) shows the watchdog module operation in the low-power modes, and shows how this module may facilitate exit from each mode.

Table 20-1. Watchdog Module Operation in Low-power Modes

Low-power Mode	Watchdog Operation	Mode Exit
Wait	Normal if WCR[WAIT] cleared, stopped otherwise	Upon Watchdog reset
Doze	Normal if WCR[DOZE] cleared, stopped otherwise	Upon Watchdog reset
Stop	Stopped	No, only via external interrupts

In wait mode, with the watchdog control register’s WAIT bit (WCR[WAIT]) set, watchdog timer operation stops. In wait mode with the WCR[WAIT] bit cleared, the watchdog timer continues to operate normally. In doze mode with the WCR[DOZE] bit set, the watchdog timer module operation stops. In doze mode with the WCR[DOZE] bit cleared, the watchdog timer continues to operate normally. Watchdog timer operation stops in stop mode. When stop mode is exited, the watchdog timer continues to operate in its pre-stop mode state.

In halted mode (entered by issuing a HALT instruction or asserting $\overline{\text{BKPT}}$) with the WCR[HALTED] bit set, watchdog timer module operation stops. When halted mode is exited, watchdog timer operation continues from the state it was in before entering halted mode, but any updates made in halted mode remain. If the WCR[HALTED] bit is cleared, the watchdog timer continues to operate normally after executing a HALT instruction. This is a debug feature available for the user

20.1.2 Block Diagram

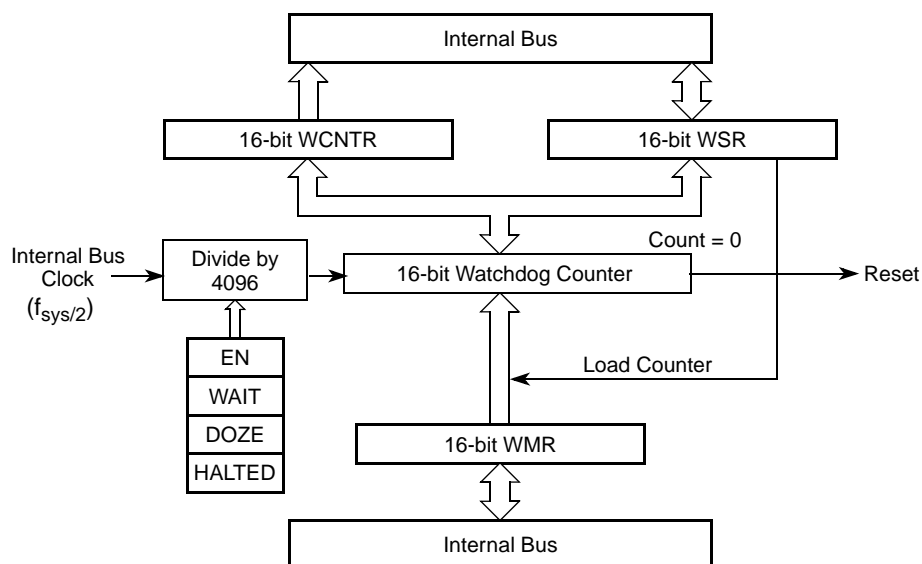


Figure 20-1. Watchdog Timer Block Diagram

20.2 Memory Map/Register Definition

This subsection describes the memory map and registers for the watchdog timer. Refer to [Table 20-2](#) for an overview of the watchdog memory map.

NOTE

Longword accesses to any of the watchdog timer registers result in a bus error. Only byte and word accesses are allowed.

Table 20-2. Watchdog Timer Module Memory Map

Address ¹	Register	Width (bits)	Access	Reset Value	Section/Page
Supervisor Only Access					
0xFC08_C000	Watchdog Control Register (WCR)	16	R/W	0x000F	20.2.1/20-3
0xFC08_C002	Watchdog Modulus Register (WMR)	16	R/W	0xFFFF	20.2.2/20-4
Supervisor/User Access					
0xFC08_C004	Watchdog Count Register (WCNTR)	16	R	0xFFFF	20.2.3/20-4
0xFC08_C006	Watchdog Service Register (WSR)	16	R/W	0x0000	20.2.4/20-5

¹ Addresses not assigned to a register and undefined register bits are reserved for expansion. Write accesses to these reserved address spaces and reserved register bits have no effect.

20.2.1 Watchdog Control Register (WCR)

The 16-bit WCR configures watchdog timer operation.

Address: 0xFC08_C000

Access: Supervisor read/write

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	0	0	0	0	0	0	0	0	0	0	0	0	WAIT	DOZE	HALTED	EN
W																
Reset	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1

Figure 20-2. Watchdog Control Register (WCR)

Table 20-3. WCR Field Descriptions

Field	Description
15–4	Reserved, should be cleared.
3 WAIT	Wait mode bit. Controls the function of the watchdog timer in wait mode. After written, the WAIT bit is not affected by further writes except in halted mode. Reset sets WAIT. 0 Watchdog timer not affected in wait mode 1 Watchdog timer stopped in wait mode
2 DOZE	Doze mode bit. Controls the function of the watchdog timer in doze mode. After written, the DOZE bit is not affected by further writes except in halted mode. Reset sets DOZE. 0 Watchdog timer not affected in doze mode 1 Watchdog timer stopped in doze mode
1 HALTED	Halted mode bit. Controls the function of the watchdog timer in halted/debug mode. After written, the HALTED bit is not affected by further writes except in halted mode. During halted mode, watchdog timer registers can be written and read normally. When halted mode is exited, timer operation continues from the state it was in before entering halted mode, but any updates made in halted mode remain. If a write-once register is written for the first time in halted mode, the register remains writable when halted mode is exited. 0 Watchdog timer not affected in halted mode 1 Watchdog timer stopped in halted mode Note: Changing the HALTED bit from 1 to 0 during halted mode starts the watchdog timer. Changing the HALTED bit from 0 to 1 during halted mode stops the watchdog timer.
0 EN	Watchdog enable bit. Enables the watchdog timer. After written, the EN bit is not affected by further writes except in halted mode. When the watchdog timer is disabled, the watchdog counter and prescaler counter are held in a stopped state. After disabled, the watchdog cannot be re-enabled. 0 Watchdog timer disabled 1 Watchdog timer enabled

20.2.2 Watchdog Modulus Register (WMR)

The WMR register determines the timer modulus reload value.

Address: 0xFC08_C002

Access: Supervisor
read/write

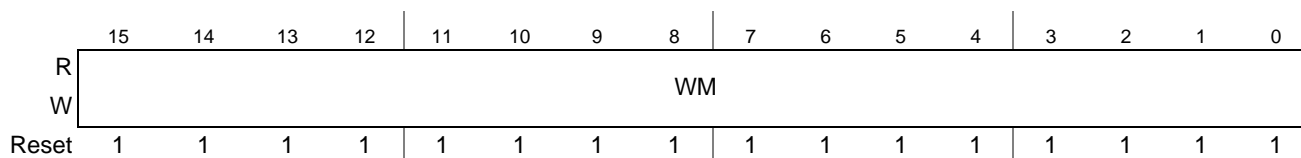


Figure 20-3. Watchdog Modulus Register (WMR)

Table 20-4. WMR Field Descriptions

Field	Description
15–0 WM	Watchdog modulus. Contains the modulus that is reloaded into the watchdog counter by a service sequence. After written, the WM[15:0] field is not affected by further writes except in halted mode. Writing to WMR immediately loads the new modulus value into the watchdog counter. The new value is also used at the next and all subsequent reloads. Reading WMR returns the value in the modulus register. Reset initializes the WM[15:0] field to 0xFFFF. Note: The prescaler counter is reset anytime a new value is loaded into the watchdog counter and also during reset.

20.2.3 Watchdog Count Register (WCNTR)

The WCNTR register provides visibility to the watchdog counter value. The timeout value for the watchdog timer is determined from the following equation:

$$\text{WDT timeout} = \frac{4096 \times \text{WCNTR}}{f_{\text{sys}/2}} \quad \text{Eqn. 20-1}$$

Thus, the maximum timeout is $4096 \times 2^{16} / f_{\text{sys}/2} = 3.22$ seconds at 83.3 MHz internal bus frequency.

Address: 0xFC08_C004

Access: User read/write

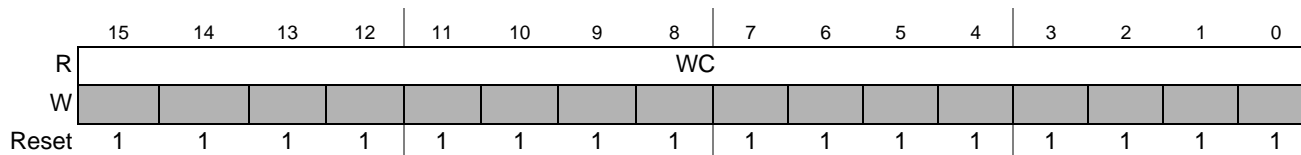


Figure 20-4. Watchdog Count Register (WCNTR)

Table 20-5. WCNTR Field Descriptions

Field	Description
15–0 WC	Watchdog count field. Reflects the current value in the watchdog counter. Reading the 16-bit WCNTR with two 8-bit reads is not guaranteed to return a coherent value. Writing to WCNTR has no effect, and write cycles are terminated normally.

20.2.4 Watchdog Service Register (WSR)

When the watchdog timer is enabled, writing 0x5555 and then 0xAAAA to WSR before the watchdog counter times out prevents a reset. If WSR is not serviced before the timeout, the watchdog timer sends a signal to the reset controller module that sets the RSR[WDR] bit and asserts a system reset.

Both writes must occur in the order listed before the timeout, but any number of instructions can be executed between the two writes. However, writing any value other than 0x5555 or 0xAAAA to WSR resets the servicing sequence, requiring both values to be written to keep the watchdog timer from causing a reset.

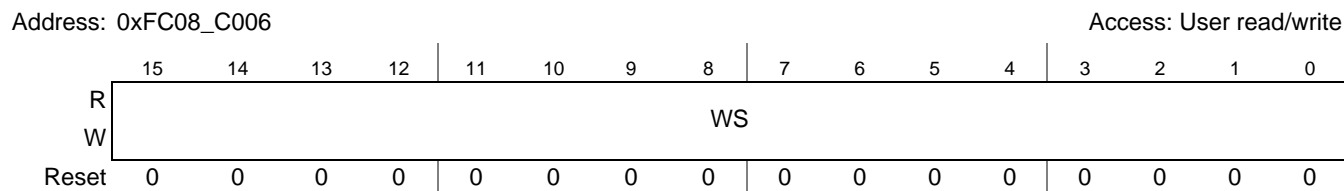


Figure 20-5. Watchdog Service Register (WSR)

Chapter 21

Programmable Interrupt Timers (PIT0–PIT1)

21.1 Introduction

This chapter describes the operation of the two programmable interrupt timer modules: PIT0–PIT1.

21.1.1 Overview

Each PIT is a 16-bit timer that provides precise interrupts at regular intervals with minimal processor intervention. The timer can count down from the value written in the modulus register or it can be a free-running down-counter.

21.1.2 Block Diagram

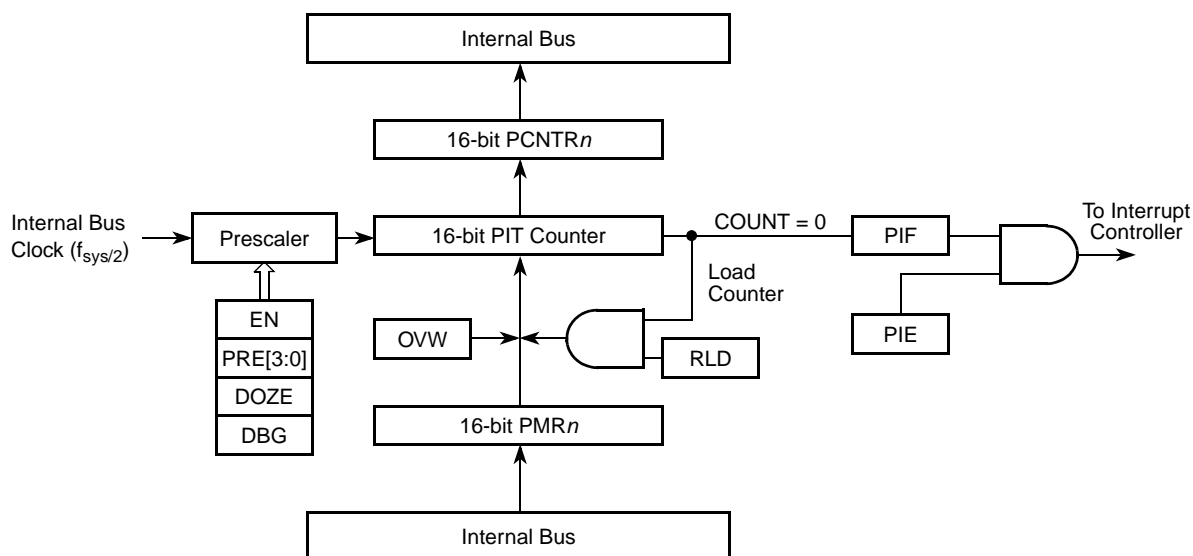


Figure 21-1. PIT Block Diagram

21.1.3 Low-Power Mode Operation

This subsection describes the operation of the PIT modules in low-power modes and debug mode of operation. Low-power modes are described in the power management module, [Chapter 8, “Power Management.”](#) Table 21-1 shows the PIT module operation in low-power modes and how it can exit from each mode.

NOTE

The low-power interrupt control register (LPICR) in the system control module specifies the interrupt level at or above which the device can be brought out of a low-power mode.

Table 21-1. PIT Module Operation in Low-power Modes

Low-power Mode	PIT Operation	Mode Exit
Wait	Normal	N/A
Doze	Normal if PCSR _n [DOZE] cleared, stopped otherwise	Any interrupt at or above level in LPICR, exit doze mode if PCSR _n [DOZE] is set. Otherwise interrupt assertion has no effect.
Stop	Stopped	No
Debug	Normal if PCSR _n [DBG] cleared, stopped otherwise	No. Any interrupt is serviced upon normal exit from debug mode

In wait mode, the PIT module continues to operate as in run mode and can be configured to exit the low-power mode by generating an interrupt request. In doze mode with the PCSR_n[DOZE] bit set, PIT module operation stops. In doze mode with the PCSR_n[DOZE] bit cleared, doze mode does not affect PIT operation. When doze mode is exited, PIT continues operating in the state it was in prior to doze mode. In stop mode, the internal bus clock is absent and PIT module operation stops.

In debug mode with the PCSR_n[DBG] bit set, PIT module operation stops. In debug mode with the PCSR_n[DBG] bit cleared, debug mode does not affect PIT operation. When debug mode is exited, the PIT continues to operate in its pre-debug mode state, but any updates made in debug mode remain.

21.2 Memory Map/Register Definition

This section contains a memory map (see [Table 21-2](#)) and describes the register structure for PIT0–PIT1.

NOTE

Longword accesses to any of the programmable interrupt timer registers results in a bus error. Only byte and word accesses are allowed.

Table 21-2. Programmable Interrupt Timer Modules Memory Map

Address	Register	Width (bits)	Access ¹	Reset Value	Section/Page
PIT 0 PIT 1					
Supervisor Access Only Registers²					
0xFC08_0000 0xFC08_4000	PIT Control and Status Register (PCSR _n)	16	R/W	0x0000	21.2.1/21-3
0xFC08_0002 0xFC08_4002	PIT Modulus Register (PMR _n)	16	R/W	0xFFFF	21.2.2/21-4

Table 21-2. Programmable Interrupt Timer Modules Memory Map (continued)

Address	Register	Width (bits)	Access ¹	Reset Value	Section/Page
PIT 0 PIT 1					
User/Supervisor Access Registers					
0xFC08_0004 0xFC08_4004	PIT Count Register (PCNTR _n)	16	R	0xFFFF	21.2.3/21-5

¹ Accesses to reserved address locations have no effect and result in a cycle termination transfer error.

² User mode accesses to supervisor only addresses have no effect and result in a cycle termination transfer error.

21.2.1 PIT Control and Status Register (PCSR_n)

The PCSR_n registers configure the corresponding timer's operation.

Address: 0xFC08_0000 (PCSR0)
0xFC08_4000 (PCSR1)

Access: Supervisor
read/write

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	0	0	0	0	PRE				0	DOZE	DBG	OVW	PIE	PIF	RLD	EN
W														w1c		
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

 Figure 21-2. PCSR_n Register

 Table 21-3. PCSR_n Field Descriptions

Field	Description																								
15–12	Reserved, must be cleared.																								
11–8 PRE	<p>Prescaler. The read/write prescaler bits select the internal bus clock divisor to generate the PIT clock. To accurately predict the timing of the next count, change the PRE[3:0] bits only when the enable bit (EN) is clear. Changing PRE[3:0] resets the prescaler counter. System reset and the loading of a new value into the counter also reset the prescaler counter. Setting the EN bit and writing to PRE[3:0] can be done in this same write cycle. Clearing the EN bit stops the prescaler counter.</p> <table><tr><th>PRE</th><th>Internal Bus Clock Divisor</th><th>Decimal Equivalent</th></tr><tr><td>0000</td><td>2^0</td><td>1</td></tr><tr><td>0001</td><td>2^1</td><td>2</td></tr><tr><td>0010</td><td>2^2</td><td>4</td></tr><tr><td>...</td><td>...</td><td>...</td></tr><tr><td>1101</td><td>2^{13}</td><td>8192</td></tr><tr><td>1110</td><td>2^{14}</td><td>16384</td></tr><tr><td>1111</td><td>2^{15}</td><td>32768</td></tr></table>	PRE	Internal Bus Clock Divisor	Decimal Equivalent	0000	2^0	1	0001	2^1	2	0010	2^2	4	1101	2^{13}	8192	1110	2^{14}	16384	1111	2^{15}	32768
PRE	Internal Bus Clock Divisor	Decimal Equivalent																							
0000	2^0	1																							
0001	2^1	2																							
0010	2^2	4																							
...																							
1101	2^{13}	8192																							
1110	2^{14}	16384																							
1111	2^{15}	32768																							

Table 21-3. PCSR_n Field Descriptions (continued)

Field	Description
7	Reserved, must be cleared.
6 DOZE	Doze Mode Bit. The read/write DOZE bit controls the function of the PIT in doze mode. Reset clears DOZE. 0 PIT function not affected in doze mode 1 PIT function stopped in doze mode. When doze mode is exited, timer operation continues from the state it was in before entering doze mode.
5 DBG	Debug mode bit. Controls the function of PIT in halted/debug mode. Reset clears DBG. During debug mode, register read and write accesses function normally. When debug mode is exited, timer operation continues from the state it was in before entering debug mode, but any updates made in debug mode remain. 0 PIT function not affected in debug mode 1 PIT function stopped in debug mode Note: Changing the DBG bit from 1 to 0 during debug mode starts the PIT timer. Likewise, changing the DBG bit from 0 to 1 during debug mode stops the PIT timer.
4 OVW	Overwrite. Enables writing to PMR _n to immediately overwrite the value in the PIT counter. 0 Value in PMR _n replaces value in PIT counter when count reaches 0x0000. 1 Writing PMR _n immediately replaces value in PIT counter.
3 PIE	PIT interrupt enable. This read/write bit enables PIF flag to generate interrupt requests. 0 PIF interrupt requests disabled 1 PIF interrupt requests enabled
2 PIF	PIT interrupt flag. This read/write bit is set when PIT counter reaches 0x0000. Clear PIF by writing a 1 to it or by writing to PMR. Writing 0 has no effect. Reset clears PIF. 0 PIT count has not reached 0x0000. 1 PIT count has reached 0x0000.
1 RLD	Reload bit. The read/write reload bit enables loading the value of PMR _n into PIT counter when the count reaches 0x0000. 0 Counter rolls over to 0xFFFF on count of 0x0000 1 Counter reloaded from PMR _n on count of 0x0000
0 EN	PIT enable bit. Enables PIT operation. When PIT is disabled, counter and prescaler are held in a stopped state. This bit is read anytime, write anytime. 0 PIT disabled 1 PIT enabled

21.2.2 PIT Modulus Register (PMR_n)

The 16-bit read/write PMR_n contains the timer modulus value loaded into the PIT counter when the count reaches 0x0000 and the PCSR_n[RLD] bit is set.

When the PCSR_n[OVW] bit is set, PMR_n is transparent, and the value written to PMR_n is immediately loaded into the PIT counter. The prescaler counter is reset (0xFFFF) anytime a new value is loaded into the PIT counter and also during reset. Reading the PMR_n returns the value written in the modulus latch. Reset initializes PMR_n to 0xFFFF.

Address: 0xFC08_0002 (PMR0)
0xFC08_4002 (PMR1)

Access: Supervisor
read/write

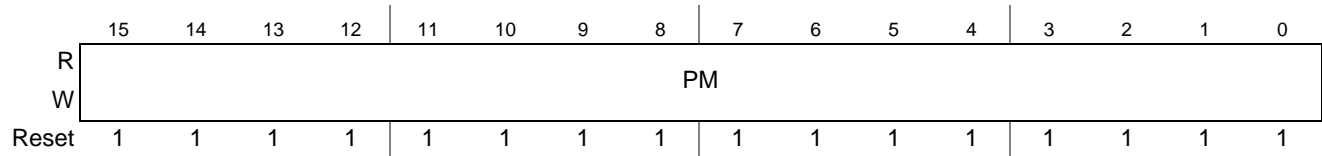


Figure 21-3. PIT Modulus Register (PMR n)

Table 21-4. PMR n Field Descriptions

Field	Description
15–0 PM	Timer modulus. The value of this register is loaded into the PIT counter when the count reaches zero and the PCSR n [RLD] bit is set. However, if PCSR n [OVW] is set, the value written to this field is immediately loaded into the counter. Reading this field returns the value written.

21.2.3 PIT Count Register (PCNTR n)

The 16-bit, read-only PCNTR n contains the counter value. Reading the 16-bit counter with two 8-bit reads is not guaranteed coherent. Writing to PCNTR n has no effect, and write cycles are terminated normally.

Address: 0xFC08_0004 (PCNTR0)
0xFC08_4004 (PCNTR1)

Access: User read only



Figure 21-4. PIT Count Register (PCNTR n)

Table 21-5. PCNTR n Field Descriptions

Field	Description
15–0 PC	Counter value. Reading this field with two 8-bit reads is not guaranteed coherent. Writing to PCNTR n has no effect, and write cycles are terminated normally.

21.3 Functional Description

This section describes the PIT functional operation.

21.3.1 Set-and-Forget Timer Operation

This mode of operation is selected when the RLD bit in the PCSR register is set.

When PIT counter reaches a count of 0x0000, PIF flag is set in PCSR n . The value in the modulus register loads into the counter, and the counter begins decrementing toward 0x0000. If the PCSR n [PIE] bit is set, the PIF flag issues an interrupt request to the CPU.

When the $PCSR_n[OVW]$ bit is set, the counter can be directly initialized by writing to PMR_n without having to wait for the count to reach 0x0000.

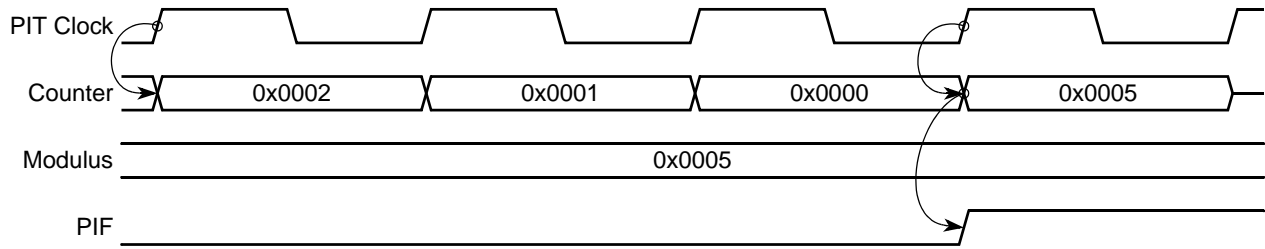


Figure 21-5. Counter Reloading from the Modulus Latch

21.3.2 Free-Running Timer Operation

This mode of operation is selected when the $PCSR_n[RLD]$ bit is clear. In this mode, the counter rolls over from 0x0000 to 0xFFFF without reloading from the modulus latch and continues to decrement.

When the counter reaches a count of 0x0000, $PCSR_n[PIF]$ flag is set. If the $PCSR_n[PIE]$ bit is set, PIF flag issues an interrupt request to the CPU.

When the $PCSR_n[OVW]$ bit is set, counter can be directly initialized by writing to PMR_n without having to wait for the count to reach 0x0000.

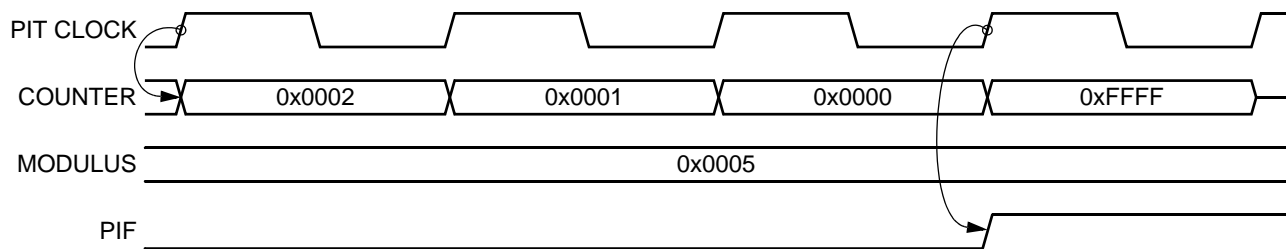


Figure 21-6. Counter in Free-Running Mode

21.3.3 Timeout Specifications

The 16-bit PIT counter and prescaler supports different timeout periods. The prescaler divides the internal bus clock period as selected by the $PCSR_n[PRE]$ bits. The $PMR_n[PM]$ bits select the timeout period.

$$\text{Timeout period} = \frac{2^{PCSR_n[PRE]} \times (PMR_n[PM] + 1)}{f_{sys/2}} \quad \text{Eqn. 21-1}$$

21.3.4 Interrupt Operation

Table 21-6 shows the interrupt request generated by the PIT.

Table 21-6. PIT Interrupt Requests

Interrupt Request	Flag	Enable Bit
Timeout	PIF	PIE

The PIF flag is set when the PIT counter reaches 0x0000. The PIE bit enables the PIF flag to generate interrupt requests. Clear PIF by writing a 1 to it or by writing to the PMR.

Chapter 22

DMA Timers (DTIM0–DTIM3)

22.1 Introduction

This chapter describes the configuration and operation of the four direct memory access (DMA) timer modules (DTIM0, DTIM1, DTIM2, and DTIM3). These 32-bit timers provide input capture and reference compare capabilities with optional signaling of events using interrupts or DMA triggers. Additionally, programming examples are included.

NOTE

The designation *n* appears throughout this section to refer to registers or signals associated with one of the four identical timer modules: DTIM0, DTIM1, DTIM2, or DTIM3.

22.1.1 Overview

Each DMA timer module has a separate register set for configuration and control. The timers can be configured to operate from the internal bus clock or from an external clocking source using the DT n IN signal. If the internal bus clock is selected, it can be divided by 16 or 1. The selected clock source is routed to an 8-bit programmable prescaler that clocks the actual DMA timer counter register (DTCN n). Using the DTMR n , DTXMR n , DTCR n , and DTRR n registers, the DMA timer may be configured to assert an output signal, generate an interrupt, or request a DMA transfer on a particular event.

NOTE

The GPIO module must be configured to enable the peripheral function of the appropriate pins (refer to [Chapter 13, “General Purpose I/O Module”](#)) prior to configuring the DMA Timers.

Figure 22-1 is a block diagram of one of the four identical timer modules.

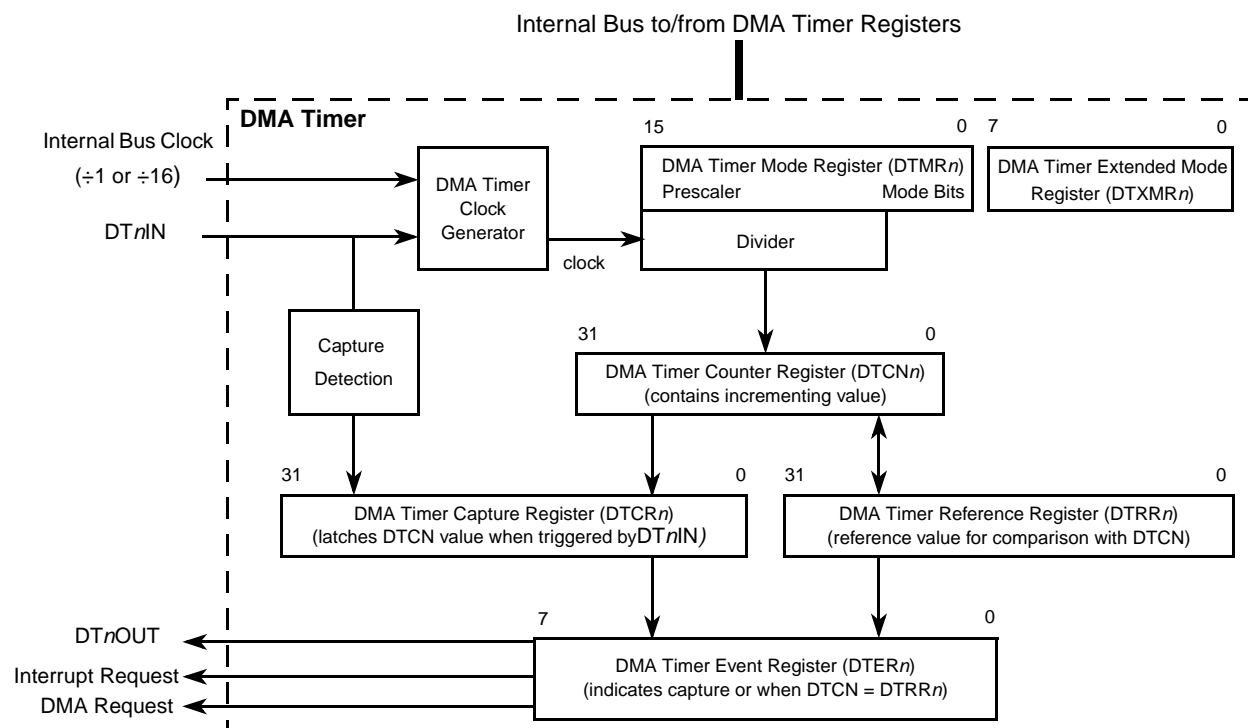


Figure 22-1. DMA Timer Block Diagram

22.1.2 Features

Each DMA timer module has:

- Maximum timeout period of 211,106 seconds at 83.33 MHz (~58 hours)
- 12-ns resolution at 83.33 MHz
- Programmable sources for the clock input, including external clock
- Programmable prescaler
- Input-capture capability with programmable trigger edge on input pin
- Programmable mode for the output pin on reference compare
- Free run and restart modes
- Programmable interrupt or DMA request on input capture or reference-compare

22.2 Memory Map/Register Definition

The timer module registers, shown in [Table 22-1](#), can be modified at any time.

Table 22-1. DMA Timer Module Memory Map

Address	Register	Width (bits)	Access	Reset Value	Section/Page
DMA Timer 0 DMA Timer 1 DMA Timer 2 DMA Timer 3					
0xFC07_0000 0xFC07_4000 0xFC07_8000 0xFC07_C000	DMA Timer <i>n</i> Mode Register (DTMR <i>n</i>)	16	R/W	0x0000	22.2.1/22-3
0xFC07_0002 0xFC07_4002 0xFC07_8002 0xFC07_C002	DMA Timer <i>n</i> Extended Mode Register (DTXMR <i>n</i>)	8	R/W	0x00	22.2.2/22-4
0xFC07_0003 0xFC07_4003 0xFC07_8003 0xFC07_C003	DMA Timer <i>n</i> Event Register (DTER <i>n</i>)	8	R/W	0x00	22.2.3/22-5
0xFC07_0004 0xFC07_4004 0xFC07_8004 0xFC07_C004	DMA Timer <i>n</i> Reference Register (DTRR <i>n</i>)	32	R/W	0xFFFF_FFFF	22.2.4/22-6
0xFC07_0008 0xFC07_4008 0xFC07_8008 0xFC07_C008	DMA Timer <i>n</i> Capture Register (DTCR <i>n</i>)	32	R/W	0x0000_0000	22.2.5/22-7
0xFC07_000C 0xFC07_400C 0xFC07_800C 0xFC07_C00C	DMA Timer <i>n</i> Counter Register (DTCN <i>n</i>)	32	R	0x0000_0000	22.2.6/22-8

22.2.1 DMA Timer Mode Registers (DTMR*n*)

DTMRs, shown in [Figure 22-2](#), program the prescaler and various timer modes.

Address: 0xFC07_0000 (DTMR0)
 0xFC07_4000 (DTMR1)
 0xFC07_8000 (DTMR2)
 0xFC07_C000 (DTMR3)

Access: User read/write

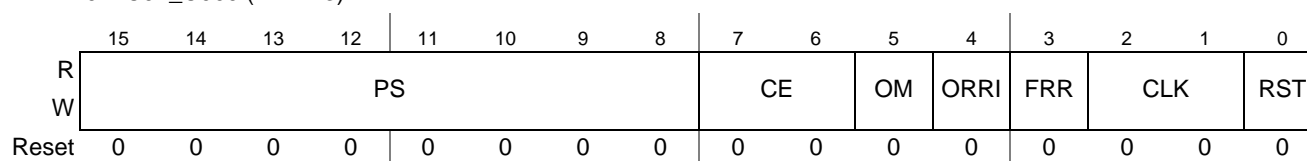


Figure 22-2. DTMR*n* Registers

Table 22-2. DTMR n Field Descriptions

Field	Description
15–8 PS	Prescaler value. Divides the clock input (internal bus clock/(16 or 1) or clock on DT n IN). 0x00 1 ... 0xFF 256
7–6 CE	Capture edge. 00 Disable capture event output 01 Capture on rising edge only 10 Capture on falling edge only 11 Capture on any edge
5 OM	Output mode. 0 Active-low pulse for one internal bus clock cycle (12-ns resolution at 83.33 MHz). 1 Toggle output.
4 ORRI	Output reference request, interrupt enable. If ORRI is set when DTER n [REF] is set, a DMA request or an interrupt occurs, depending on the value of DTXMR n [DMAEN] (DMA request if set, interrupt if cleared). 0 Disable DMA request or interrupt for reference reached (does not affect DMA request or interrupt on capture function). 1 Enable DMA request or interrupt upon reaching the reference value.
3 FRR	Free run/restart 0 Free run. Timer count continues incrementing after reaching the reference value. 1 Restart. Timer count is reset immediately after reaching the reference value.
2–1 CLK	Input clock source for the timer. Avoid setting CLK when RST is already set. Doing so causes CLK to zero (stop counting). 00 Stop count 01 Internal bus clock divided by 1 10 Internal bus clock divided by 16. This clock source is not synchronized with the timer; therefore, successive time-outs may vary slightly. 11 DT n IN pin (falling edge)
0 RST	Reset timer. Performs a software timer reset similar to an external reset, although other register values can be written while RST is cleared. A transition of RST from 1 to 0 resets register values. The timer counter is not clocked unless the timer is enabled. 0 Reset timer (software reset) 1 Enable timer

22.2.2 DMA Timer Extended Mode Registers (DTXMR n)

The DTXMR n register programs DMA request and increment modes for the timers.

Address: 0xFC07_0002 (DTXMR0)
0xFC07_4002 (DTXMR1)
0xFC07_8002 (DTXMR2)
0xFC07_C002 (DTXMR3)

Access: User read/write

	7	6	5	4	3	2	1	0
R	DMAEN	0	0	0	0	0	0	MODE16
W								

Figure 22-3. DTXMR n Registers

Table 22-3. DTXMR n Field Descriptions

Field	Description
7 DMAEN	DMA request. Enables DMA request output on counter reference match or capture edge event. 0 DMA request disabled 1 DMA request enabled
6–1	Reserved, must be cleared.
0 MODE16	Selects the increment mode for the timer. Setting MODE16 is intended to exercise the upper bits of the 32-bit timer in diagnostic software without requiring the timer to count through its entire dynamic range. When set, the counter's upper 16 bits mirror its lower 16 bits. All 32 bits of the counter remain compared to the reference value. 0 Increment timer by 1 1 Increment timer by 65,537

22.2.3 DMA Timer Event Registers (DTER n)

DTER n , shown in Figure 22-4, reports capture or reference events by setting DTER n [CAP] or DTER n [REF]. This reporting happens regardless of the corresponding DMA request or interrupt enable values, DTXMR n [DMAEN] and DTMR n [ORRI,CE].

Writing a 1 to DTER n [REF] or DTER n [CAP] clears it (writing a 0 does not affect bit value); both bits can be cleared at the same time. If configured to generate an interrupt request, clear REF and CAP early in the interrupt service routine so the timer module can negate the interrupt request signal to the interrupt controller. If configured to generate a DMA request, processing of the DMA data transfer automatically clears the REF and CAP flags via the internal DMA ACK signal.

Address: 0xFC07_0003 (DTER0)
 0xFC07_4003 (DTER1)
 0xFC07_8003 (DTER2)
 0xFC07_C003 (DTER3)

Access: User read/write

	7	6	5	4	3	2	1	0
R	0	0	0	0	0	0	REF	CAP
W							w1c	w1c
Reset:	0	0	0	0	0	0	0	0

Figure 22-4. DTER n Registers

Table 22-4. DTER n Field Descriptions

Field	Description																																								
7–2	Reserved, must be cleared.																																								
1 REF	Output reference event. The counter value (DTCN <i>n</i>) equals DTRR <i>n</i> . Writing a 1 to REF clears the event condition. Writing a 0 has no effect. <table><tr><th>REF</th><th>DTMR<i>n</i>[ORRI]</th><th>DTXMR<i>n</i>[DMAEN]</th><th></th></tr><tr><td>0</td><td>X</td><td>X</td><td>No event</td></tr><tr><td>1</td><td>0</td><td>0</td><td>No request asserted</td></tr><tr><td>1</td><td>0</td><td>1</td><td>No request asserted</td></tr><tr><td>1</td><td>1</td><td>0</td><td>Interrupt request asserted</td></tr><tr><td>1</td><td>1</td><td>1</td><td>DMA request asserted</td></tr></table>	REF	DTMR <i>n</i> [ORRI]	DTXMR <i>n</i> [DMAEN]		0	X	X	No event	1	0	0	No request asserted	1	0	1	No request asserted	1	1	0	Interrupt request asserted	1	1	1	DMA request asserted																
REF	DTMR <i>n</i> [ORRI]	DTXMR <i>n</i> [DMAEN]																																							
0	X	X	No event																																						
1	0	0	No request asserted																																						
1	0	1	No request asserted																																						
1	1	0	Interrupt request asserted																																						
1	1	1	DMA request asserted																																						
0 CAP	Capture event. The counter value has been latched into DTCR <i>n</i> . Writing a 1 to CAP clears the event condition. Writing a 0 has no effect. <table><tr><th>CAP</th><th>DTMR<i>n</i>[CE]</th><th>DTXMR<i>n</i>[DMAEN]</th><th></th></tr><tr><td>0</td><td>XX</td><td>X</td><td>No event</td></tr><tr><td>1</td><td>00</td><td>0</td><td>Disable capture event output</td></tr><tr><td>1</td><td>00</td><td>1</td><td>Disable capture event output</td></tr><tr><td>1</td><td>01</td><td>0</td><td>Capture on rising edge and trigger interrupt</td></tr><tr><td>1</td><td>01</td><td>1</td><td>Capture on rising edge and trigger DMA</td></tr><tr><td>1</td><td>10</td><td>0</td><td>Capture on falling edge and trigger interrupt</td></tr><tr><td>1</td><td>10</td><td>1</td><td>Capture on falling edge and trigger DMA</td></tr><tr><td>1</td><td>11</td><td>0</td><td>Capture on any edge and trigger interrupt</td></tr><tr><td>1</td><td>11</td><td>1</td><td>Capture on any edge and trigger DMA</td></tr></table>	CAP	DTMR <i>n</i> [CE]	DTXMR <i>n</i> [DMAEN]		0	XX	X	No event	1	00	0	Disable capture event output	1	00	1	Disable capture event output	1	01	0	Capture on rising edge and trigger interrupt	1	01	1	Capture on rising edge and trigger DMA	1	10	0	Capture on falling edge and trigger interrupt	1	10	1	Capture on falling edge and trigger DMA	1	11	0	Capture on any edge and trigger interrupt	1	11	1	Capture on any edge and trigger DMA
CAP	DTMR <i>n</i> [CE]	DTXMR <i>n</i> [DMAEN]																																							
0	XX	X	No event																																						
1	00	0	Disable capture event output																																						
1	00	1	Disable capture event output																																						
1	01	0	Capture on rising edge and trigger interrupt																																						
1	01	1	Capture on rising edge and trigger DMA																																						
1	10	0	Capture on falling edge and trigger interrupt																																						
1	10	1	Capture on falling edge and trigger DMA																																						
1	11	0	Capture on any edge and trigger interrupt																																						
1	11	1	Capture on any edge and trigger DMA																																						

22.2.4 DMA Timer Reference Registers (DTRR n)

As part of the output-compare function, each DTRR n contains the reference value compared with the respective free-running timer counter (DTCN n).

The reference value is matched when DTCN n equals DTRR n . The prescaler indicates that DTCN n should be incremented again. Therefore, the reference register is matched after DTRR n + 1 time intervals.

Address: 0xFC07_0004 (DTRR0)
 0xFC07_4004 (DTRR1)
 0xFC07_8004 (DTRR2)
 0xFC07_C004 (DTRR3)

Access: User read/write

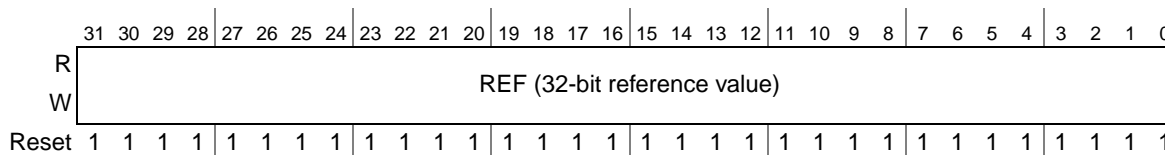


Figure 22-5. DTRR n Registers

Table 22-5. DTRR n Field Descriptions

Field	Description
31–0 REF	Reference value compared with the respective free-running timer counter (DTCN n) as part of the output-compare function.

22.2.5 DMA Timer Capture Registers (DTCR n)

Each DTCR n latches the corresponding DTCN n value during a capture operation when an edge occurs on DT n IN, as programmed in DTMR n . The internal bus clock is assumed to be the clock source. DT n IN cannot simultaneously function as a clocking source and as an input capture pin. Indeterminate operation results if DT n IN is set as the clock source when the input capture mode is used.

Address: 0xFC07_0008 (DTCR0)
 0xFC07_4008 (DTCR1)
 0xFC07_8008 (DTCR2)
 0xFC07_C008 (DTCR3)

Access: User read-only

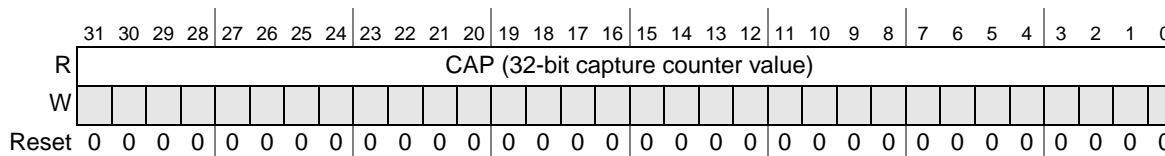


Figure 22-6. DTCR n Registers

Table 22-6. DTCR n Field Descriptions

Field	Description
31–0 CAP	Captures the corresponding DTCN n value during a capture operation when an edge occurs on DT n IN, as programmed in DTMR n .

22.2.6 DMA Timer Counters (DTCN n)

The current value of the 32-bit timer counter can be read at anytime without affecting counting. Writes to DTCN n clear the timer counter. The timer counter increments on the clock source rising edge (internal bus clock divided by 1, internal bus clock divided by 16, or DT n IN).

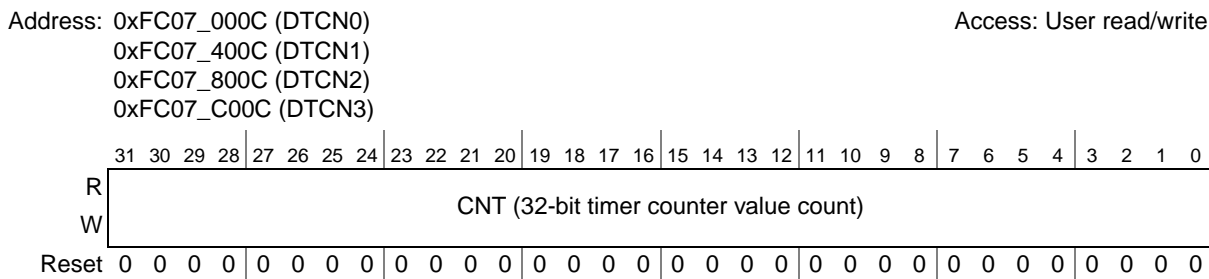


Figure 22-7. DMA Timer Counters (DTCN n)

Table 22-7. DTCN n Field Descriptions

Field	Description
31–0 CNT	Timer counter. Can be read at anytime without affecting counting and any write to this field clears it.

22.3 Functional Description

22.3.1 Prescaler

The prescaler clock input is selected from the internal bus clock ($f_{\text{sys}}/2$ divided by 1 or 16) or from the corresponding timer input, DT n IN. DT n IN is synchronized to the internal bus clock, and the synchronization delay is between two and three internal bus clocks. The corresponding DTMR n [CLK] selects the clock input source. A programmable prescaler divides the clock input by values from 1 to 256. The prescaler output is an input to the 32-bit counter, DTCN n .

22.3.2 Capture Mode

Each DMA timer has a 32-bit timer capture register (DTCR n) that latches the counter value when the corresponding input capture edge detector senses a defined DT n IN transition. The capture edge bits (DTMR n [CE]) select the type of transition that triggers the capture and sets the timer event register capture event bit, DTER n [CAP]. If DTER n [CAP] and DTXMR n [DMAEN] are set, a DMA request is asserted. If DTER n [CAP] is set and DTXMR n [DMAEN] is cleared, an interrupt is asserted.

22.3.3 Reference Compare

Each DMA timer can be configured to count up to a reference value, at which point DTER n [REF] is set. If DTMR n [ORRI] is set and DTXMR n [DMAEN] is cleared, an interrupt is asserted. If DTMR n [ORRI] and DTXMR n [DMAEN] are set, a DMA request is asserted. If the free run/restart bit DTMR n [FRR] is set, a new count starts. If it is clear, the timer keeps running.

22.3.4 Output Mode

When a timer reaches the reference value selected by DTRR, it can send an output signal on DT n OUT. DT n OUT can be an active-low pulse or a toggle of the current output, as selected by the DTMR n [OM] bit.

22.3.5 IEEE 1588 Support

The DMA timers on this device can use the Ethernet assembly's IEEE-1588 timebase count value as its clock source. This feature supports triggering events via processor interrupts or DMA requests based on network time values.

22.4 Initialization/Application Information

The general-purpose timer modules typically, but not necessarily, follow this program order:

- The DTMR n and DTXMR n registers are configured for the desired function and behavior.
 - Count and compare to a reference value stored in the DTRR n register
 - Capture the timer value on an edge detected on DT n IN
 - Configure DT n OUT output mode
 - Increment counter by 1 or by 65,537 (16-bit mode)
 - Enable/disable interrupt or DMA request on counter reference match or capture edge
- The DTMR n [CLK] register is configured to select the clock source to be routed to the prescaler.
 - Internal bus clock (can be divided by 1 or 16)
 - DT n IN, the maximum value of DT n IN is 1/5 of the internal bus clock, as described in the device's electrical characteristics

NOTE

DT n IN may not be configured as a clock source when the timer capture mode is selected or indeterminate operation results.

- The 8-bit DTMR n [PS] prescaler value is set.
- Using DTMR n [RST], counter is cleared and started.
- Timer events are managed with an interrupt service routine, a DMA request, or by a software polling mechanism.

22.4.1 Code Example

The following code provides an example of how to initialize and use DMA Timer0 for counting time-out periods.

```
DTMR0 EQU 0xFC07_0000 ;Timer0 mode register
DTMR1 EQU 0xFC07_4000 ;Timer1 mode register
DTRR0 EQU 0xFC07_0004 ;Timer0 reference register
DTRR1 EQU 0xFC07_4004 ;Timer1 reference register
DTCR0 EQU 0xFC07_0008 ;Timer0 capture register
DTCR1 EQU 0xFC07_4008 ;Timer1 capture register
DTCN0 EQU 0xFC07_000C ;Timer0 counter register
```

```

DTCN1 EQU 0xFC07_400C ;Timer1 counter register
DTER0 EQU 0xFC07_0003 ;Timer0 event register
DTER1 EQU 0xFC07_4003 ;Timer1 event register
* TMR0 is defined as: *
*[PS] = 0xFF,      divide clock by 256
*[CE] = 00         disable capture event output
*[OM] = 0          output=active-low pulse
*[ORRI] = 0,       disable ref. match output
*[FRR] = 1,        restart mode enabled
*[CLK] = 10,       internal bus clock/16
*[RST] = 0,        timer0 disabled

        move.w #0xFF0C,D0
        move.w D0,TMR0

        move.l #0x0000,D0;writing to the timer counter with any
        move.l D0,TCN0 ;value resets it to zero

        move.l #0xAFAF,D0 ;set the timer0 reference to be
        move.l #D0,TRR0 ;defined as 0xAFAF

```

The simple example below uses Timer0 to count time-out loops. A time-out occurs when the reference value, 0xAFAF, is reached.

```

timer0_ex
        clr.l D0
        clr.l D1
        clr.l D2

        move.l #0x0000,D0
        move.l D0,TCN0           ;reset the counter to 0x0000
        move.b #0x03,D0         ;writing ones to TER0[REF,CAP]
        move.b D0,TER0          ;clears the event flags
        move.w TMR0,D0          ;save the contents of TMR0 while setting
        bset #0,D0              ;the 0 bit. This enables timer 0 and starts counting
        move.w D0,TMR0          ;load the value back into the register, setting TMR0[RST]

T0_LOOP
        move.b TER0,D1          ;load TER0 and see if
        btst #1,D1              ;TER0[REF] has been set
        beq T0_LOOP

        addi.l #1,D2             ;Increment D2
        cmp.l #5,D2             ;Did D2 reach 5? (i.e. timer ref has timed)
        beq T0_FINISH          ;If so, end timer0 example. Otherwise jump back.
        move.b #0x02,D0         ;writing one to TER0[REF] clears the event flag
        move.b D0,TER0
        jmp T0_LOOP

T0_FINISH
        HALT                    ;End processing. Example is finished

```

22.4.2 Calculating Time-Out Values

Equation 22-1 determines time-out periods for various reference values:

$$\text{Timeout period} = (1/\text{clock frequency}) \times (1 \text{ or } 16) \times (\text{DTMR}_n[\text{PS}] + 1) \times (\text{DTRR}_n[\text{REF}] + 1) \quad \text{Eqn. 22-1}$$

When calculating time-out periods, add 1 to the prescaler to simplify calculating, because $\text{DTMR}_n[\text{PS}]$ equals 0x00 yields a prescaler of 1, and $\text{DTMR}_n[\text{PS}]$ equals 0xFF yields a prescaler of 256.

For example, if a 83.33-MHz timer clock is divided by 16, DTMR n [PS] equals 0x7F, and the timer is referenced at 0x13DC3 (81,347 decimal), the time-out period is:

$$\text{Timeout period} = \frac{1}{83.3 \times 10^6} \times 16 \times (127 + 1) \times (81347 + 1) = 2.00 \text{ s} \quad \textbf{Eqn. 22-2}$$

Chapter 23

Queued Serial Peripheral Interface (QSPI)

23.1 Introduction

This chapter describes the queued serial peripheral interface (QSPI) module.

23.1.1 Block Diagram

Figure 23-1 illustrates the QSPI module.

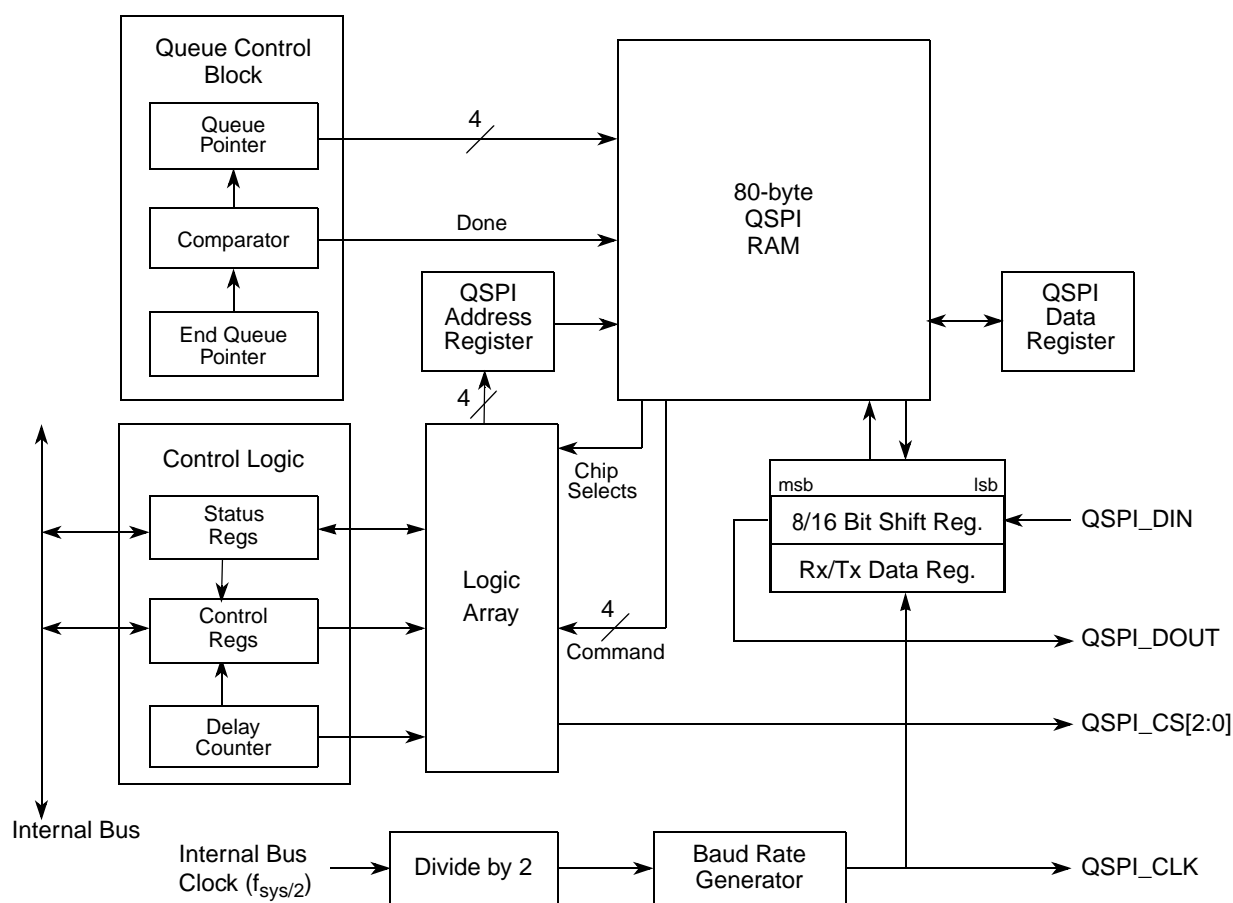


Figure 23-1. QSPI Block Diagram

23.1.2 Overview

The queued serial peripheral interface module provides a serial peripheral interface with queued transfer capability. It allows users to queue up to 16 transfers at once, eliminating CPU intervention between transfers. Transfer RAM in the QSPI is indirectly accessible using address and data registers.

NOTE

The GPIO module must be configured to enable the peripheral function of the appropriate pins (refer to [Chapter 13, “General Purpose I/O Module”](#)) prior to configuring the QSPI module.

23.1.3 Features

Features include:

- Programmable queue to support up to 16 transfers without user intervention
 - 80 bytes of data storage provided
- Supports transfer sizes of 8 to 16 bits in 1-bit increments
- Three peripheral chip-select lines for control of up to 7 devices (All chip selects may not be available on all devices. See [Chapter 2, “Signal Descriptions,”](#) for details on which chip-selects are pinned-out.)
- Baud rates from 163.39 Kbps to 20.83 Mbps at 83.33 MHz internal bus frequency
- Programmable delays before and after transfers
- Programmable QSPI clock phase and polarity
- Supports wraparound mode for continuous transfers

23.1.4 Modes of Operation

Because the QSPI module only operates in master mode, the master bit in the QSPI mode register (QMR[MSTR]) must be set for the QSPI to function properly. If the master bit is not set, QSPI activity is indeterminate. The QSPI can initiate serial transfers but cannot respond to transfers initiated by other QSPI masters.

23.2 External Signal Description

The module provides access to as many as 7 devices with a total of six signals: QSPI_DOUT, QSPI_DIN, QSPI_CLK, QSPI_CS[2:0].

Peripheral chip-select signals, QSPI_CS n , are used to select an external device as the source or destination for serial data transfer. Signals are asserted when a command in the queue is executed. More than one chip-select signal can be asserted simultaneously.

Although QSPI_CS n signals function as simple chip selects in most applications, up to 7 devices can be selected by decoding them with an external 3-to-8 decoder.

Table 23-1. QSPI Input and Output Signals and Functions

Signal Name	Hi-Z or Actively Driven	Function
Data output (QSPI_DOUT)	Configurable	Serial data output from QSPI
Data input (QSPI_DIN)	N/A	Serial data input to QSPI
Serial clock (QSPI_CLK)	Actively driven	Clock output from QSPI
Peripheral chip selects (QSPI_CS _n)	Actively driven	Peripheral selects from QSPI

23.3 Memory Map/Register Definition

Table 23-2 is the QSPI register memory map. Reading reserved locations returns zeros.

Table 23-2. QSPI Memory Map

Address ¹	Register	Width (bits)	Access	Reset Value	Section/Page
0xFC05_C000	QSPI Mode Register (QMR)	16	R/W	0x0104	23.3.1/23-3
0xFC05_C004	QSPI Delay Register (QDLYR)	16	R/W	0x0404	23.3.2/23-5
0xFC05_C008	QSPI Wrap Register (QWR)	16	R/W ²	0x0000	23.3.3/23-6
0xFC05_C00C	QSPI Interrupt Register (QIR)	16	R/W ²	0x0000	23.3.4/23-6
0xFC05_C010	QSPI Address Register (QAR)	16	R/W ²	0x0000	23.3.5/23-7
0xFC05_C014	QSPI Data Register (QDR)	16	R/W	0x0000	23.3.6/23-8

¹ Addresses not assigned to a register and undefined register bits are reserved for expansion.

² See the register description for special cases. Some bits may be read- or write-only.

23.3.1 QSPI Mode Register (QMR)

The QMR, shown in Figure 23-2, determines the basic operating modes of the QSPI module. Parameters such as QSPI_CLK polarity and phase, baud rate, master mode operation, and transfer size are determined by this register.

NOTE

Because the QSPI does not operate in slave mode, the master mode enable bit (QMR[MSTR]) must be set for the QSPI module to operate correctly.

Address: 0xFC05_C000 (QMR)

Access: User read/write

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	MSTR	0	BITS				CPOL	CPHA	BAUD							
W																
Reset	0	0	0	0	0	0	0	1	0	0	0	0	0	1	0	0

Figure 23-2. QSPI Mode Register (QMR)

Table 23-3. QMR Field Descriptions

Field	Description																						
15 MSTR	Master mode enable. 0 Reserved, do not use. 1 The QSPI is in master mode. Must be set for the QSPI module to operate correctly.																						
14	Reserved, must be cleared.																						
13–10 BITS	Transfer size. Determines the number of bits to be transferred for each entry in the queue. <table border="1"> <thead> <tr> <th>BITS</th><th>Bits per Transfer</th></tr> </thead> <tbody> <tr> <td>0000</td><td>16</td></tr> <tr> <td>0001–0111</td><td>Reserved</td></tr> <tr> <td>1000</td><td>8</td></tr> <tr> <td>1001</td><td>9</td></tr> <tr> <td>1010</td><td>10</td></tr> <tr> <td>1011</td><td>11</td></tr> <tr> <td>1100</td><td>12</td></tr> <tr> <td>1101</td><td>13</td></tr> <tr> <td>1110</td><td>14</td></tr> <tr> <td>1111</td><td>15</td></tr> </tbody> </table>	BITS	Bits per Transfer	0000	16	0001–0111	Reserved	1000	8	1001	9	1010	10	1011	11	1100	12	1101	13	1110	14	1111	15
BITS	Bits per Transfer																						
0000	16																						
0001–0111	Reserved																						
1000	8																						
1001	9																						
1010	10																						
1011	11																						
1100	12																						
1101	13																						
1110	14																						
1111	15																						
9 CPOL	Clock polarity. Defines the clock polarity of QSPI_CLK. 0 The inactive state value of QSPI_CLK is logic level 0. 1 The inactive state value of QSPI_CLK is logic level 1.																						
8 CPHA	Clock phase. Defines the QSPI_CLK clock-phase. 0 Data captured on the leading edge of QSPI_CLK and changed on the following edge of QSPI_CLK. 1 Data changed on the leading edge of QSPI_CLK and captured on the following edge of QSPI_CLK.																						
7–0 BAUD	Baud rate divider. The baud rate is selected by writing a value in the range 2–255. A value of zero disables the QSPI. A value of 1 is an invalid setting. The desired QSPI_CLK baud rate is related to the internal bus clock and QMR[BAUD] by the following expression: $\text{QMR[BAUD]} = f_{\text{sys}/2} / (2 \times [\text{desired QSPI_CLK baud rate}])$																						

Figure 23-3 shows an example of a QSPI clocking and data transfer.

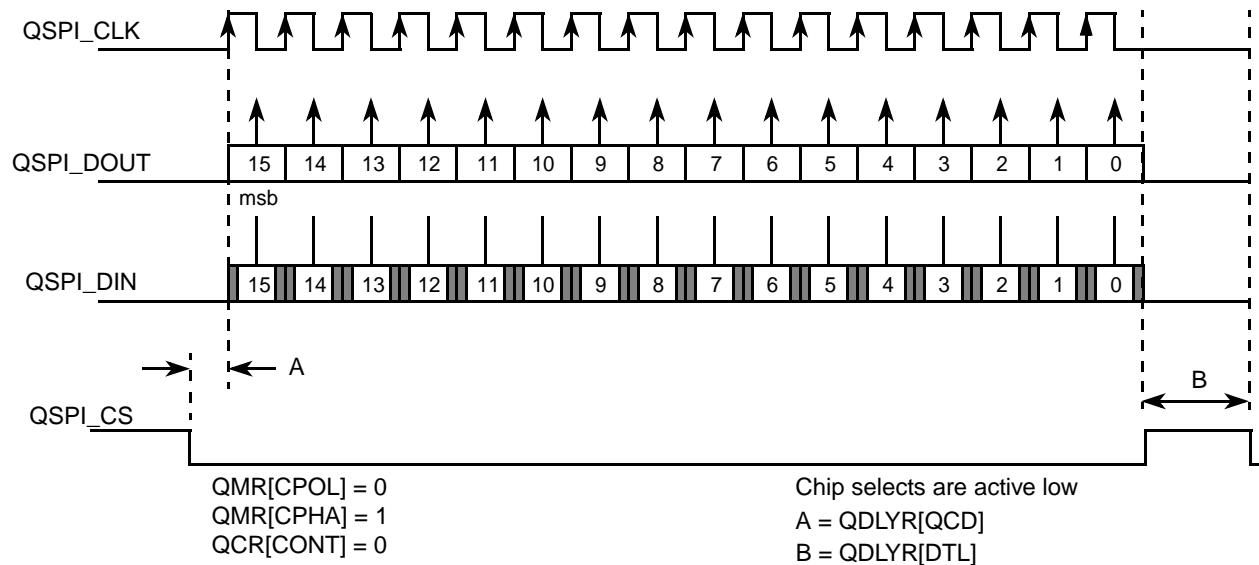


Figure 23-3. QSPI Clocking and Data Transfer Example

23.3.2 QSPI Delay Register (QDLYR)

The QDLYR is used to initiate master mode transfers and to set various delay parameters.

Address: 0xFC05_C004 (QDLYR)

Access: User read/write

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	SPE	QCD								DTL						
Reset	0	0	0	0	0	1	0	0	0	0	0	0	0	1	0	0

Figure 23-4. QSPI Delay Register (QDLYR)

Table 23-4. QDLYR Field Descriptions

Field	Description
15 SPE	QSPI enable. When set, the QSPI initiates transfers in master mode by executing commands in the command RAM. The QSPI clears this bit automatically when a transfer completes. The user can also clear this bit to abort transfer unless QIR[ABRTL] is set. The recommended method for aborting transfers is to set QWR[HALT].
14–8 QCD	QSPI_CLK delay. When the DSCK bit in the command RAM is set this field determines the length of the delay from assertion of the chip selects to valid QSPI_CLK transition. See Section 23.4.3, “Transfer Delays” for information on setting this bit field.
7–0 DTL	Delay after transfer. When the DT bit in the command RAM is set this field determines the length of delay after the serial transfer.

23.3.3 QSPI Wrap Register (QWR)

The QSPI wrap register provides halt transfer control, wraparound settings, and queue pointer locations.

Address: 0xFC05_C008 (QWR)

Access: User read/write

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	HALT	WREN	WRT0	CSIV	ENDQP				CPTQP				NEWQP			
W																
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Figure 23-5. QSPI Wrap Register (QWR)

Table 23-5. QWR Field Descriptions

Field	Description
15 HALT	Halt transfers. Assertion of this bit causes the QSPI to stop execution of commands after it has completed execution of the current command.
14 WREN	Wraparound enable. Enables wraparound mode. 0 Execution stops after executing the command pointed to by QWR[ENDQP]. 1 After executing command pointed to by QWR[ENDQP], wrap back to entry zero, or the entry pointed to by QWR[NEWQP] and continue execution.
13 WRT0	Wraparound location. Determines where the QSPI wraps to in wraparound mode. 0 Wrap to RAM entry zero. 1 Wrap to RAM entry pointed to by QWR[NEWQP].
12 CSIV	QSPI_CS inactive level. 0 QSPI chip select outputs return to zero when not driven from the value in the current command RAM entry during a transfer (that is, inactive state is 0, chip selects are active high). 1 QSPI chip select outputs return to one when not driven from the value in the current command RAM entry during a transfer (that is, inactive state is 1, chip selects are active low).
11–8 ENDQP	End of queue pointer. Points to the RAM entry that contains the last transfer description in the queue.
7–4 CPTQP	Completed queue entry pointer. Points to the RAM entry that contains the last command to have been completed. This field is read only.
3–0 NEWQP	Start of queue pointer. This 4-bit field points to the first entry in the RAM to be executed on initiating a transfer.

23.3.4 QSPI Interrupt Register (QIR)

The QIR contains QSPI interrupt enables and status flags.

Address: 0xFC05_C00C (QIR)

Access: User read/write

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	WCEFB	ABRTB	0	ABRTL	WCEFE	ABRTE	0	SPIFE	0	0	0	0	WCEF	ABRT	0	SPIF
W													w1c	w1c		w1c
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Figure 23-6. QSPI Interrupt Register (QIR)

Table 23-6. QIR Field Descriptions

Field	Description
15 WCEFB	Write collision access error enable. A write collision occurs during a data transfer when the RAM entry containing the current command is written to by the CPU with the QDR. When this bit is asserted, the write access to QDR results in an access error.
14 ABRTB	Abort access error enable. An abort occurs when QDLYR[SPE] is cleared during a transfer. When set, an attempt to clear QDLYR[SPE] during a transfer results in an access error.
13	Reserved, must be cleared.
12 ABRTL	Abort lock-out. When set, QDLYR[SPE] cannot be cleared by writing to the QDLYR. QDLYR[SPE] is only cleared by the QSPI when a transfer completes.
11 WCEFE	Write collision (WCEF) interrupt enable. 0 Write collision interrupt disabled 1 Write collision interrupt enabled
10 ABRTE	Abort (ABRT) interrupt enable. 0 Abort interrupt disabled 1 Abort interrupt enabled
9	Reserved, must be cleared.
8 SPIFE	QSPI finished (SPIF) interrupt enable. 0 SPIF interrupt disabled 1 SPIF interrupt enabled
7–4	Reserved, must be cleared.
3 WCEF	Write collision error flag. Indicates that an attempt has been made to write to the RAM entry that is currently being executed. Writing a 1 to this bit (w1c) clears it and writing 0 has no effect.
2 ABRT	Abort flag. Indicates that QDLYR[SPE] has been cleared by the user writing to the QDLYR rather than by completion of the command queue by the QSPI. Writing a 1 to this bit (w1c) clears it and writing 0 has no effect.
1	Reserved, must be cleared.
0 SPIF	QSPI finished flag. Asserted when the QSPI has completed all the commands in the queue. Set on completion of the command pointed to by QWR[ENDQP], and on completion of the current command after assertion of QWR[HALT]. In wraparound mode, this bit is set every time the command pointed to by QWR[ENDQP] is completed. Writing a 1 to this bit (w1c) clears it and writing 0 has no effect.

23.3.5 QSPI Address Register (QAR)

The QAR is used to specify the location in the QSPI RAM that read and write operations affect. As shown in [Section 23.4.1, “QSPI RAM”](#), the transmit RAM is located at addresses 0x0 to 0xF, the receive RAM is located at 0x10 to 0x1F, and the command RAM is located at 0x20 to 0x2F. (These addresses refer to the QSPI RAM space, not the device memory map.)

NOTE

A read or write to the QSPI RAM causes QAR to increment. However, the QAR does not wrap after the last queue entry within each section of the RAM. The application software must manage address range errors.

Address: 0xFC05_C010 (QAR)

Access: User read/write

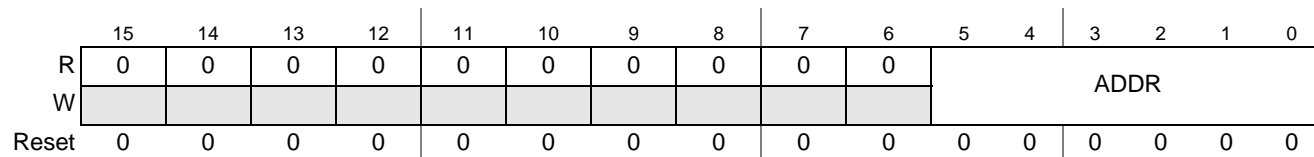


Figure 23-7. QSPI Address Register (QAR)

Table 23-7. QAR Field Descriptions

Field	Description
15–6	Reserved, must be cleared.
5–0 ADDR	Address used to read/write the QSPI RAM. Ranges are as follows: 0x00–0x0F Transmit RAM 0x10–0x1F Receive RAM 0x20–0x2F Command RAM 0x30–0x3F Reserved

23.3.6 QSPI Data Register (QDR)

The QDR is used to access QSPI RAM indirectly. The CPU reads and writes all data from and to the QSPI RAM through this register.

A write to QDR causes data to be written to the RAM entry specified by QAR[ADDR]. This also causes the value in QAR to increment. Correspondingly, a read at QDR returns the data in the RAM at the address specified by QAR[ADDR]. This also causes QAR to increment. A read access requires a single wait state.

Address: 0xFC05_C014 (QDR)

Access: User read/write

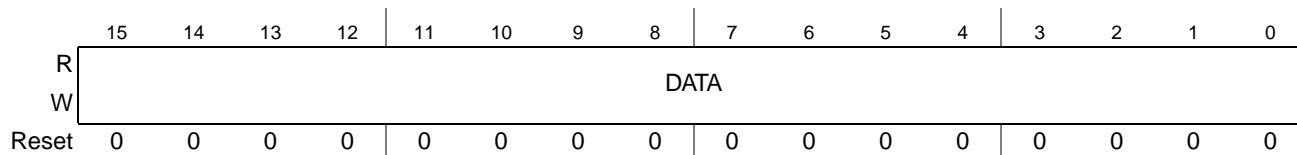


Figure 23-8. QSPI Data Register (QDR)

Table 23-8. QDR Field Descriptions

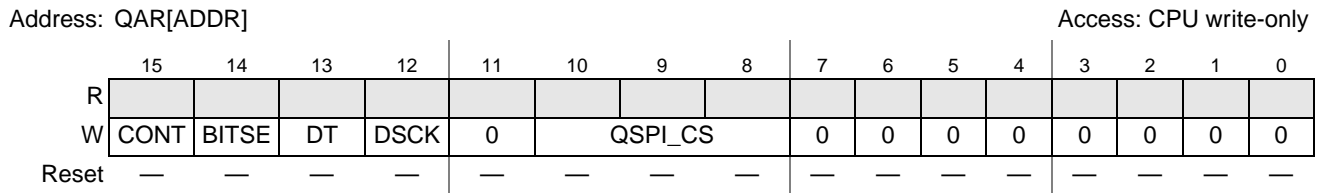
Field	Description
15–0 DATA	A write to this field causes data to be written to the QSPI RAM entry specified by QAR[ADDR]. Similarly, a read of this field returns the data in the QSPI RAM at the address specified by QAR[ADDR]. During command RAM accesses (QAR[ADDR] = 0x20–0x2F), only the most significant byte of this field is used.

23.3.7 Command RAM Registers (QCR0–QCR15)

The command RAM is accessed using the upper byte of the QDR; the QSPI cannot modify information in command RAM. There are 16 bytes in the command RAM. Each byte is divided into two fields. The chip select field enables external peripherals for transfer. The command field provides transfer operations.

NOTE

The command RAM is accessed only using the most significant byte of QDR and indirect addressing based on QAR[ADDR].

**Figure 23-9. Command RAM Registers (QCR0–QCR15)****Table 23-9. QCR0–QCR15 Field Descriptions**

Field	Description
15 CONT	Continuous. 0 Chip selects return to inactive level defined by QWR[CSIV] when a single word transfer is complete. 1 Chip selects return to inactive level defined by QWR[CSIV] only after the transfer of the queue entries (max of 16 words). Note: To keep the chip selects asserted for transfers beyond 16 words, the QWR[CSIV] bit must be set to control the level that the chip selects return to after the first transfer.
14 BITSE	Bits per transfer enable. 0 Eight bits 1 Number of bits set in QMR[BITS]
13 DT	Delay after transfer enable. 0 Default reset value. 1 The QSPI provides a variable delay at the end of serial transfer to facilitate interfacing with peripherals that have a latency requirement. The delay between transfers is determined by QDLR[DTL].
12 DSCK	Chip select to QSPI_CLK delay enable. 0 Chip select valid to QSPI_CLK transition is one-half QSPI_CLK period. 1 QDLR[QCD] specifies the delay from QSPI_CS valid to QSPI_CLK.
11	Reserved, must be cleared.
10–8 QSPI_CS	Peripheral chip selects. Used to select an external device for serial data transfer. More than one chip select may be active at once, and more than one device can be connected to each chip select. Bits 10-8 map directly to the corresponding QSPI_CS n pins. If more than three chip selects are needed, then an external demultiplexor can be used with the QSPI_CS n pins. Note: Not all chip selects may be available on all device packages. See Chapter 2, “Signal Descriptions,” for details on which chip selects are pinned-out.
7–0	Reserved, must be cleared.

23.4 Functional Description

The QSPI uses a dedicated 80-byte block of static RAM accessible to the module and CPU to perform queued operations. The RAM is divided into three segments:

- 16 command control bytes (command RAM)
- 32 transmit data bytes (transmit data RAM)

- 32 receive data bytes (receive data RAM)

The RAM is organized so that 1 byte of command control data, 1 word of transmit data, and 1 word of receive data comprise 1 of the 16 queue entries (0x0–0xF).

NOTE

Throughout ColdFire documentation, the term word is used to designate a 16-bit data unit. The only exceptions to this appear in discussions of serial communication modules such as QSPI that support variable-length data units. To simplify these discussions, the functional unit is referred to as a word regardless of length.

The user initiates QSPI operation by loading a queue of commands in command RAM, writing transmit data into transmit RAM, and then enabling the QSPI data transfer. The QSPI executes the queued commands and sets the completion flag in the QSPI interrupt register (QIR[SPIF]) to signal their completion. As another option, QIR[SPIFE] can be enabled to generate an interrupt.

The QSPI uses four queue pointers. The user can access three of them through fields in QSPI wrap register (QWR):

- New queue pointer (QWR[NEWQP])—points to the first command in the queue
- Internal queue pointer—points to the command currently being executed
- Completed queue pointer (QWR[CPTQP])—points to the last command executed
- End queue pointer (QWR[ENDQP]) —points to the final command in the queue

The internal pointer is initialized to the same value as QWR[NEWQP]. During normal operation, the following sequence repeats:

1. The command pointed to by the internal pointer is executed.
2. The value in the internal pointer is copied into QWR[CPTQP].
3. The internal pointer is incremented.

Execution continues at the internal pointer address unless the QWR[NEWQP] value is changed. After each command is executed, QWR[ENDQP] and QWR[CPTQP] are compared. When a match occurs, QIR[SPIF] is set and the QSPI stops unless wraparound mode is enabled. Setting QWR[WREN] enables wraparound mode.

QWR[NEWQP] is cleared at reset. When the QSPI is enabled, execution begins at address 0x0 unless another value has been written into QWR[NEWQP]. QWR[ENDQP] is cleared at reset but is changed to show the last queue entry before the QSPI is enabled. QWR[NEWQP] and QWR[ENDQP] can be written at any time. When the QWR[NEWQP] value changes, the internal pointer value also changes unless a transfer is in progress, in which case the transfer completes normally. Leaving QWR[NEWQP] and QWR[ENDQP] set to 0x0 causes a single transfer to occur when the QSPI is enabled.

Data is transferred relative to QSPI_CLK, which can be generated in any one of four combinations of phase and polarity using QMR[CPHA,CPOL]. Data is transferred with the most significant bit (msb) first. The number of bits transferred defaults to 8, but can be set to any value between 8 and 16 by writing a value into the BITSE field of the command RAM (QCR[BITSE]).

23.4.1 QSPI RAM

The QSPI contains an 80-byte block of static RAM that can be accessed by the user and the QSPI. This RAM does not appear in the device memory map, because it can only be accessed by the user indirectly through the QSPI address register (QAR) and the QSPI data register (QDR). The RAM is divided into three segments with 16 addresses each:

- Receive data RAM—the initial destination for all incoming data
- Transmit data RAM—a buffer for all out-bound data
- Command RAM—where commands are loaded

The transmit data and command RAM are user write-only. The receive RAM is user read-only.

Figure 23-10 shows the RAM configuration. The RAM contents are undefined immediately after a reset.

The command and data RAM in the QSPI are indirectly accessible with QDR and QAR as 48 separate locations that comprise 16 words of transmit data, 16 words of receive data, and 16 bytes of commands.

A write to QDR causes data to be written to the RAM entry specified by QAR[ADDR] and causes the value in QAR to increment. Correspondingly, a read from QDR returns the data in the RAM at the address specified by QAR[ADDR]. This also causes QAR to increment. A read access requires a single wait state.

Relative Address	Register	Function
0x00	QTR0	Transmit RAM 16 bits wide
0x01	QTR1	
...	...	
0x0F	QTR15	
0x10	QRR0	Receive RAM 16 bits wide
0x11	QRR1	
...	...	
0x1F	QRR15	
0x20	QCR0	Command RAM 8 bits wide
0x21	QCR1	
...	...	
0x2F	QCR15	

Figure 23-10. QSPI RAM Model

23.4.1.1 Receive RAM

Data received by the QSPI is stored in the receive RAM segment located at 0x10 to 0x1F in the QSPI RAM space. Read this segment to retrieve data from the QSPI. Data words with less than 16 bits are stored in

the least significant bits of the RAM. Unused bits in a receive queue entry are set to zero upon completion of the individual queue entry. Receive RAM is not writeable.

QWR[CPTQP] shows which queue entries have been executed. The user can query this field to determine which locations in receive RAM contain valid data.

23.4.1.2 Transmit RAM

Data to be transmitted by the QSPI is stored in the transmit RAM segment located at addresses 0x0 to 0xF. The user normally writes 1 word into this segment for each queue command to be executed. The user cannot read data in the transmit RAM.

Outbound data must be written to transmit RAM in a right-justified format. The unused bits are ignored. The QSPI copies the data to its data serializer (shift register) for transmission. The data is transmitted most significant bit first and remains in transmit RAM until overwritten by the user.

23.4.1.3 Command RAM

The CPU writes one byte of control information to this segment for each QSPI command to be executed. Command RAM, referred to as QCR0–15, is write-only memory from a user's perspective.

Command RAM consists of 16 bytes, each divided into two fields. The peripheral chip select field controls the QSPI_CS signal levels for the transfer. The command control field provides transfer options.

A maximum of 16 commands can be in the queue. Queue execution proceeds from the address in QWR[NEWQP] through the address in QWR[ENDQP].

The QSPI executes a queue of commands defined by the control bits in each command RAM entry that sequence the following actions:

- Chip-select pins are activated.
- Data is transmitted from the transmit RAM and received into the receive RAM.
- The synchronous transfer clock QSPI_CLK is generated.

Before any data transfers begin, control data must be written to the command RAM, and any out-bound data must be written to the transmit RAM. Also, the queue pointers must be initialized to the first and last entries in the command queue.

Data transfer is synchronized with the internally generated QSPI_CLK, whose phase and polarity are controlled by QMR[CPHA] and QMR[CPOL]. These control bits determine which QSPI_CLK edge is used to drive outgoing data and to latch incoming data.

23.4.2 Baud Rate Selection

The maximum QSPI clock frequency is one-fourth the clock frequency of the internal bus clock ($f_{\text{sys}/2}$). Baud rate is selected by writing a value from 2–255 into QMR[BAUD]. The QSPI uses a prescaler to derive the QSPI_CLK rate from the internal bus clock divided by two. [Table 23-10](#) shows the QSPI_CLK frequency as a function of internal bus clock and baud rate.

A baud rate value of zero turns off the QSPI_CLK.

The desired QSPI_CLK baud rate is related to the internal bus clock and QMR[BAUD] by the following expression:

$$\text{QMR[BAUD]} = \frac{f_{\text{sys}/2}}{2 \times [\text{desired QSPI_CLK baud rate}]} \quad \text{Eqn. 23-1}$$

Table 23-10. QSPI_CLK Frequency as Function of Internal Bus Clock and Baud Rate

Internal Bus Clock = 83.33 MHz	
QMR [BAUD]	QSPI_CLK
2	20.83 MHz
4	10.425 MHz
8	5.208 MHz
16	2.604 MHz
32	1.302 MHz
255	163.39 kHz

23.4.3 Transfer Delays

The QSPI supports programmable delays for the QSPI_CS signals before and after a transfer. The time between QSPI_CS assertion and the leading QSPI_CLK edge, and the time between the end of one transfer and the beginning of the next, are both independently programmable.

The chip select to clock delay enable bit in the command RAM, QCR[DSCK], enables the programmable delay period from QSPI_CS assertion until the leading edge of QSPI_CLK. QDLYR[QCD] determines the period of delay before the leading edge of QSPI_CLK. The following expression determines the actual delay before the QSPI_CLK leading edge:

$$\text{QSPI_CS-to-QSPI_CLK delay} = \frac{\text{QDLYR[QCD]}}{f_{\text{sys}/2}} \quad \text{Eqn. 23-2}$$

QDLYR[QCD] has a range of 1–127.

When QDLYR[QCD] or QCR[DSCK] equals zero, the standard delay of one-half the QSPI_CLK period is used.

The command RAM delay after transmit enable bit, QCR[DT], enables the programmable delay period from the negation of the QSPI_CS signals until the start of the next transfer. The delay after transfer can be used to provide a peripheral deselection interval. A delay can also be inserted between consecutive transfers to allow serial A/D converters to complete conversion. There are two transfer delay options: the user can choose to delay a standard period after serial transfer is complete or can specify a delay period. Writing a value to QDLYR[DTL] specifies a delay period. QCR[DT] determines whether the standard delay period (DT = 0) or the specified delay period (DT = 1) is used. The following expression is used to calculate the delay when DT equals 1:

$$\text{Delay after transfer} = \frac{32 \times \text{QDLYR[DTL]}}{f_{\text{sys}/2}} \quad (\text{DT} = 1) \quad \text{Eqn. 23-3}$$

where QDLYR[DTL] has a range of 1–255. A zero value for DTL causes a delay-after-transfer value of $8192/f_{\text{sys}/2}$. Standard delay period ($DT = 0$) is calculated by the following:

$$\text{Standard delay after transfer} = \frac{17}{f_{\text{sys}/2}} \quad (DT = 0) \quad \text{Eqn. 23-4}$$

Adequate delay between transfers must be specified for long data streams because the QSPI module requires time to load a transmit RAM entry for transfer. Receiving devices need at least the standard delay between successive transfers. If the internal bus clock is operating at a slower rate, the delay between transfers must be increased proportionately.

23.4.4 Transfer Length

There are two transfer length options. The user can choose a default value of 8 bits or a programmed value of 8 to 16 bits. The programmed value must be written into QMR[BITS]. The command RAM bits per transfer enable field, QCR[BITSE], determines whether the default value ($BITSE = 0$) or the BITS[3–0] value ($BITSE = 1$) is used. QMR[BITS] indicates the required number of bits to be transferred, with the default value of 16 bits.

23.4.5 Data Transfer

The transfer operation is initiated by setting QDLYR[SPE]. Shortly after QDLYR[SPE] is set, the QSPI executes the command at the command RAM address pointed to by QWR[NEWQP]. Data at the pointer address in transmit RAM is loaded into the data serializer and transmitted. Data that is simultaneously received is stored at the pointer address in receive RAM.

When the proper number of bits has been transferred, the QSPI stores the working queue pointer value in QWR[CPTQP], increments the working queue pointer, and loads the next data for transfer from the transmit RAM. The command pointed to by the incremented working queue pointer is executed next unless a new value has been written to QWR[NEWQP]. If a new queue pointer value is written while a transfer is in progress, the current transfer is completed normally.

When the CONT bit in the command RAM is set, the QSPI_CS n signals are asserted between transfers. When CONT is cleared, QSPI_CS n are negated between transfers. The QSPI_CS n signals are not high impedance.

When the QSPI reaches the end of the queue, it asserts the SPIF flag, QIR[SPIF]. If QIR[SPIFE] is set, an interrupt request is generated when QIR[SPIF] is asserted. Then the QSPI clears QDLYR[SPE] and stops, unless wraparound mode is enabled.

Wraparound mode is enabled by setting QWR[WREN]. The queue can wrap to pointer address 0x0, or to the address specified by QWR[NEWQP], depending on the state of QWR[WRTO].

In wraparound mode, the QSPI cycles through the queue continuously, even while requesting interrupt service. QDLYR[SPE] is not cleared when the last command in the queue is executed. New receive data overwrites previously received data in the receive RAM. Each time the end of the queue is reached,

QIR[SPIFE] is set. QIR[SPIF] is not automatically reset. If interrupt driven QSPI service is used, the service routine must clear QIR[SPIF] to abort the current request. Additional interrupt requests during servicing can be prevented by clearing QIR[SPIFE].

There are two recommended methods of exiting wraparound mode: clearing QWR[WREN] or setting QWR[HALT]. Exiting wraparound mode by clearing QDLYR[SPE] is not recommended because this may abort a serial transfer in progress. The QSPI sets SPIF, clears QDLYR[SPE], and stops the first time it reaches the end of the queue after QWR[WREN] is cleared. After QWR[HALT] is set, the QSPI finishes the current transfer, then stops executing commands. After the QSPI stops, QDLYR[SPE] can be cleared.

23.5 Initialization/Application Information

The following steps are necessary to set up the QSPI 12-bit data transfers and a QSPI_CLK of 5.188 MHz. The QSPI RAM is set up for a queue of 12 transfers. All three QSPI_CS signals are used in this example.

1. Write the QMR with 0xB308 to set up 12-bit data words with the data shifted on the falling clock edge, and a QSPI_CLK frequency of 5.188 MHz (assuming a 83.33-MHz internal bus clock).
2. Write QDLYR with the desired delays.
3. Write QIR with 0xD00F to enable write collision, abort bus errors, and clear any interrupts.
4. Write QAR with 0x0020 to select the first command RAM entry.
5. Write QDR with 0x7E00, 0x7E00, 0x7E00, 0x7E00, 0x7D00, 0x7D00, 0x7D00, 0x7D00, 0x7B00, 0x7B00, 0x7B00, and 0x7B00 to set up four transfers for each chip select. The chip selects are active low in this example.
6. Write QAR with 0x0000 to select the first transmit RAM entry.
7. Write QDR with twelve 12-bit words of data.
8. Write QWR with 0x0B00 to set up a queue beginning at entry 0 and ending at entry 11.
9. Set QDLYR[SPE] to enable the transfers.
10. Wait until the transfers are complete. QIR[SPIF] is set when the transfers are complete.
11. Write QAR with 0x0010 to select the first receive RAM entry.
12. Read QDR to get the received data for each transfer.
13. Repeat steps 5 through 13 to do another transfer.

Chapter 24

UART Modules

24.1 Introduction

This chapter describes the use of the three universal asynchronous receiver/transmitters (UARTs) and includes programming examples.

NOTE

The designation n appears throughout this section to refer to registers or signals associated with one of the three identical UART modules: UART0, UART1, or UART2.

24.1.1 Overview

The internal bus clock can clock each of the three independent UARTs, eliminating the need for an external UART clock. As [Figure 24-1](#) shows, each UART module interfaces directly to the CPU and consists of:

- Serial communication channel
- Programmable clock generation
- Interrupt control logic and DMA request logic
- Internal channel control logic

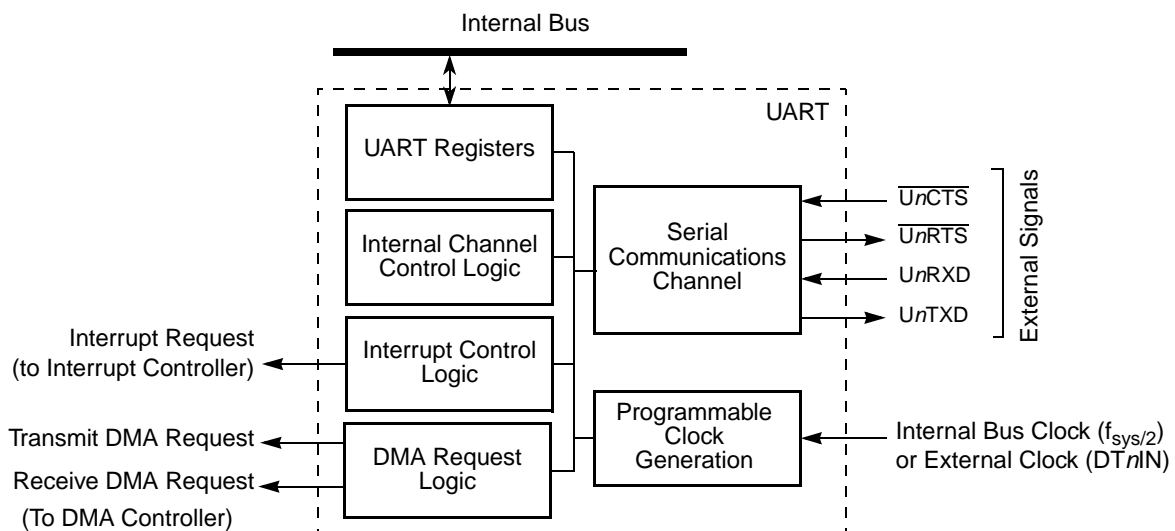


Figure 24-1. UART Block Diagram

NOTE

The DTnIN pin can clock UARTn. However, if the timers are operating and the UART uses DTnIN as a clock source, input capture mode is not available for that timer.

The serial communication channel provides a full-duplex asynchronous/synchronous receiver and transmitter deriving an operating frequency from the internal bus clock or an external clock using the timer pin. The transmitter converts parallel data from the CPU to a serial bit stream, inserting appropriate start, stop, and parity bits. It outputs the resulting stream on the transmitter serial data output (UnTXD). See [Section 24.4.2.1, “Transmitter.”](#)

The receiver converts serial data from the receiver serial data input (UnRXD) to parallel format, checks for a start, stop, and parity bits, or break conditions, and transfers the assembled character onto the bus during read operations. The receiver may be polled, interrupt driven, or use DMA requests for servicing. See [Section 24.4.2.2, “Receiver.”](#)

NOTE

The GPIO module must be configured to enable the peripheral function of the appropriate pins (refer to [Chapter 13, “General Purpose I/O Module”](#)) prior to configuring the UART module.

24.1.2 Features

The device contains three independent UART modules with:

- Each clocked by external clock or internal bus clock (eliminates need for an external UART clock)
- Full-duplex asynchronous/synchronous receiver/transmitter
- Quadruple-buffered receiver
- Double-buffered transmitter
- Independently programmable receiver and transmitter clock sources
- Programmable data format:
 - 5–8 data bits plus parity
 - Odd, even, no parity, or force parity
 - One, one-and-a-half, or two stop bits
- Each serial channel programmable to normal (full-duplex), automatic echo, local loopback, or remote loopback mode
- Automatic wake-up mode for multidrop applications
- Four maskable interrupt conditions
- All three UARTs have DMA request capability
- Parity, framing, and overrun error detection
- False-start bit detection
- Line-break detection and generation
- Detection of breaks originating in the middle of a character

- Start/end break interrupt/status

24.2 External Signal Description

Table 24-1 briefly describes the UART module signals.

Table 24-1. UART Module External Signals

Signal	Description
\overline{UnTXD}	Transmitter Serial Data Output. \overline{UnTXD} is held high (mark condition) when the transmitter is disabled, idle, or operating in the local loopback mode. Data is shifted out on \overline{UnTXD} on the falling edge of the clock source, with the least significant bit (lsb) sent first.
\overline{UnRXD}	Receiver Serial Data Input. Data received on \overline{UnRXD} is sampled on the rising edge of the clock source, with the lsb received first.
\overline{UnCTS}	Clear-to-Send. This input can generate an interrupt on a change of state.
\overline{UnRTS}	Request-to-Send. This output can be programmed to be negated or asserted automatically by the receiver or the transmitter. When connected to a transmitter's \overline{UnCTS} , \overline{UnRTS} can control serial data flow.

Figure 24-2 shows a signal configuration for a UART/RS-232 interface.

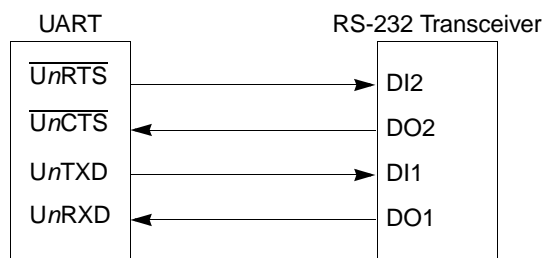


Figure 24-2. UART/RS-232 Interface

24.3 Memory Map/Register Definition

This section contains a detailed description of each register and its specific function. Flowcharts in Section 24.5, “Initialization/Application Information,” describe basic UART module programming. Writing control bytes into the appropriate registers controls the operation of the UART module.

NOTE

UART registers are accessible only as bytes.

NOTE

Interrupt can mean an interrupt request asserted to the CPU or a DMA request.

Table 24-2. UART Module Memory Map

Address	Register	Width (bit)	Access	Reset Value	Section/Page
UART0 UART1 UART2					
0xFC06_0000 0xFC06_4000 0xFC06_8000	UART Mode Registers ¹ (UMR1 <i>n</i>), (UMR2 <i>n</i>)	8	R/W	0x00	24.3.1/24-5 24.3.2/24-6
0xFC06_0004 0xFC06_4004 0xFC06_8004	UART Status Register (USR <i>n</i>)	8	R	0x00	24.3.3/24-8
	UART Clock Select Register ¹ (UCSR <i>n</i>)	8	W	See Section	24.3.4/24-9
0xFC06_0008 0xFC06_4008 0xFC06_8008	UART Command Registers (UCR <i>n</i>)	8	W	0x00	24.3.5/24-9
0xFC06_000C 0xFC06_400C 0xFC06_800C	UART Receive Buffers (URB <i>n</i>)	8	R	0xFF	24.3.6/24-11
	UART Transmit Buffers (UTB <i>n</i>)	8	W	0x00	24.3.7/24-12
0xFC06_0010 0xFC06_4010 0xFC06_8010	UART Input Port Change Register (UIPCR <i>n</i>)	8	R	See Section	24.3.8/24-12
	UART Auxiliary Control Register (UACR <i>n</i>)	8	W	0x00	24.3.9/24-13
0xFC06_0014 0xFC06_4014 0xFC06_8014	UART Interrupt Status Register (UISR <i>n</i>)	8	R	0x00	24.3.10/24-13
	UART Interrupt Mask Register (UIMR <i>n</i>)	8	W	0x00	
0xFC06_0018 0xFC06_4018 0xFC06_8018	UART Baud Rate Generator Register (UBG1 <i>n</i>)	8	W ²	0x00	24.3.11/24-15
0xFC06_001C 0xFC06_401C 0xFC06_801C	UART Baud Rate Generator Register (UBG2 <i>n</i>)	8	W ²	0x00	24.3.11/24-15
0xFC06_0034 0xFC06_4034 0xFC06_8034	UART Input Port Register (UIP <i>n</i>)	8	R	0xFF	24.3.12/24-15
0xFC06_0038 0xFC06_4038 0xFC06_8038	UART Output Port Bit Set Command Register (UOP1 <i>n</i>)	8	W ²	0x00	24.3.13/24-16
0xFC06_003C 0xFC06_403C 0xFC06_803C	UART Output Port Bit Reset Command Register (UOP0 <i>n</i>)	8	W ²	0x00	24.3.13/24-16

¹ UMR1*n*, UMR2*n*, and UCSR*n* must be changed only after the receiver/transmitter is issued a software reset command. If operation is not disabled, undesirable results may occur.

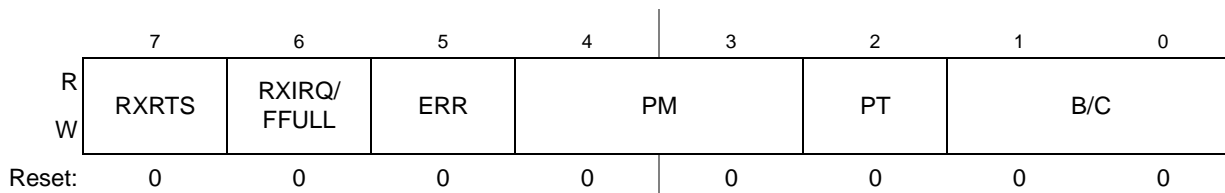
² Reading this register results in undesired effects and possible incorrect transmission or reception of characters. Register contents may also be changed.

24.3.1 UART Mode Registers 1 (UMR1 n)

The UMR1 n registers control UART module configuration. UMR1 n can be read or written when the mode register pointer points to it, at RESET or after a RESET MODE REGISTER POINTER command using UCR n [MISC]. After UMR1 n is read or written, the pointer points to UMR2 n .

Address: 0xFC06_0000 (UMR10)
 0xFC06_4000 (UMR11)
 0xFC06_8000 (UMR12)

Access: User read/write¹



¹ After UMR1 n is read or written, the pointer points to UMR2 n

Figure 24-3. UART Mode Registers 1 (UMR1 n)

Table 24-3. UMR1 n Field Descriptions

Field	Description
7 RXRTS	Receiver request-to-send. Allows the \overline{UnRTS} output to control the \overline{UnCTS} input of the transmitting device to prevent receiver overrun. If the receiver and transmitter are incorrectly programmed for \overline{UnRTS} control, \overline{UnRTS} control is disabled for both. Transmitter RTS control is configured in UMR2 n [TXRTS]. 0 The receiver has no effect on \overline{UnRTS} . 1 When a valid start bit is received, \overline{UnRTS} is negated if the UART's FIFO is full. \overline{UnRTS} is reasserted when the FIFO has an empty position available.
6 RXIRQ/ FFULL	Receiver interrupt select. 0 RXRDY is the source generating interrupt or DMA requests. 1 FFULL is the source generating interrupt or DMA requests.
5 ERR	Error mode. Configures the FIFO status bits, USR n [RB,FE,PE]. 0 Character mode. The USR n values reflect the status of the character at the top of the FIFO. ERR must be 0 for correct A/D flag information when in multidrop mode. 1 Block mode. The USR n values are the logical OR of the status for all characters reaching the top of the FIFO since the last RESET ERROR STATUS command for the UART was issued. See Section 24.3.5, "UART Command Registers (UCRn)" .
4–3 PM	Parity mode. Selects the parity or multidrop mode for the UART. The parity bit is added to the transmitted character, and the receiver performs a parity check on incoming data. The value of PM affects PT, as shown below.

Table 24-3. UMR1*n* Field Descriptions (continued)

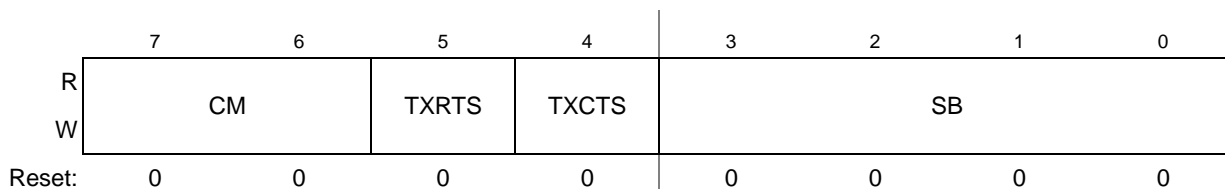
Field	Description																				
2 PT	<p>Parity type. PM and PT together select parity type (PM = 0x) or determine whether a data or address character is transmitted (PM = 11).</p> <table><tr><th>PM</th><th>Parity Mode</th><th>Parity Type (PT= 0)</th><th>Parity Type (PT= 1)</th></tr><tr><td>00</td><td>With parity</td><td>Even parity</td><td>Odd parity</td></tr><tr><td>01</td><td>Force parity</td><td>Low parity</td><td>High parity</td></tr><tr><td>10</td><td>No parity</td><td colspan="2">N/A</td></tr><tr><td>11</td><td>Multidrop mode</td><td>Data character</td><td>Address character</td></tr></table>	PM	Parity Mode	Parity Type (PT= 0)	Parity Type (PT= 1)	00	With parity	Even parity	Odd parity	01	Force parity	Low parity	High parity	10	No parity	N/A		11	Multidrop mode	Data character	Address character
PM	Parity Mode	Parity Type (PT= 0)	Parity Type (PT= 1)																		
00	With parity	Even parity	Odd parity																		
01	Force parity	Low parity	High parity																		
10	No parity	N/A																			
11	Multidrop mode	Data character	Address character																		
1–0 B/C	<p>Bits per character. Selects the number of data bits per character to be sent. The values shown do not include start, parity, or stop bits.</p> <p>00 5 bits 01 6 bits 10 7 bits 11 8 bits</p>																				

24.3.2 UART Mode Register 2 (UMR2*n*)

The UMR2*n* registers control UART module configuration. UMR2*n* can be read or written when the mode register pointer points to it, which occurs after any access to UMR1*n*. UMR2*n* accesses do not update the pointer.

Address: 0xFC06_0000 (UMR20)
 0xFC06_4000 (UMR21)
 0xFC06_8000 (UMR22)

Access: User read/write¹



¹ After UMR1*n* is read or written, the pointer points to UMR2*n*

Figure 24-4. UART Mode Registers 2 (UMR2*n*)

Table 24-4. UMR2n Field Descriptions

Field	Description																																													
7–6 CM	Channel mode. Selects a channel mode. Section 24.4.3, “Looping Modes,” describes individual modes. 00 Normal 01 Automatic echo 10 Local loopback 11 Remote loopback																																													
5 TXRTS	Transmitter ready-to-send. Controls negation of \overline{UnRTS} to automatically terminate a message transmission. Attempting to program a receiver and transmitter in the same UART for \overline{UnRTS} control is not permitted and disables \overline{UnRTS} control for both. 0 The transmitter has no effect on \overline{UnRTS} . 1 In applications where the transmitter is disabled after transmission completes, setting this bit automatically clears UOP[RTS] one bit time after any characters in the transmitter shift and holding registers are completely sent, including the programmed number of stop bits.																																													
4 TXCTS	Transmitter clear-to-send. If TXCTS and TXRTS are set, TXCTS controls the operation of the transmitter. 0 \overline{UnCTS} has no effect on the transmitter. 1 Enables clear-to-send operation. The transmitter checks the state of \overline{UnCTS} each time it is ready to send a character. If \overline{UnCTS} is asserted, the character is sent; if it is deasserted, the signal $UnTXD$ remains in the high state and transmission is delayed until \overline{UnCTS} is asserted. Changes in \overline{UnCTS} as a character is being sent do not affect its transmission.																																													
3–0 SB	Stop-bit length control. Selects length of stop bit appended to the transmitted character. Stop-bit lengths of 9/16 to 2 bits are programmable for 6–8 bit characters. Lengths of 1-1/16 to 2 bits are programmable for 5-bit characters. In all cases, the receiver checks only for a high condition at the center of the first stop-bit position, one bit time after the last data bit or after the parity bit, if parity is enabled. If an external 1x clock is used for the transmitter, clearing bit 3 selects one stop bit and setting bit 3 selects two stop bits for transmission. <div><table><tr><th>SB</th><th>5 Bits</th><th>6–8 Bits</th></tr><tr><td>0000</td><td>1.063</td><td>0.563</td></tr><tr><td>0001</td><td>1.125</td><td>0.625</td></tr><tr><td>0010</td><td>1.188</td><td>0.688</td></tr><tr><td>0011</td><td>1.250</td><td>0.750</td></tr><tr><td>0100</td><td>1.313</td><td>0.813</td></tr><tr><td>0101</td><td>1.375</td><td>0.875</td></tr><tr><td>0110</td><td>1.438</td><td>0.938</td></tr><tr><td>0111</td><td>1.500</td><td>1.000</td></tr></table><table><tr><th>SB</th><th>5–8 Bits</th></tr><tr><td>1000</td><td>1.563</td></tr><tr><td>1001</td><td>1.625</td></tr><tr><td>1010</td><td>1.688</td></tr><tr><td>1011</td><td>1.750</td></tr><tr><td>1100</td><td>1.813</td></tr><tr><td>1101</td><td>1.875</td></tr><tr><td>1110</td><td>1.938</td></tr><tr><td>1111</td><td>2.000</td></tr></table></div>	SB	5 Bits	6–8 Bits	0000	1.063	0.563	0001	1.125	0.625	0010	1.188	0.688	0011	1.250	0.750	0100	1.313	0.813	0101	1.375	0.875	0110	1.438	0.938	0111	1.500	1.000	SB	5–8 Bits	1000	1.563	1001	1.625	1010	1.688	1011	1.750	1100	1.813	1101	1.875	1110	1.938	1111	2.000
SB	5 Bits	6–8 Bits																																												
0000	1.063	0.563																																												
0001	1.125	0.625																																												
0010	1.188	0.688																																												
0011	1.250	0.750																																												
0100	1.313	0.813																																												
0101	1.375	0.875																																												
0110	1.438	0.938																																												
0111	1.500	1.000																																												
SB	5–8 Bits																																													
1000	1.563																																													
1001	1.625																																													
1010	1.688																																													
1011	1.750																																													
1100	1.813																																													
1101	1.875																																													
1110	1.938																																													
1111	2.000																																													

24.3.3 UART Status Registers (USR_n)

The USR_n registers show the status of the transmitter, the receiver, and the FIFO.

Address: 0xFC06_0004 (USR0)
 0xFC06_4004 (USR1)
 0xFC06_8004 (USR2)

Access: User read-only

	7	6	5	4	3	2	1	0
R	RB	FE	PE	OE	TXEMP	TXRDY	FFULL	RXRDY
W								
Reset:	0	0	0	0	0	0	0	0

Figure 24-5. UART Status Registers (USR_n)

Table 24-5. USR_n Field Descriptions

Field	Description
7 RB	Received break. The received break circuit detects breaks originating in the middle of a received character. However, a break in the middle of a character must persist until the end of the next detected character time. 0 No break was received. 1 An all-zero character of the programmed length was received without a stop bit. Only a single FIFO position is occupied when a break is received. Further entries to the FIFO are inhibited until U _n RXD returns to the high state for at least one-half bit time, which equals two successive edges of the UART clock. RB is valid only when RXRDY is set.
6 FE	Framing error. 0 No framing error occurred. 1 No stop bit was detected when the corresponding data character in the FIFO was received. The stop-bit check occurs in the middle of the first stop-bit position. FE is valid only when RXRDY is set.
5 PE	Parity error. Valid only if RXRDY is set. 0 No parity error occurred. 1 If UMR1 _n [PM] equals 0x (with parity or force parity), the corresponding character in the FIFO was received with incorrect parity. If UMR1 _n [PM] equals 11 (multidrop), PE stores the received address or data (A/D) bit. PE is valid only when RXRDY is set.
4 OE	Overrun error. Indicates whether an overrun occurs. 0 No overrun occurred. 1 One or more characters in the received data stream have been lost. OE is set upon receipt of a new character when the FIFO is full and a character is already in the shift register waiting for an empty FIFO position. When this occurs, the character in the receiver shift register and its break detect, framing error status, and parity error, if any, are lost. The RESET ERROR STATUS command in UCR _n clears OE.
3 TEMP	Transmitter empty. 0 The transmit buffer is not empty. A character is shifted out, or the transmitter is disabled. The transmitter is enabled/disabled by programming UCR _n [TC]. 1 The transmitter has underrun (the transmitter holding register and transmitter shift registers are empty). This bit is set after transmission of the last stop bit of a character if there are no characters in the transmitter holding register awaiting transmission.
2 TXRDY	Transmitter ready. 0 The CPU loaded the transmitter holding register, or the transmitter is disabled. 1 The transmitter holding register is empty and ready for a character. TXRDY is set when a character is sent to the transmitter shift register or when the transmitter is first enabled. If the transmitter is disabled, characters loaded into the transmitter holding register are not sent.

Table 24-5. USR n Field Descriptions (continued)

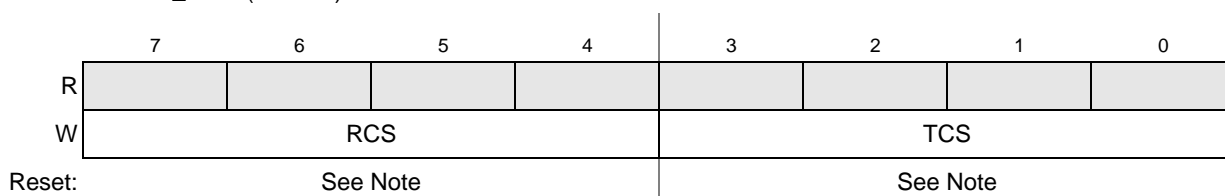
Field	Description
1 FFULL	FIFO full. 0 The FIFO is not full but may hold up to two unread characters. 1 A character was received and the receiver FIFO is now full. Any characters received when the FIFO is full are lost.
0 RXRDY	Receiver ready. 0 The CPU has read the receive buffer and no characters remain in the FIFO after this read. 1 One or more characters were received and are waiting in the receive buffer FIFO.

24.3.4 UART Clock Select Registers (UCSR n)

The UCSRs select an external clock on the DTIN input (divided by 1 or 16) or a prescaled internal bus clock as the clocking source for the transmitter and receiver. See [Section 24.4.1, “Transmitter/Receiver Clock Source.”](#) The transmitter and receiver can use different clock sources. To use the internal bus clock for both, set UCSR n to 0xDD.

Address: 0xFC06_0004 (UCSR0)
0xFC06_4004 (UCSR1)
0xFC06_8004 (UCSR2)

Access: User write-only



Note: The RCS and TCS reset values are set so the receiver and transmitter use the prescaled internal bus clock as their clock source.

Figure 24-6. UART Clock Select Registers (UCSR n)Table 24-6. UCSR n Field Descriptions

Field	Description
7–4 RCS	Receiver clock select. Selects the clock source for the receiver. 1101 Prescaled internal bus clock ($f_{sys/2}$) 1110 DTIN divided by 16 1111 DTIN
3–0 TCS	Transmitter clock select. Selects the clock source for the transmitter. 1101 Prescaled internal bus clock ($f_{sys/2}$) 1110 DTIN divided by 16 1111 DTIN

24.3.5 UART Command Registers (UCR n)

The UCRs supply commands to the UART. Only multiple commands that do not conflict can be specified in a single write to a UCR n . For example, RESET TRANSMITTER and ENABLE TRANSMITTER cannot be specified in one command.

Address: 0xFC06_0008 (UCR0)
 0xFC06_4008 (UCR1)
 0xFC06_8008 (UCR2)

Access: User write-only

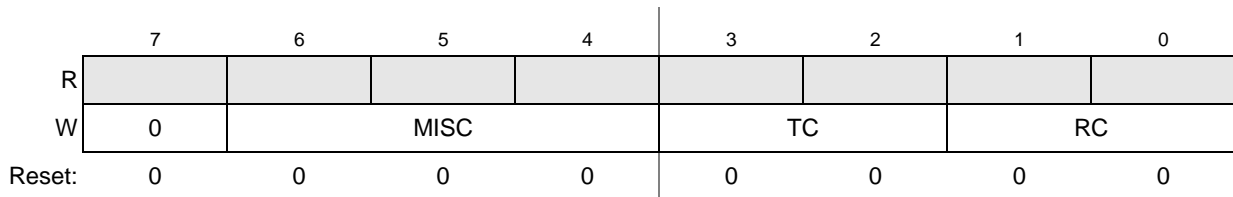


Figure 24-7. UART Command Registers (UCR_n)

Table 24-7 describes UCR_n fields and commands. Examples in [Section 24.4.2, “Transmitter and Receiver Operating Modes,”](#) show how these commands are used.

Table 24-7. UCR_n Field Descriptions

Field	Description		
7	Reserved, must be cleared.		
6–4 MISC	MISC Field (this field selects a single command)		
	Command	Description	
000	NO COMMAND	—	
001	RESET MODE REGISTER POINTER	Causes the mode register pointer to point to UMR1 _n .	
010	RESET RECEIVER	Immediately disables the receiver, clears USR _n [FFULL,RXRDY], and reinitializes the receiver FIFO pointer. No other registers are altered. Because it places the receiver in a known state, use this command instead of RECEIVER DISABLE when reconfiguring the receiver.	
011	RESET TRANSMITTER	Immediately disables the transmitter and clears USR _n [TXEMP,TXRDY]. No other registers are altered. Because it places the transmitter in a known state, use this command instead of TRANSMITTER DISABLE when reconfiguring the transmitter.	
100	RESET ERROR STATUS	Clears USR _n [RB,FE,PE,OE]. Also used in block mode to clear all error bits after a data block is received.	
101	RESET BREAK – CHANGE INTERRUPT	Clears the delta break bit, UISR _n [DB].	
110	START BREAK	Forces UnTXD low. If the transmitter is empty, break may be delayed up to one bit time. If the transmitter is active, break starts when character transmission completes. Break is delayed until any character in the transmitter shift register is sent. Any character in the transmitter holding register is sent after the break. Transmitter must be enabled for the command to be accepted. This command ignores the state of UnCTS.	
111	STOP BREAK	Causes UnTXD to go high (mark) within two bit times. Any characters in the transmit buffer are sent.	

Table 24-7. UCR_n Field Descriptions (continued)

Field	Description		
3–2 TC	Transmit command field. Selects a single transmit command.		
		Command	Description
	00	NO ACTION TAKEN	Causes the transmitter to stay in its current mode: if the transmitter is enabled, it remains enabled; if the transmitter is disabled, it remains disabled.
	01	TRANSMITTER ENABLE	Enables operation of the UART's transmitter. USR _n [TXEMP, TXRDY] are set. If the transmitter is already enabled, this command has no effect.
	10	TRANSMITTER DISABLE	Terminates transmitter operation and clears USR _n [TXEMP, TXRDY]. If a character is being sent when the transmitter is disabled, transmission completes before the transmitter becomes inactive. If the transmitter is already disabled, the command has no effect.
	11	—	Reserved, do not use.
1–0 RC	Receive command field. Selects a single receive command.		
		Command	Description
	00	NO ACTION TAKEN	Causes the receiver to stay in its current mode. If the receiver is enabled, it remains enabled; if disabled, it remains disabled.
	01	RECEIVER ENABLE	If the UART module is not in multidrop mode (UMR1 _n [PM] ≠ 11), RECEIVER ENABLE enables the UART's receiver and forces it into search-for-start-bit state. If the receiver is already enabled, this command has no effect.
	10	RECEIVER DISABLE	Disables the receiver immediately. Any character being received is lost. The command does not affect receiver status bits or other control registers. If the UART module is programmed for local loopback or multidrop mode, the receiver operates even though this command is selected. If the receiver is already disabled, the command has no effect.
	11	—	Reserved, do not use.

24.3.6 UART Receive Buffers (URB_n)

The receive buffers contain one serial shift register and three receiver holding registers, which act as a FIFO. UnRXD is connected to the serial shift register. The CPU reads from the top of the FIFO while the receiver shifts and updates from the bottom when the shift register is full (see [Figure 24-18](#)). RB contains the character in the receiver.

Address: 0xFC06_000C (URB0)
0xFC06_400C (URB1)
0xFC06_800C (URB2)

Access: User read-only

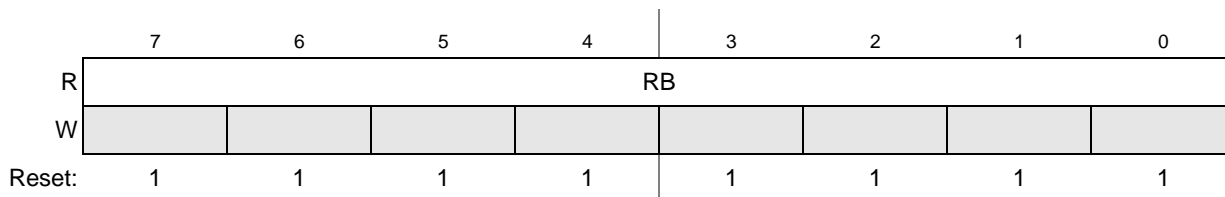


Figure 24-8. UART Receive Buffer (URB_n)

24.3.7 UART Transmit Buffers (UTB_n)

The transmit buffers consist of the transmitter holding register and the transmitter shift register. The holding register accepts characters from the bus master if UART's USR_n[TXRDY] is set. A write to the transmit buffer clears USR_n[TXRDY], inhibiting any more characters until the shift register can accept more data. When the shift register is empty, it checks if the holding register has a valid character to be sent (TXRDY = 0). If there is a valid character, the shift register loads it and sets USR_n[TXRDY] again. Writes to the transmit buffer when the UART's TXRDY is cleared and the transmitter is disabled have no effect on the transmit buffer.

Figure 24-9 shows UTB_n. TB contains the character in the transmit buffer.

Address: 0xFC06_000C (UTB0)
0xFC06_400C (UTB1)
0xFC06_800C (UTB2)

Access: User write-only

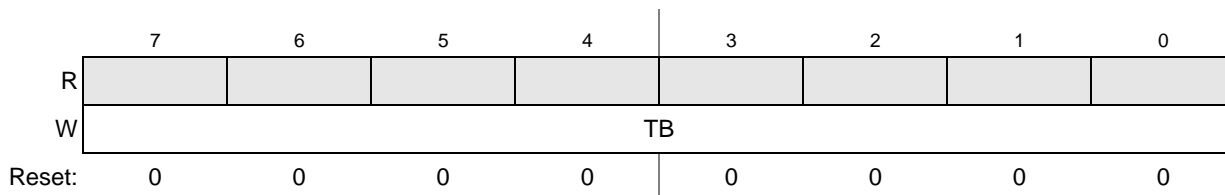


Figure 24-9. UART Transmit Buffer (UTB_n)

24.3.8 UART Input Port Change Registers (UIPCR_n)

The UIPCRs hold the current state and the change-of-state for \overline{UnCTS} .

Address: 0xFC06_0010 (UIPCR0)
0xFC06_4010 (UIPCR1)
0xFC06_8010 (UIPCR2)

Access: User read-only

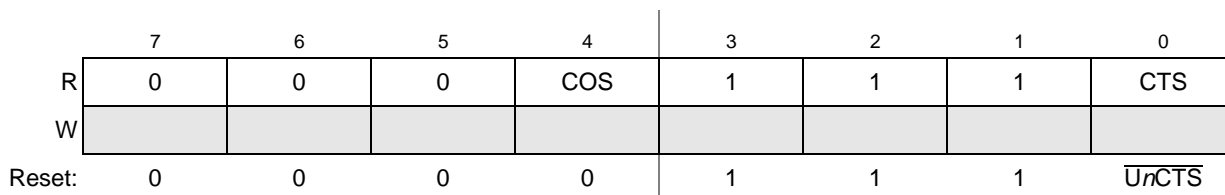


Figure 24-10. UART Input Port Changed Registers (UIPCR_n)

Table 24-8. UIPCR n Field Descriptions

Field	Description
7–5	Reserved
4 COS	Change of state (high-to-low or low-to-high transition). 0 No change-of-state since the CPU last read UIPCR n . Reading UIPCR n clears UISR n [COS]. 1 A change-of-state longer than 25–50 μ s occurred on the \overline{UnCTS} input. UACR n can be programmed to generate an interrupt to the CPU when a change of state is detected.
3–1	Reserved
0 CTS	Current state of clear-to-send. Starting two serial clock periods after reset, CTS reflects the state of \overline{UnCTS} . If \overline{UnCTS} is detected asserted at that time, COS is set, which initiates an interrupt if UACR n [IEC] is enabled. 0 The current state of the \overline{UnCTS} input is asserted. 1 The current state of the \overline{UnCTS} input is deasserted.

24.3.9 UART Auxiliary Control Register (UACR n)

The UACRs control the input enable.

Address: 0xFC06_0010 (UACR0)
0xFC06_4010 (UACR1)
0xFC06_8010 (UACR2)

Access: User write-only

	7	6	5	4	3	2	1	0
R								
W	0	0	0	0	0	0	0	IEC
Reset:	0	0	0	0	0	0	0	0

Figure 24-11. UART Auxiliary Control Registers (UACR n)Table 24-9. UACR n Field Descriptions

Field	Description
7–1	Reserved, must be cleared.
0 IEC	Input enable control. 0 Setting the corresponding UIPCR n bit has no effect on UISR n [COS]. 1 UISR n [COS] is set and an interrupt is generated when the UIPCR n [COS] is set by an external transition on the \overline{UnCTS} input (if UIMR n [COS] = 1).

24.3.10 UART Interrupt Status/Mask Registers (UISR n /UIMR n)

The UISRs provide status for all potential interrupt sources. UISR n contents are masked by UIMR n . If corresponding UISR n and UIMR n bits are set, internal interrupt output is asserted. If a UIMR n bit is cleared, state of the corresponding UISR n bit has no effect on the output.

The UISR n and UIMR n registers share the same space in memory. Reading this register provides the user with interrupt status, while writing controls the mask bits.

NOTE

True status is provided in the $UISR_n$ regardless of $UIMR_n$ settings. $UISR_n$ is cleared when the UART module is reset.

Address: 0xFC06_0014 ($UISR_0$)
 0xFC06_4014 ($UISR_1$)
 0xFC06_8014 ($UISR_2$)

Access: User read/write

	7	6	5	4	3	2	1	0
R ($UISR_n$)	COS	0	0	0	0	DB	FFULL/ RXRDY	TXRDY
W ($UIMR_n$)	COS	0	0	0	0	DB	FFULL/ RXRDY	TXRDY
Reset:	0	0	0	0	0	0	0	0

Figure 24-12. UART Interrupt Status/Mask Registers ($UISR_n/UIMR_n$)

Table 24-10. $UISR_n/UIMR_n$ Field Descriptions

Field	Description																						
7 COS	Change-of-state. 0 UIPCR n [COS] is not selected. 1 Change-of-state occurred on \overline{UnCTS} and was programmed in UACR n [IEC] to cause an interrupt.																						
6–3	Reserved, must be cleared.																						
2 DB	Delta break. 0 No new break-change condition to report. Section 24.3.5, “UART Command Registers (UCRn),” describes the RESET BREAK-CHANGE INTERRUPT command. 1 The receiver detected the beginning or end of a received break.																						
1 FFULL/ RXRDY	Status of FIFO or receiver, depending on UMR1[FFULL/RXRDY] bit. Duplicate of USR n [FIFO] and USR n [RXRDY] <table><tr><th rowspan="2">UIMRn [FFULL/RXRDY]</th><th rowspan="2">UISRn [FFULL/RXRDY]</th><th colspan="2">UMR1n[FFULL/RXRDY]</th></tr><tr><th>0 (RXRDY)</th><th>1 (FIFO)</th></tr><tr><td>0</td><td>0</td><td>Receiver not ready</td><td>FIFO not full</td></tr><tr><td>1</td><td>0</td><td>Receiver not ready</td><td>FIFO not full</td></tr><tr><td>0</td><td>1</td><td>Receiver is ready, Do not interrupt</td><td>FIFO is full, Do not interrupt</td></tr><tr><td>1</td><td>1</td><td>Receiver is ready, interrupt</td><td>FIFO is full, interrupt</td></tr></table>	UIMR n [FFULL/RXRDY]	UISR n [FFULL/RXRDY]	UMR1 n [FFULL/RXRDY]		0 (RXRDY)	1 (FIFO)	0	0	Receiver not ready	FIFO not full	1	0	Receiver not ready	FIFO not full	0	1	Receiver is ready, Do not interrupt	FIFO is full, Do not interrupt	1	1	Receiver is ready, interrupt	FIFO is full, interrupt
UIMR n [FFULL/RXRDY]	UISR n [FFULL/RXRDY]			UMR1 n [FFULL/RXRDY]																			
		0 (RXRDY)	1 (FIFO)																				
0	0	Receiver not ready	FIFO not full																				
1	0	Receiver not ready	FIFO not full																				
0	1	Receiver is ready, Do not interrupt	FIFO is full, Do not interrupt																				
1	1	Receiver is ready, interrupt	FIFO is full, interrupt																				
0 TXRDY	Transmitter ready. This bit is the duplication of USR n [TXRDY]. 0 The transmitter holding register was loaded by the CPU or the transmitter is disabled. Characters loaded into the transmitter holding register when TXRDY is cleared are not sent. 1 The transmitter holding register is empty and ready to be loaded with a character.																						

24.3.11 UART Baud Rate Generator Registers (UBG1 n /UBG2 n)

The UBG1 n registers hold the MSB, and the UBG2 n registers hold the LSB of the preload value. UBG1 n and UBG2 n concatenate to provide a divider to the internal bus clock for transmitter/receiver operation, as described in [Section 24.4.1.2.1, “Internal Bus Clock Baud Rates.”](#)

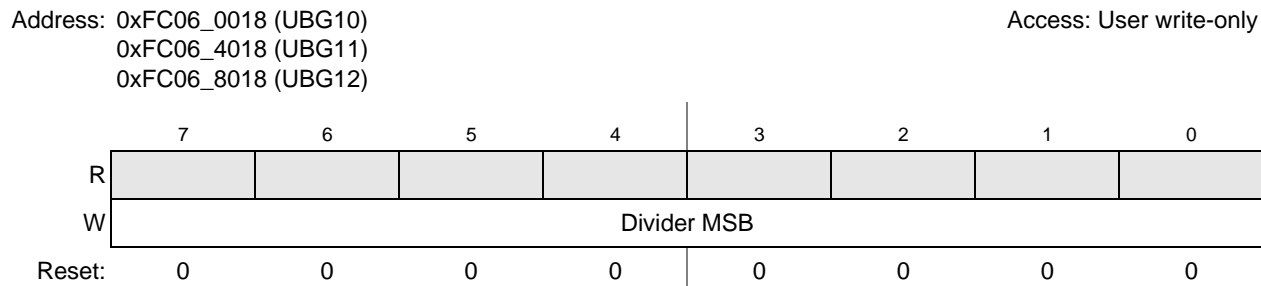


Figure 24-13. UART Baud Rate Generator Registers (UBG1 n)

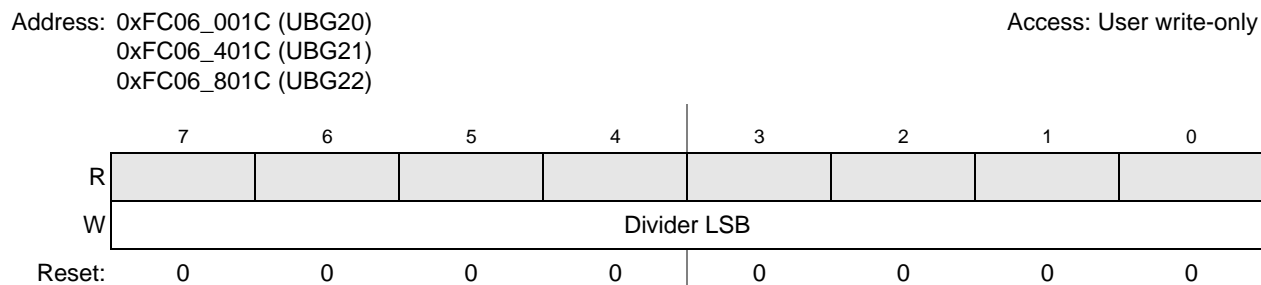


Figure 24-14. UART Baud Rate Generator Registers (UBG2 n)

NOTE

The minimum value loaded on the concatenation of UBG1 n with UBG2 n is 0x0002. The UBG2 n reset value of 0x00 is invalid and must be written to before the UART transmitter or receiver are enabled. UBG1 n and UBG2 n are write-only and cannot be read by the CPU.

24.3.12 UART Input Port Register (UIP n)

The UIP n registers show the current state of the \overline{UnCTS} input.

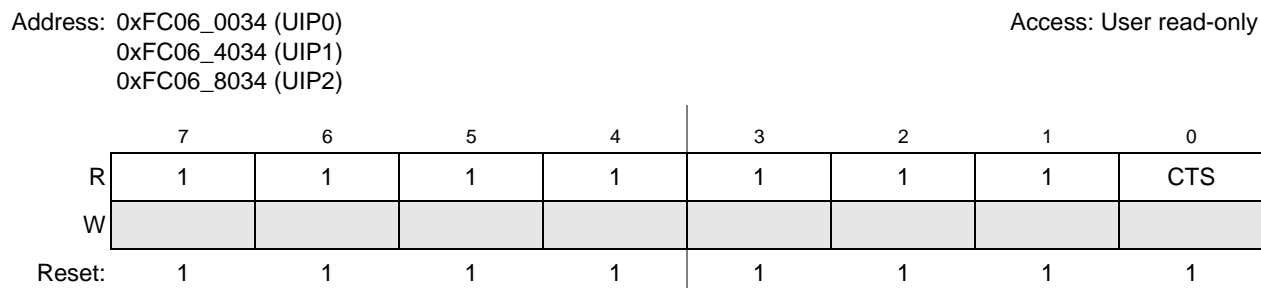


Figure 24-15. UART Input Port Registers (UIP n)

Table 24-11. UIP n Field Descriptions

Field	Description
7–1	Reserved
0 CTS	Current state of clear-to-send. The $\overline{U_nCTS}$ value is latched and reflects the state of the input pin when UIP n is read. Note: This bit has the same function and value as UIPCR n [CTS]. 0 The current state of the $\overline{U_nCTS}$ input is logic 0. 1 The current state of the $\overline{U_nCTS}$ input is logic 1.

24.3.13 UART Output Port Command Registers (UOP1 n /UOP0 n)

The $\overline{U_nRTS}$ output can be asserted by writing a 1 to UOP1 n [RTS] and negated by writing a 1 to UOP0 n [RTS].

Address: 0xFC06_0038 (UOP10)
 0xFC06_003C (UOP00)
 0xFC06_4038 (UOP11)
 0xFC06_403C (UOP01)
 0xFC06_8038 (UOP12)
 0xFC06_803C (UOP02)

Access: User write-only

	7	6	5	4	3	2	1	0
R								
W	0	0	0	0	0	0	0	RTS
Reset:	0	0	0	0	0	0	0	0

Figure 24-16. UART Output Port Command Registers (UOP1 n /UOP0 n)Table 24-12. UOP1 n /UOP0 n Field Descriptions

Field	Description
7–1	Reserved, must be cleared.
0 RTS	Output port output. Controls assertion (UOP1)/negation (UOP0) of $\overline{U_nRTS}$ output. 0 Not affected. 1 Asserts $\overline{U_nRTS}$ in UOP1. Negates $\overline{U_nRTS}$ in UOP0.

24.4 Functional Description

This section describes operation of the clock source generator, transmitter, and receiver.

24.4.1 Transmitter/Receiver Clock Source

The internal bus clock serves as the basic timing reference for the clock source generator logic, which consists of a clock generator and a programmable 16-bit divider dedicated to each UART. The 16-bit divider is used to produce standard UART baud rates.

24.4.1.1 Programmable Divider

As Figure 24-17 shows, the UART n transmitter and receiver can use the following clock sources:

- An external clock signal on the DT n IN pin. When not divided, DT n IN provides a synchronous clock; when divided by 16, it is asynchronous.
- The internal bus clock supplies an asynchronous clock source divided by 32 and then divided by the 16-bit value programmed in UBG1 n and UBG2 n . See Section 24.3.11, “UART Baud Rate Generator Registers (UBG1 n /UBG2 n).”

The choice of DTIN or internal bus clock is programmed in the UCSR.

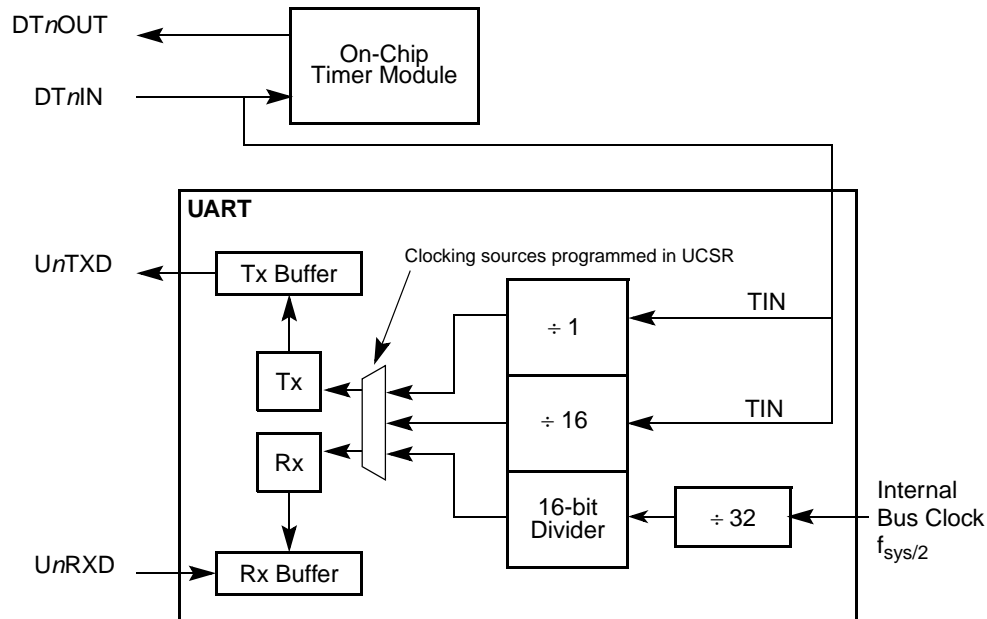


Figure 24-17. Clocking Source Diagram

NOTE

If DT n IN is a clocking source for the timer or UART, that timer module cannot use DT n IN for timer input capture.

24.4.1.2 Calculating Baud Rates

The following sections describe how to calculate baud rates.

24.4.1.2.1 Internal Bus Clock Baud Rates

When the internal bus clock is the UART clocking source, it goes through a divide-by-32 prescaler and then passes through the 16-bit divider of the concatenated UBG1 n and UBG2 n registers. The baud-rate calculation is:

$$\text{Baudrate} = \frac{f_{\text{sys}/2}}{[32 \times \text{divider}]} \quad \text{Eqn. 24-1}$$

Using a 83-MHz internal bus clock and letting baud rate equal 9600, then

$$\text{Divider} = \frac{83\text{MHz}}{[32 \times 9600]} = 270(\text{decimal}) = 0x010E(\text{hexadecimal}) \quad \text{Eqn. 24-2}$$

Therefore, UBG1n equals 0x01 and UBG2n equals 0x0E.

24.4.1.2.2 External Clock

An external source clock (DTnIN) passes through a divide-by-1 or 16 prescaler. If f_{extc} is the external clock frequency, baud rate can be described with this equation:

$$\text{Baudrate} = \frac{f_{\text{extc}}}{(16 \text{ or } 1)} \quad \text{Eqn. 24-3}$$

24.4.2 Transmitter and Receiver Operating Modes

Figure 24-18 is a functional block diagram of the transmitter and receiver showing the command and operating registers, which are described generally in the following sections. For detailed descriptions, refer to Section 24.3, “Memory Map/Register Definition.”

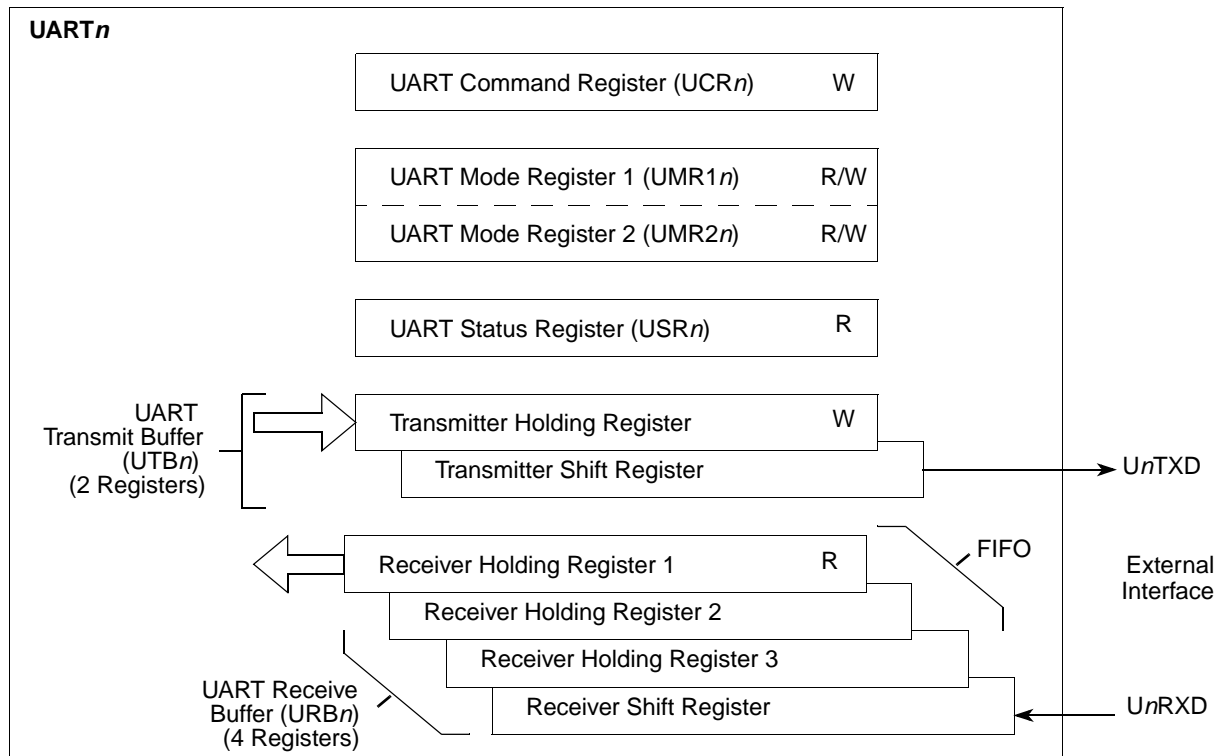


Figure 24-18. Transmitter and Receiver Functional Diagram

24.4.2.1 Transmitter

The transmitter is enabled through the UART command register (UCRn). When it is ready to accept a character, UART sets USRn[TXRDY]. The transmitter converts parallel data from the CPU to a serial bit stream on UnTXD. It automatically sends a start bit followed by the programmed number of data bits, an

optional parity bit, and the programmed number of stop bits. The lsb is sent first. Data is shifted from the transmitter output on the falling edge of the clock source.

After the stop bits are sent, if no new character is in the transmitter holding register, the $UnTXD$ output remains high (mark condition) and the transmitter empty bit ($USRn[TXEMP]$) is set. Transmission resumes and $TXEMP$ is cleared when the CPU loads a new character into the UART transmit buffer ($UTBn$). If the transmitter receives a disable command, it continues until any character in the transmitter shift register is completely sent.

If the transmitter is reset through a software command, operation stops immediately (see [Section 24.3.5, “UART Command Registers \(UCRn\)”](#)). The transmitter is reenabled through the $UCRn$ to resume operation after a disable or software reset.

If the clear-to-send operation is enabled, \overline{UnCTS} must be asserted for the character to be transmitted. If \overline{UnCTS} is negated in the middle of a transmission, the character in the shift register is sent and $UnTXD$ remains in mark state until \overline{UnCTS} is reasserted. If transmitter is forced to send a continuous low condition by issuing a SEND BREAK command, transmitter ignores the state of \overline{UnCTS} .

If the transmitter is programmed to automatically negate \overline{UnRTS} when a message transmission completes, \overline{UnRTS} must be asserted manually before a message is sent. In applications in which the transmitter is disabled after transmission is complete and \overline{UnRTS} is appropriately programmed, \overline{UnRTS} is negated one bit time after the character in the shift register is completely transmitted. The transmitter must be manually reenabled by reasserting \overline{UnRTS} before the next message is sent.

[Figure 24-19](#) shows the functional timing information for the transmitter.

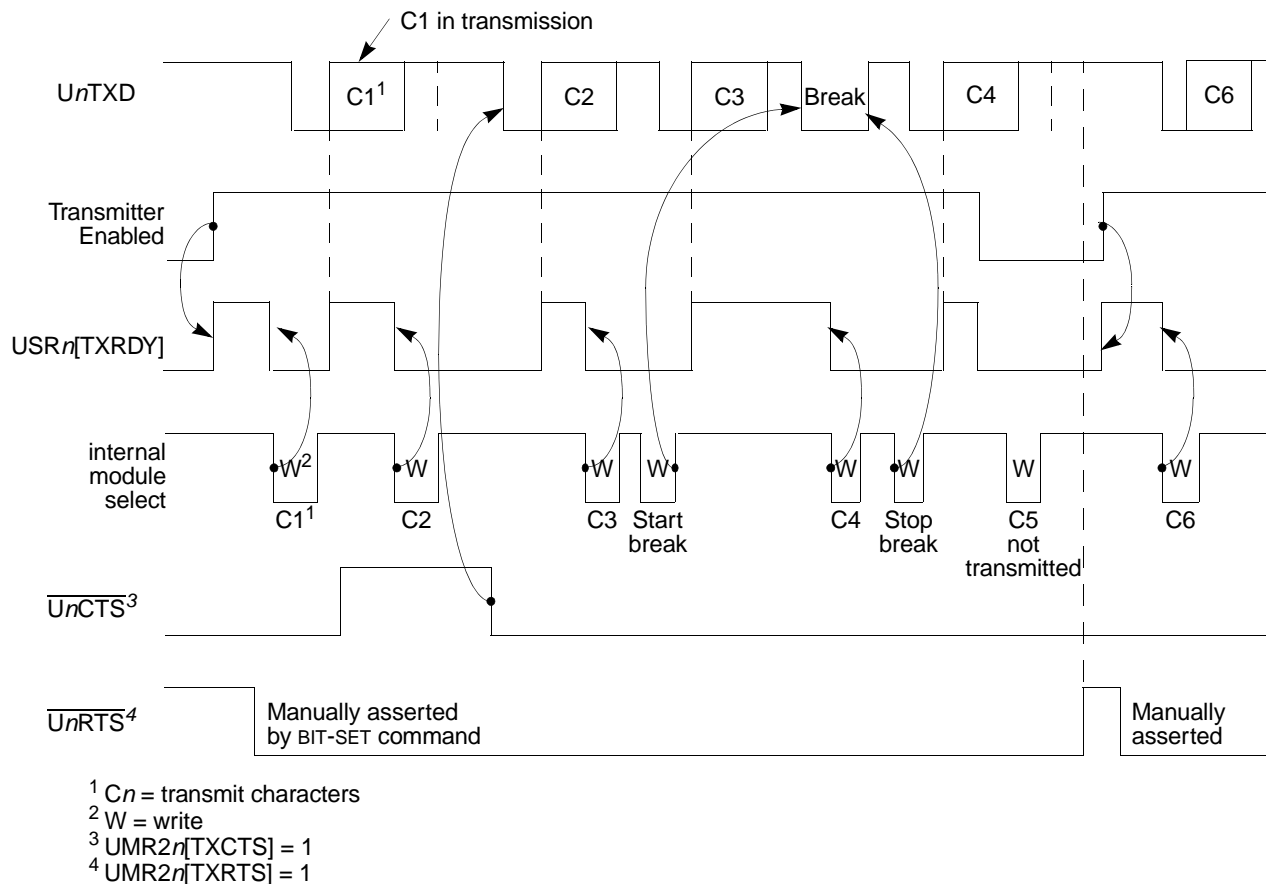


Figure 24-19. Transmitter Timing Diagram

24.4.2.2 Receiver

The receiver is enabled through its UCR_n , as described in [Section 24.3.5, “UART Command Registers \(UCRn\).”](#)

When the receiver detects a high-to-low (mark-to-space) transition of the start bit on $UnRXD$, the state of $UnRXD$ is sampled eight times on the edge of the bit time clock starting one-half clock after the transition (asynchronous operation) or at the next rising edge of the bit time clock (synchronous operation). If $UnRXD$ is sampled high, start bit is invalid and the search for the valid start bit begins again.

If $UnRXD$ remains low, a valid start bit is assumed. The receiver continues sampling the input at one-bit time intervals at the theoretical center of the bit until the proper number of data bits and parity, if any, is assembled and one stop bit is detected. Data on the $UnRXD$ input is sampled on the rising edge of the programmed clock source. The lsb is received first. The data then transfers to a receiver holding register and $USR_n[RXRDY]$ is set. If the character is less than 8 bits, the most significant unused bits in the receiver holding register are cleared.

After the stop bit is detected, receiver immediately looks for the next start bit. However, if a non-zero character is received without a stop bit (framing error) and $UnRXD$ remains low for one-half of the bit period after the stop bit is sampled, receiver operates as if a new start bit were detected. Parity error,

framing error, overrun error, and received break conditions set the respective PE, FE, OE, and RB error and break flags in the USR_n at the received character boundary. They are valid only if $USR_n[RXRDY]$ is set.

If a break condition is detected ($UnRXD$ is low for the entire character including the stop bit), a character of all 0s loads into the receiver holding register and $USR_n[RB,RXRDY]$ are set. $UnRXD$ must return to a high condition for at least one-half bit time before a search for the next start bit begins.

The receiver detects the beginning of a break in the middle of a character if the break persists through the next character time. If the break begins in the middle of a character, receiver places the damaged character in the Rx FIFO and sets the corresponding USR_n error bits and $USR_n[RXRDY]$. Then, if the break lasts until the next character time, receiver places an all-zero character into the Rx FIFO and sets $USR_n[RB,RXRDY]$.

Figure 24-20 shows receiver functional timing.

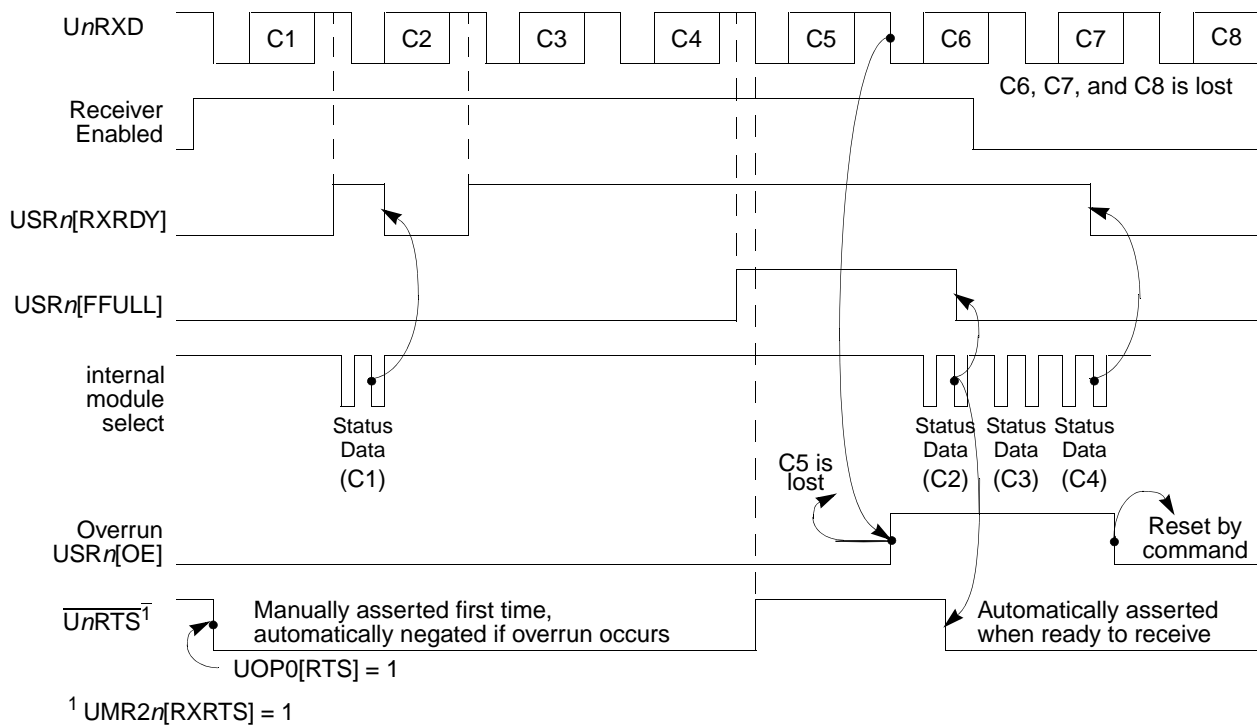


Figure 24-20. Receiver Timing Diagram

24.4.2.3 FIFO

The FIFO is used in the UART's receive buffer logic. The FIFO consists of three receiver holding registers. The receive buffer consists of the FIFO and a receiver shift register connected to the $UnRXD$ (see Figure 24-18). Data is assembled in the receiver shift register and loaded into the top empty receiver holding register position of the FIFO. Therefore, data flowing from the receiver to the CPU is quadruple-buffered.

In addition to the data byte, three status bits—parity error (PE), framing error (FE), and received break (RB)—are appended to each data character in the FIFO; overrun error (OE) is not appended. By

programming the ERR bit in the UART's mode register (UMR1*n*), status is provided in character or block modes.

USR*n*[RXRDY] is set when at least one character is available to be read by the CPU. A read of the receive buffer produces an output of data from the top of the FIFO. After the read cycle, the data at the top of the FIFO and its associated status bits are popped and the receiver shift register can add new data at the bottom of the FIFO. The FIFO-full status bit (FFULL) is set if all three positions are filled with data. The RXRDY or FFULL bit can be selected to cause an interrupt and TXRDY or RXRDY can be used to generate a DMA request.

The two error modes are selected by UMR1*n*[ERR]:

- In character mode (UMR1*n*[ERR] = 0), status is given in the USR*n* for the character at the top of the FIFO.
- In block mode, the USR*n* shows a logical OR of all characters reaching the top of the FIFO since the last RESET ERROR STATUS command. Status is updated as characters reach the top of the FIFO. Block mode offers a data-reception speed advantage where the software overhead of error-checking each character cannot be tolerated. However, errors are not detected until the check is performed at the end of an entire message—the faulting character is not identified.

In either mode, reading the USR*n* does not affect the FIFO. The FIFO is popped only when the receive buffer is read. The USR*n* should be read before reading the receive buffer. If all three receiver holding registers are full, a new character is held in the receiver shift register until space is available. However, if a second new character is received, the contents of the character in the receiver shift register is lost, the FIFOs are unaffected, and USR*n*[OE] is set when the receiver detects the start bit of the new overrunning character.

To support flow control, the receiver can be programmed to automatically negate and assert \overline{UnRTS} , in which case the receiver automatically negates \overline{UnRTS} when a valid start bit is detected and the FIFO is full. The receiver asserts \overline{UnRTS} when a FIFO position becomes available; therefore, connecting \overline{UnRTS} to the $UnCTS$ input of the transmitting device can prevent overrun errors.

NOTE

The receiver continues reading characters in the FIFO if the receiver is disabled. If the receiver is reset, the FIFO, \overline{UnRTS} control, all receiver status bits, interrupts, and DMA requests are reset. No more characters are received until the receiver is reenabled.

24.4.3 Looping Modes

The UART can be configured to operate in various looping modes. These modes are useful for local and remote system diagnostic functions. The modes are described in the following paragraphs and in [Section 24.3, “Memory Map/Register Definition.”](#)

The UART's transmitter and receiver should be disabled when switching between modes. The selected mode is activated immediately upon mode selection, regardless of whether a character is being received or transmitted.

24.4.3.1 Automatic Echo Mode

In automatic echo mode, shown in Figure 24-21, the UART automatically resends received data bit by bit. The local CPU-to-receiver communication continues normally, but the CPU-to-transmitter link is disabled. In this mode, received data is clocked on the receiver clock and re-sent on $UnTXD$. The receiver must be enabled, but the transmitter need not be.

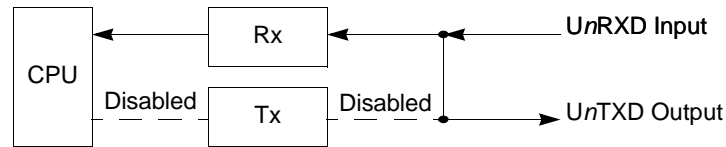


Figure 24-21. Automatic Echo

Because the transmitter is inactive, $USR_n[TXEMP, TXRDY]$ is inactive and data is sent as it is received. Received parity is checked but not recalculated for transmission. Character framing is also checked, but stop bits are sent as they are received. A received break is echoed as received until the next valid start bit is detected.

24.4.3.2 Local Loopback Mode

Figure 24-22 shows how $UnTXD$ and $UnRXD$ are internally connected in local loopback mode. This mode is for testing the operation of a UART by sending data to the transmitter and checking data assembled by the receiver to ensure proper operations.

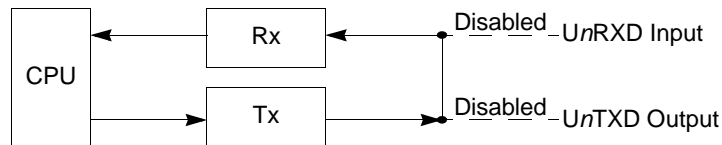


Figure 24-22. Local Loopback

Features of this local loopback mode are:

- Transmitter and CPU-to-receiver communications continue normally in this mode.
- $UnRXD$ input data is ignored.
- $UnTXD$ is held marking.
- The receiver is clocked by the transmitter clock. The transmitter must be enabled, but the receiver need not be.

24.4.3.3 Remote Loopback Mode

In remote loopback mode, shown in Figure 24-23, the UART automatically transmits received data bit by bit on the $UnTXD$ output. The local CPU-to-transmitter link is disabled. This mode is useful in testing receiver and transmitter operation of a remote UART. For this mode, transmitter uses the receiver clock.

Because the receiver is not active, received data cannot be read by the CPU and all status conditions are inactive. Received parity is not checked and is not recalculated for transmission. Stop bits are sent as they are received. A received break is echoed as received until next valid start bit is detected.

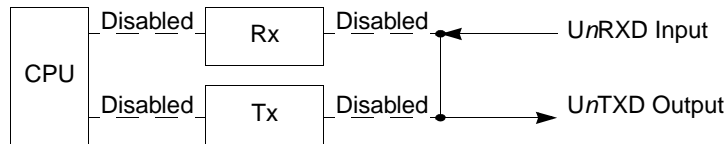


Figure 24-23. Remote Loopback

24.4.4 Multidrop Mode

Setting $UMR1n[PM]$ programs the UART to operate in a wake-up mode for multidrop or multiprocessor applications. In this mode, a master can transmit an address character followed by a block of data characters targeted for one of up to 256 slave stations.

Although slave stations have their receivers disabled, they continuously monitor the master's data stream. When the master sends an address character, the slave receiver notifies its respective CPU by setting $USRn[RXRDY]$ and generating an interrupt (if programmed to do so). Each slave station CPU then compares the received address to its station address and enables its receiver if it wishes to receive the subsequent data characters or block of data from the master station. Unaddressed slave stations continue monitoring the data stream. Data fields in the data stream are separated by an address character. After a slave receives a block of data, its CPU disables the receiver and repeats the process. Functional timing information for multidrop mode is shown in [Figure 24-24](#).

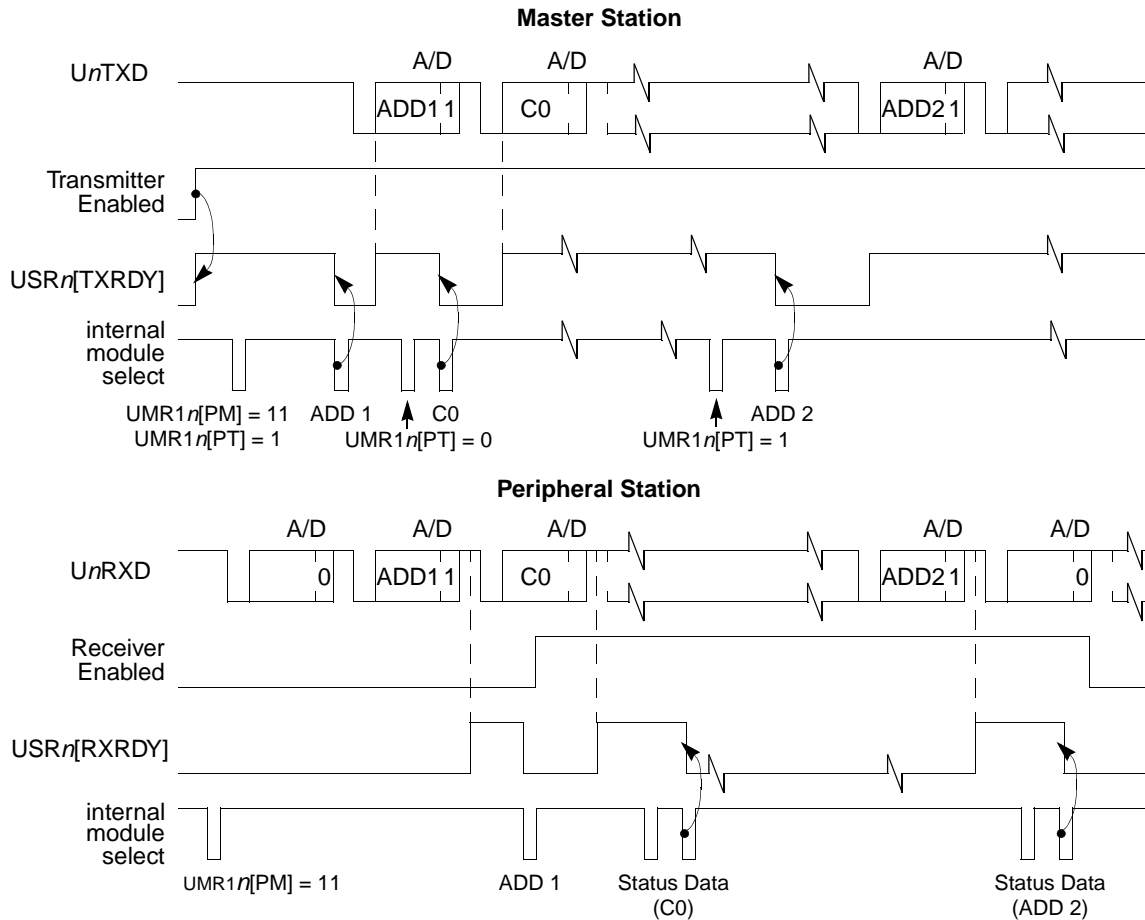


Figure 24-24. Multidrop Mode Timing Diagram

A character sent from the master station consists of a start bit, a programmed number of data bits, an address/data (A/D) bit flag, and a programmed number of stop bits. A/D equals 1 indicates an address character; A/D equals 0 indicates a data character. The polarity of A/D is selected through UMR1n[PT]. UMR1n should be programmed before enabling the transmitter and loading the corresponding data bits into the transmit buffer.

In multidrop mode, the receiver continuously monitors the received data stream, regardless of whether it is enabled or disabled. If the receiver is disabled, it sets the RXRDY bit and loads the character into the receiver holding register FIFO provided the received A/D bit is a 1 (address tag). The character is discarded if the received A/D bit is 0 (data tag). If the receiver is enabled, all received characters are transferred to the CPU through the receiver holding register during read operations.

In either case, data bits load into the data portion of the FIFO while the A/D bit loads into the status portion of the FIFO normally used for a parity error (USRn[PE]).

Framing error, overrun error, and break detection operate normally. The A/D bit takes the place of the parity bit; therefore, parity is neither calculated nor checked. Messages in this mode may continue containing error detection and correction information. If 8-bit characters are not required, one way to provide error detection is to use software to calculate parity and append it to the 5-, 6-, or 7-bit character.

24.4.5 Bus Operation

This section describes bus operation during read, write, and interrupt acknowledge cycles to the UART module.

24.4.5.1 Read Cycles

The UART module responds to reads with byte data. Reserved registers return zeros.

24.4.5.2 Write Cycles

The UART module accepts write data as bytes only. Write cycles to read-only or reserved registers complete normally without an error termination, but data is ignored.

24.5 Initialization/Application Information

The software flowchart, [Figure 24-25](#), consists of:

- UART module initialization—These routines consist of SINIT and CHCHK (See Sheet 1 p. 24-29 and Sheet 2 p. 24-30). Before SINIT is called at system initialization, the calling routine allocates 2 words on the system FIFO. On return to the calling routine, SINIT passes UART status data on the FIFO. If SINIT finds no errors, the transmitter and receiver are enabled. SINIT calls CHCHK to perform the checks. When called, SINIT places the UART in local loopback mode and checks for the following errors:
 - Transmitter never ready
 - Receiver never ready
 - Parity error
 - Incorrect character received
- I/O driver routine—This routine (See Sheet 4 p. 24-32 and Sheet 5 p. 24-33) consists of INCH, the terminal input character routine which gets a character from the receiver, and OUTCH, which sends a character to the transmitter.
- Interrupt handling—This consists of SIRQ (See Sheet 4 p. 24-32), which is executed after the UART module generates an interrupt caused by a change-in-break (beginning of a break). SIRQ then clears the interrupt source, waits for the next change-in-break interrupt (end of break), clears the interrupt source again, then returns from exception processing to the system monitor.

24.5.1 Interrupt and DMA Request Initialization

24.5.1.1 Setting up the UART to Generate Core Interrupts

The list below provides steps to properly initialize the UART to generate an interrupt request to the processor's interrupt controller. See [Section 14.2.9.1, "Interrupt Sources,"](#) for details on interrupt assignments for the UART modules.

1. Initialize the appropriate ICRx register in the interrupt controller.
2. Unmask appropriate bits in IMR in the interrupt controller.

3. Unmask appropriate bits in the core's status register (SR) to enable interrupts.
4. If TXRDY or RXRDY generates interrupt requests, verify that the corresponding UART DMA channels are not enabled.
5. Initialize interrupts in the UART, see [Table 24-13](#).

Table 24-13. UART Interrupts

Register	Bit	Interrupt
UMR1 <i>n</i>	6	RxIRQ
UIMR <i>n</i>	7	Change of State (COS)
UIMR <i>n</i>	2	Delta Break
UIMR <i>n</i>	1	RxFIFO Full
UIMR <i>n</i>	0	TXRDY

24.5.1.2 Setting up the UART to Request DMA Service

The UART is capable of generating two internal DMA request signals: transmit and receive.

The transmit DMA request signal is asserted when the TXRDY (transmitter ready) in the UART interrupt status register (UISR*n*[TXRDY]) is set. When the transmit DMA request signal is asserted, the DMA can initiate a data copy, reading the next character transmitted from memory and writing it into the UART transmit buffer (UTB*n*). This allows the DMA channel to stream data from memory to the UART for transmission without processor intervention. After the entire message has been moved into the UART, the DMA would typically generate an end-of-data-transfer interrupt request to the CPU. The resulting interrupt service routine (ISR) could query the UART programming model to determine the end-of-transmission status.

Similarly, the receive DMA request signal is asserted when the FIFO full or receive ready (FFULL/RXRDY) flag in the interrupt status register (UISR*n*[FFULL/RXRDY]) is set. When the receive DMA request signal is asserted, the DMA can initiate a data move, reading the appropriate characters from the UART receive buffer (URB*n*) and storing them in memory. This allows the DMA channel to stream data from the UART receive buffer into memory without processor intervention. After the entire message has been moved from the UART, the DMA would typically generate an end-of-data-transfer interrupt request to the CPU. The resulting interrupt service routine (ISR) should query the UART programming model to determine the end-of-transmission status. In typical applications, the receive DMA request should be configured to use RXRDY directly (and not FFULL) to remove any complications related to retrieving the final characters from the FIFO buffer.

The implementation described in this section allows independent DMA processing of transmit and receive data while continuing to support interrupt notification to the processor for $\overline{\text{CTS}}$ change-of-state and delta break error managing.

[Table 24-14](#) shows the DMA requests.

Table 24-14. UART DMA Requests

Register	Bit	DMA Request
UISR n	1	Receive DMA request
UISR n	0	Transmit DMA request

24.5.2 UART Module Initialization Sequence

The following shows the UART module initialization sequence.

1. UCR n :
 - a) Reset the receiver and transmitter.
 - b) Reset the mode pointer (MISC[2–0] = 0b001).
2. UIMR n : Enable the desired interrupt sources.
3. UACR n : Initialize the input enable control (IEC bit).
4. UCSR n : Select the receiver and transmitter clock. Use timer as source if required.
5. UMR1 n :
 - a) If preferred, program operation of receiver ready-to-send (RXRTS bit).
 - a) Select receiver-ready or FIFO-full notification (RXRDY/FFULL bit).
 - b) Select character or block error mode (ERR bit).
 - c) Select parity mode and type (PM and PT bits).
 - d) Select number of bits per character (B/Cx bits).
6. UMR2 n :
 - a) Select the mode of operation (CM bits).
 - b) If preferred, program operation of transmitter ready-to-send (TXRTS).
 - c) If preferred, program operation of clear-to-send (TXCTS bit).
 - d) Select stop-bit length (SB bits).
7. UCR n : Enable transmitter and/or receiver.

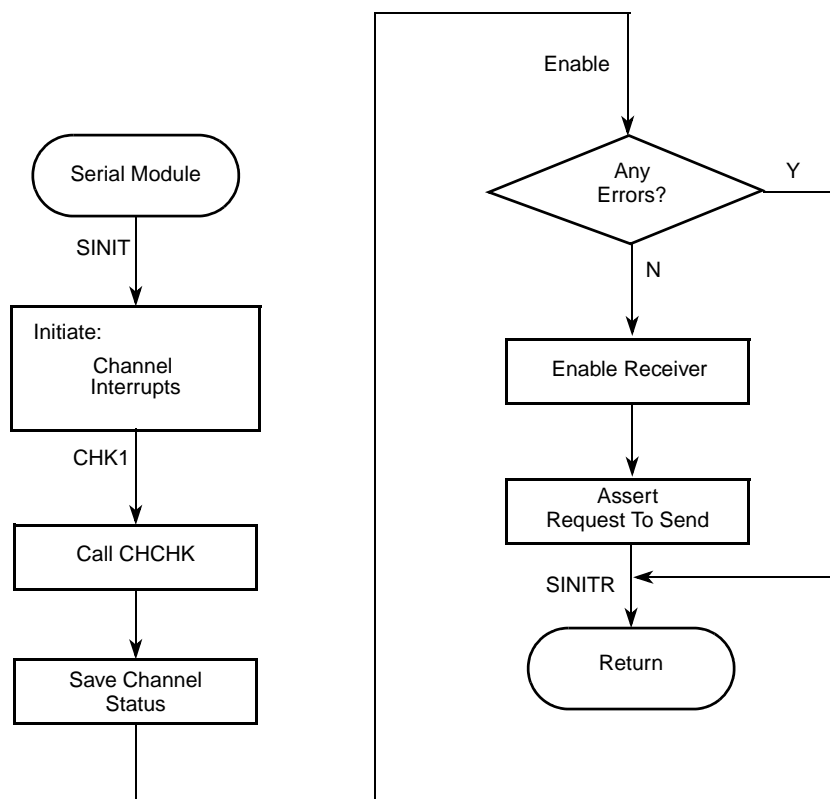


Figure 24-25. UART Mode Programming Flowchart (Sheet 1 of 5)

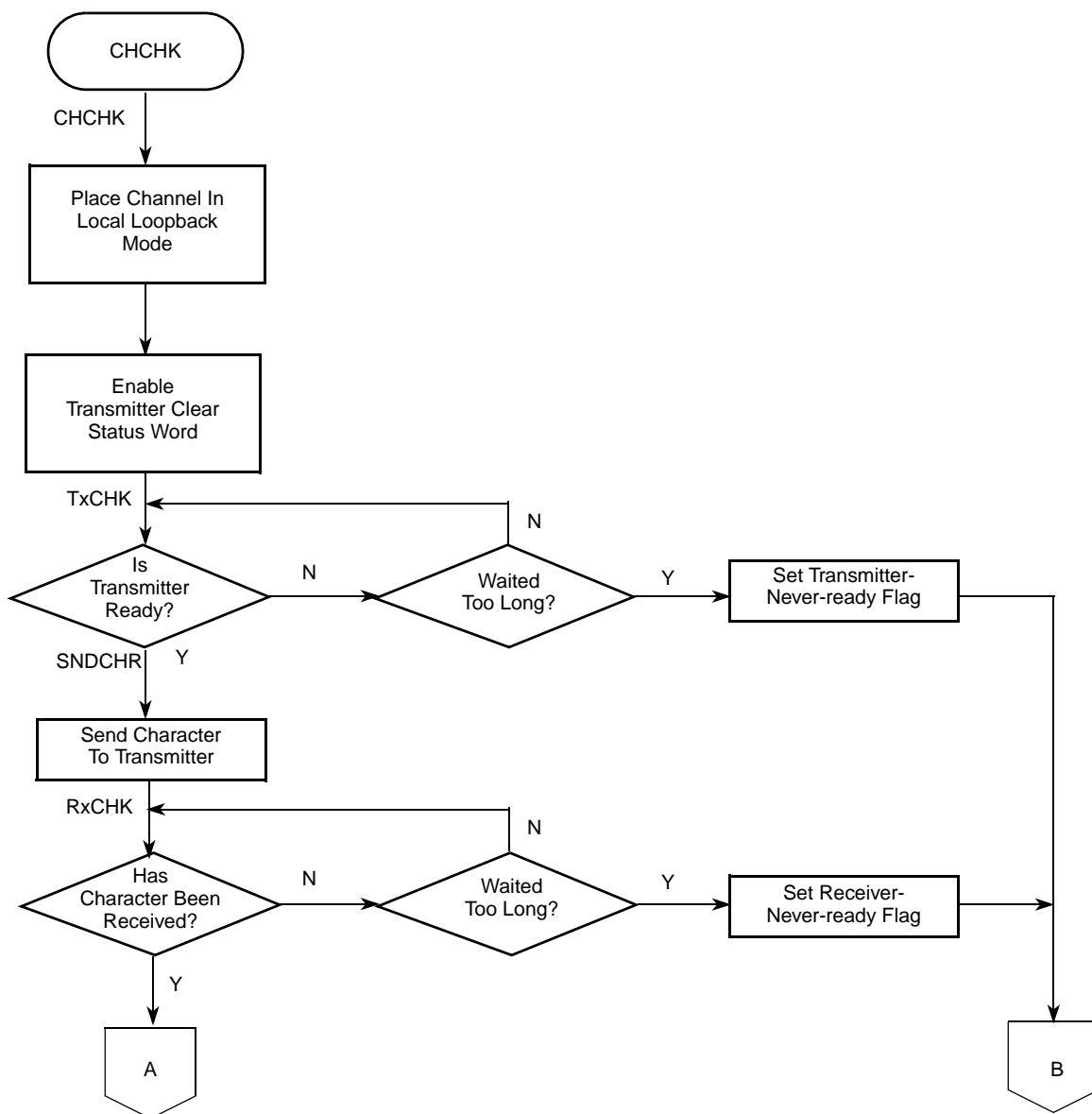


Figure 24-25. UART Mode Programming Flowchart (Sheet 2 of 5)

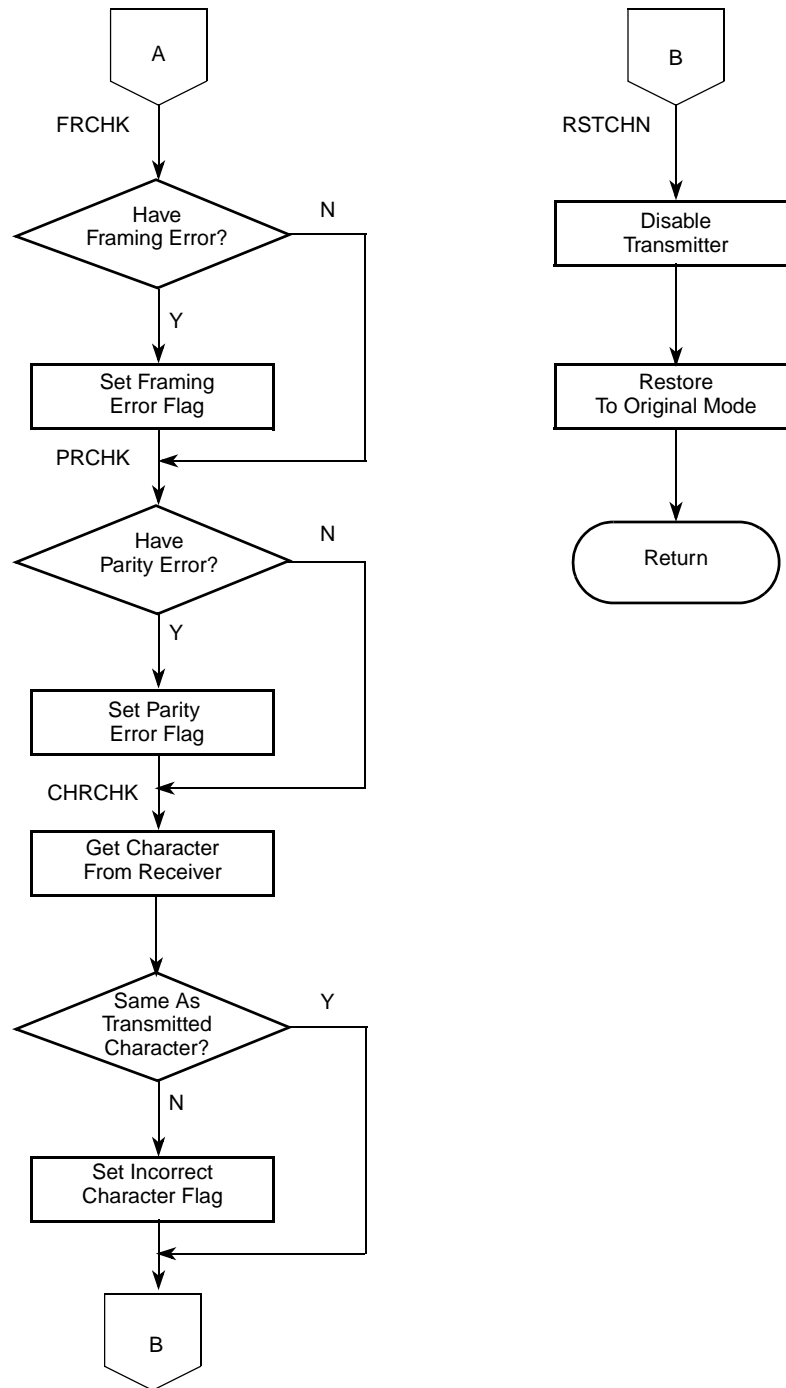


Figure 24-25. UART Mode Programming Flowchart (Sheet 3 of 5)

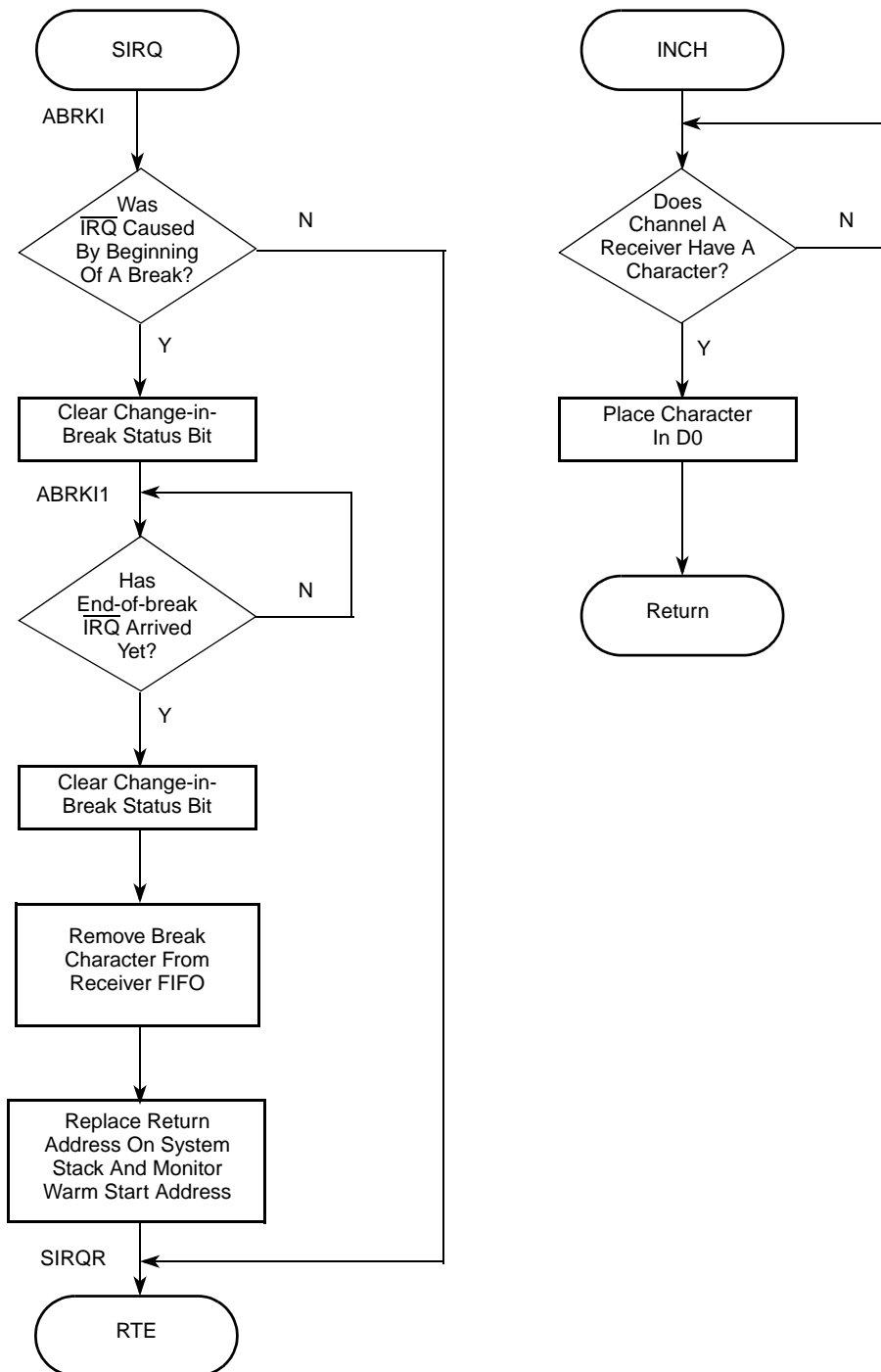


Figure 24-25. UART Mode Programming Flowchart (Sheet 4 of 5)

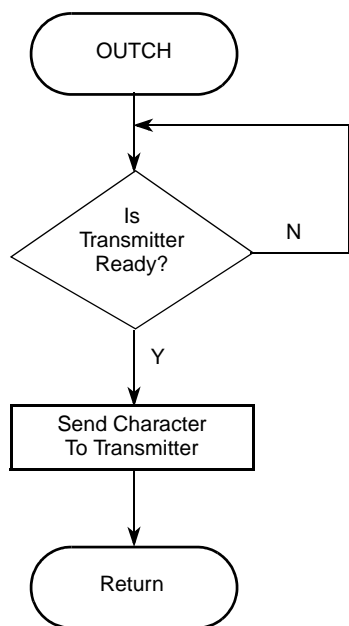


Figure 24-25. UART Mode Programming Flowchart (Sheet 5 of 5)

Chapter 25

I²C Interface

25.1 Introduction

This chapter describes the I²C module, clock synchronization, and I²C programming model registers. It also provides extensive programming examples.

25.1.1 Block Diagram

Figure 25-1 is a I²C module block diagram, illustrating the interaction of the registers described in Section 25.2, “Memory Map/Register Definition”.

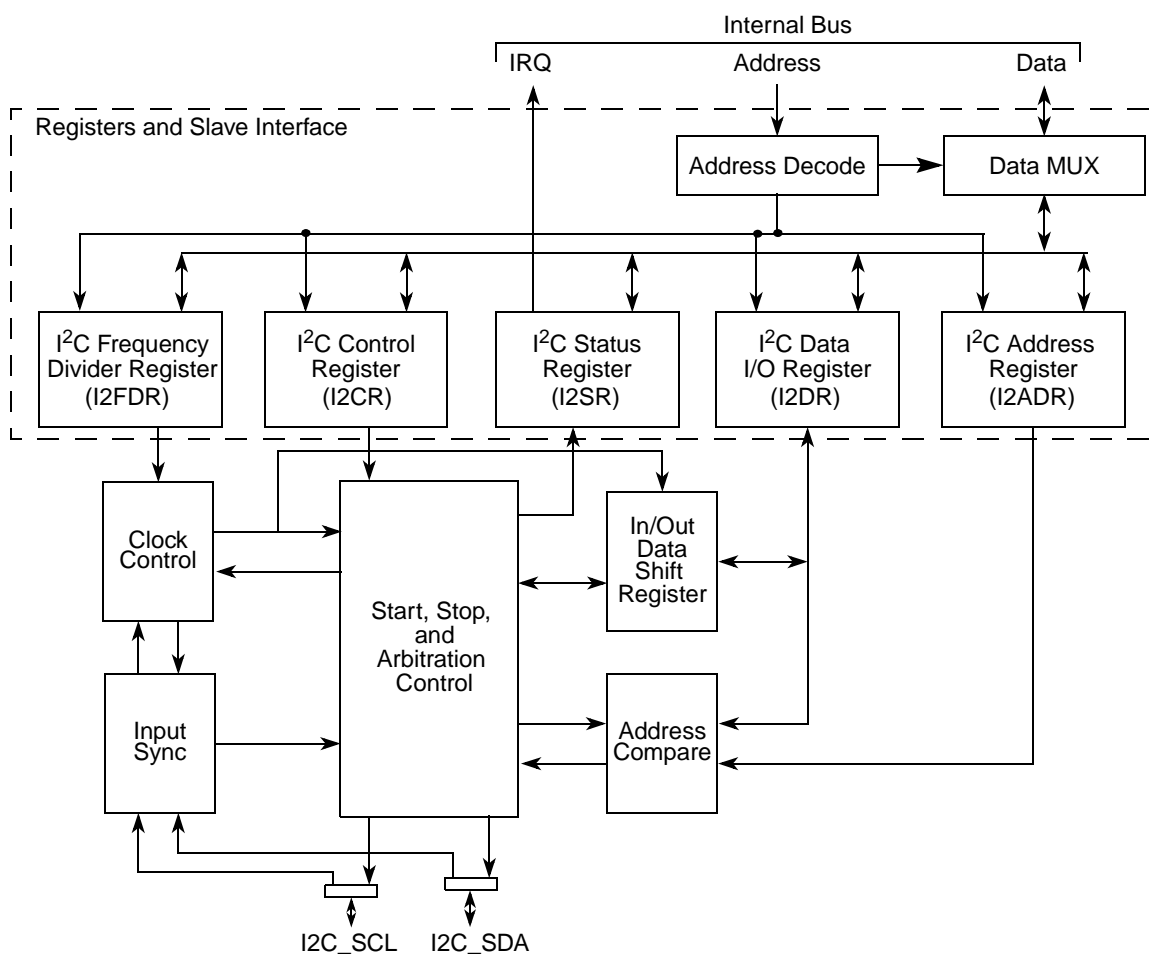


Figure 25-1. I²C Module Block Diagram

25.1.2 Overview

I²C is a two-wire, bidirectional serial bus that provides a simple, efficient method of data exchange, minimizing the interconnection between devices. This bus is suitable for applications that require occasional communication between many devices over a short distance. The flexible I²C bus allows additional devices to connect to the bus for expansion and system development.

The interface operates up to 100 Kbps with maximum bus loading and timing. The device is capable of operating at higher baud rates, up to a maximum of the internal bus clock divided by 20, with reduced bus loading. The maximum communication length and the number of devices connected are limited by a maximum bus capacitance of 400 pF.

The I²C system is a true multiple-master bus; it uses arbitration and collision detection to prevent data corruption in the event that multiple devices attempt to control the bus simultaneously. This feature supports complex applications with multiprocessor control and can be used for rapid testing and alignment of end products through external connections to an assembly-line computer.

NOTE

The I²C module is compatible with the Philips I²C bus protocol. For information on system configuration, protocol, and restrictions, see *The I²C Bus Specification, Version 2.1*.

NOTE

The GPIO module must be configured to enable the peripheral function of the appropriate pins (refer to [Chapter 13, “General Purpose I/O Module”](#)) prior to configuring the I²C module.

25.1.3 Features

The I²C module has these key features:

- Compatibility with I²C bus standard version 2.1
- Support for 3.3-V tolerant devices
- Multiple-master operation
- Software-programmable for one of 50 different serial clock frequencies
- Software-selectable acknowledge bit
- Interrupt-driven, byte-by-byte data transfer
- Arbitration-lost interrupt with automatic mode switching from master to slave
- Calling address identification interrupt
- START and STOP signal generation/detection
- Repeated START signal generation
- Acknowledge bit generation/detection
- Bus-busy detection

25.2 Memory Map/Register Definition

The below table lists the configuration registers used in the I²C interface.

Table 25-1. I²C Module Memory Map

Address	Register	Access	Reset Value	Section/Page
0xFC05_8000	I ² C Address Register (I2ADR)	R/W	0x00	25.2.1/25-3
0xFC05_8004	I ² C Frequency Divider Register (I2FDR)	R/W	0x00	25.2.2/25-3
0xFC05_8008	I ² C Control Register (I2CR)	R/W	0x00	25.2.3/25-4
0xFC05_800C	I ² C Status Register (I2SR)	R/W	0x81	25.2.4/25-5
0xFC05_8010	I ² C Data I/O Register (I2DR)	R/W	0x00	25.2.5/25-6

25.2.1 I²C Address Register (I2ADR)

I2ADR holds the address the I²C responds to when addressed as a slave. It is not the address sent on the bus during the address transfer when the module is performing a master transfer.

Address: 0xFC05_8000 (I2ADR)

Access: User read/write

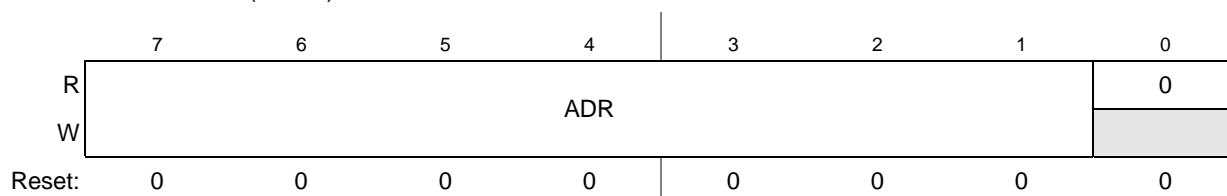


Figure 25-2. I²C Address Register (I2ADR)

Table 25-2. I2ADR Field Descriptions

Field	Description
7–1 ADR	Slave address. Contains the specific slave address to be used by the I ² C module. Slave mode is the default I ² C mode for an address match on the bus.
0	Reserved, must be cleared.

25.2.2 I²C Frequency Divider Register (I2FDR)

The I2FDR, shown in [Figure 25-3](#), provides a programmable prescaler to configure the I²C clock for bit-rate selection.

Address: 0xFC05_8004 (I2FDR)

Access: User read/write



Figure 25-3. I²C Frequency Divider Register (I2FDR)

Table 25-3. I2FDR Field Descriptions

Field	Description																																																																																																																																								
7–6	Reserved, must be cleared.																																																																																																																																								
5–0 IC	<p>I²C clock rate. Prescales the clock for bit-rate selection. The serial bit clock frequency is equal to the internal bus clock divided by the divider shown below. Due to potentially slow I2C_SCL and I2C_SDA rise and fall times, bus signals are sampled at the prescaler frequency.</p> <table><tr><th>IC</th><th>Divider</th><th>IC</th><th>Divider</th><th>IC</th><th>Divider</th><th>IC</th><th>Divider</th></tr><tr><td>0x00</td><td>28</td><td>0x10</td><td>288</td><td>0x20</td><td>20</td><td>0x30</td><td>160</td></tr><tr><td>0x01</td><td>30</td><td>0x11</td><td>320</td><td>0x21</td><td>22</td><td>0x31</td><td>192</td></tr><tr><td>0x02</td><td>34</td><td>0x12</td><td>384</td><td>0x22</td><td>24</td><td>0x32</td><td>224</td></tr><tr><td>0x03</td><td>40</td><td>0x13</td><td>480</td><td>0x23</td><td>26</td><td>0x33</td><td>256</td></tr><tr><td>0x04</td><td>44</td><td>0x14</td><td>576</td><td>0x24</td><td>28</td><td>0x34</td><td>320</td></tr><tr><td>0x05</td><td>48</td><td>0x15</td><td>640</td><td>0x25</td><td>32</td><td>0x35</td><td>384</td></tr><tr><td>0x06</td><td>56</td><td>0x16</td><td>768</td><td>0x26</td><td>36</td><td>0x36</td><td>448</td></tr><tr><td>0x07</td><td>68</td><td>0x17</td><td>960</td><td>0x27</td><td>40</td><td>0x37</td><td>512</td></tr><tr><td>0x08</td><td>80</td><td>0x18</td><td>1152</td><td>0x28</td><td>48</td><td>0x38</td><td>640</td></tr><tr><td>0x09</td><td>88</td><td>0x19</td><td>1280</td><td>0x29</td><td>56</td><td>0x39</td><td>768</td></tr><tr><td>0x0A</td><td>104</td><td>0x1A</td><td>1536</td><td>0x2A</td><td>64</td><td>0x3A</td><td>896</td></tr><tr><td>0x0B</td><td>128</td><td>0x1B</td><td>1920</td><td>0x2B</td><td>72</td><td>0x3B</td><td>1024</td></tr><tr><td>0x0C</td><td>144</td><td>0x1C</td><td>2304</td><td>0x2C</td><td>80</td><td>0x3C</td><td>1280</td></tr><tr><td>0x0D</td><td>160</td><td>0x1D</td><td>2560</td><td>0x2D</td><td>96</td><td>0x3D</td><td>1536</td></tr><tr><td>0x0E</td><td>192</td><td>0x1E</td><td>3072</td><td>0x2E</td><td>112</td><td>0x3E</td><td>1792</td></tr><tr><td>0x0F</td><td>240</td><td>0x1F</td><td>3840</td><td>0x2F</td><td>128</td><td>0x3F</td><td>2048</td></tr></table>	IC	Divider	IC	Divider	IC	Divider	IC	Divider	0x00	28	0x10	288	0x20	20	0x30	160	0x01	30	0x11	320	0x21	22	0x31	192	0x02	34	0x12	384	0x22	24	0x32	224	0x03	40	0x13	480	0x23	26	0x33	256	0x04	44	0x14	576	0x24	28	0x34	320	0x05	48	0x15	640	0x25	32	0x35	384	0x06	56	0x16	768	0x26	36	0x36	448	0x07	68	0x17	960	0x27	40	0x37	512	0x08	80	0x18	1152	0x28	48	0x38	640	0x09	88	0x19	1280	0x29	56	0x39	768	0x0A	104	0x1A	1536	0x2A	64	0x3A	896	0x0B	128	0x1B	1920	0x2B	72	0x3B	1024	0x0C	144	0x1C	2304	0x2C	80	0x3C	1280	0x0D	160	0x1D	2560	0x2D	96	0x3D	1536	0x0E	192	0x1E	3072	0x2E	112	0x3E	1792	0x0F	240	0x1F	3840	0x2F	128	0x3F	2048
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0x0F	240	0x1F	3840	0x2F	128	0x3F	2048																																																																																																																																		

25.2.3 I²C Control Register (I2CR)

I2CR enables the I²C module and the I²C interrupt. It also contains bits that govern operation as a slave or a master.

Address: 0xFC05_8008 (I2CR)

Access: User read/write

	7	6	5	4	3	2	1	0
R	IEN	IIEN	MSTA	MTX	TXAK	RSTA	0	0
W								
Reset:	0	0	0	0	0	0	0	0

Figure 25-4. I²C Control Register (I2CR)

Table 25-4. I2CR Field Descriptions

Field	Description
7 IEN	I ² C enable. Controls the software reset of the entire I ² C module. If the module is enabled in the middle of a byte transfer, slave mode ignores the current bus transfer and starts operating when the next START condition is detected. Master mode is not aware that the bus is busy; initiating a start cycle may corrupt the current bus cycle, ultimately causing the current master or the I ² C module to lose arbitration, after which bus operation returns to normal. 0 The I ² C module is disabled, but registers can be accessed. 1 The I ² C module is enabled. This bit must be set before any other I2CR bits have any effect.
6 IEN	I ² C interrupt enable. 0 I ² C module interrupts are disabled, but currently pending interrupt condition is not cleared. 1 I ² C module interrupts are enabled. An I ² C interrupt occurs if I2SR[IIF] is also set.
5 MSTA	Master/slave mode select bit. If the master loses arbitration, MSTA is cleared without generating a STOP signal. 0 Slave mode. Changing MSTA from 1 to 0 generates a STOP and selects slave mode. 1 Master mode. Changing MSTA from 0 to 1 signals a START on the bus and selects master mode.
4 MTX	Transmit/receive mode select bit. Selects the direction of master and slave transfers. 0 Receive 1 Transmit. When the device is addressed as a slave, software must set MTX according to I2SR[SRW]. In master mode, MTX must be set according to the type of transfer required. Therefore, when the MCU addresses a slave device, MTX is always 1.
3 TXAK	Transmit acknowledge enable. Specifies the value driven onto I2C_SDA during acknowledge cycles for master and slave receivers. Writing TXAK applies only when the I ² C bus is a receiver. 0 An acknowledge signal is sent to the bus at the ninth clock bit after receiving one byte of data. 1 No acknowledge signal response is sent (acknowledge bit = 1).
2 RSTA	Repeat start. Always read as 0. Attempting a repeat start without bus mastership causes loss of arbitration. 0 No repeat start 1 Generates a repeated START condition.
1	Reserved, must be cleared.

25.2.4 I²C Status Register (I2SR)

I2SR contains bits that indicate transaction direction and status.

Address: 0xFC05_800C (I2SR)

Access: User read/write

	7	6	5	4	3	2	1	0
R	ICF	IAAS	IBB	IAL	0	SRW	IIF	RXAK
W								
Reset:	1	0	0	0	0	0	0	1

Figure 25-5. I²C Status Register (I2SR)

Table 25-5. I2SR Field Descriptions

Field	Description
7 ICF	I ² C Data transferring bit. While one byte of data is transferred, ICF is cleared. 0 Transfer in progress 1 Transfer complete. Set by falling edge of ninth clock of a byte transfer.
6 IAAS	I ² C addressed as a slave bit. The CPU is interrupted if I2CR[IEN] is set. Next, the CPU must check SRW and set its TX/RX mode accordingly. Writing to I2CR clears this bit. 0 Not addressed. 1 Addressed as a slave. Set when its own address (IADR) matches the calling address.
5 IBB	I ² C bus busy bit. Indicates the status of the bus. 0 Bus is idle. If a STOP signal is detected, IBB is cleared. 1 Bus is busy. When START is detected, IBB is set.
4 IAL	I ² C arbitration lost. Set by hardware in the following circumstances. (IAL must be cleared by software by writing zero to it.) <ul style="list-style-type: none"> • I2C_SDA sampled low when the master drives high during an address or data-transmit cycle. • I2C_SDA sampled low when the master drives high during the acknowledge bit of a data-receive cycle. • A start cycle is attempted when the bus is busy. • A repeated start cycle is requested in slave mode. • A stop condition is detected when the master did not request it.
3	Reserved, must be cleared.
2 SRW	Slave read/write. When IAAS is set, SRW indicates the value of the R/W command bit of the calling address sent from the master. SRW is valid only when a complete transfer has occurred, no other transfers have been initiated, and the I ² C module is a slave and has an address match. 0 Slave receive, master writing to slave. 1 Slave transmit, master reading from slave.
1 IIF	I ² C interrupt. Must be cleared by software by writing a 0 in the interrupt routine. 0 No I ² C interrupt pending 1 An interrupt is pending, which causes a processor interrupt request (if IEN = 1). Set when one of the following occurs: <ul style="list-style-type: none"> • Complete one byte transfer (set at the falling edge of the ninth clock) • Reception of a calling address that matches its own specific address in slave-receive mode • Arbitration lost
0 RXAK	Received acknowledge. The value of I2C_SDA during the acknowledge bit of a bus cycle. 0 An acknowledge signal was received after the completion of 8-bit data transmission on the bus 1 No acknowledge signal was detected at the ninth clock.

25.2.5 I²C Data I/O Register (I2DR)

In master-receive mode, reading I2DR allows a read to occur and for the next data byte to be received. In slave mode, the same function is available after the I²C has received its slave address.

Address: 0xFC05_8010 (I2DR)

Access: User read/write

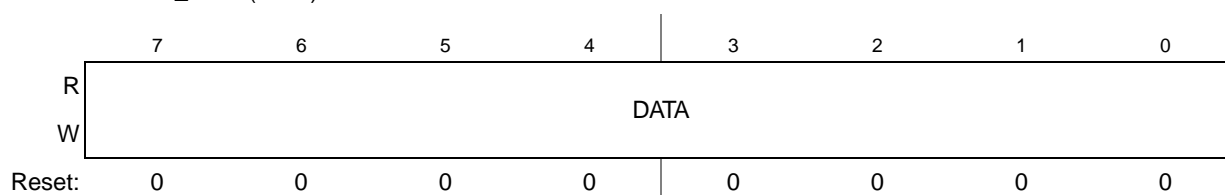
Figure 25-6. I²C Data I/O Register (I2DR)

Table 25-6. I2DR Field Description

Field	Description
7–0 DATA	<p>I²C data. When data is written to this register in master transmit mode, a data transfer is initiated. The most significant bit is sent first. In master receive mode, reading this register initiates the reception of the next byte of data. In slave mode, the same functions are available after an address match has occurred.</p> <p>Note: In master transmit mode, the first byte of data written to I2DR following assertion of I2CR[MSTA] is used for the address transfer and should comprise the calling address (in position D7–D1) concatenated with the required R/W bit (in position D0). This bit (D0) is not automatically appended by the hardware, software must provide the appropriate R/W bit.</p> <p>Note: I2CR[MSTA] generates a start when a master does not already own the bus. I2CR[RSTA] generates a start (restart) without the master first issuing a stop (i.e., the master already owns the bus). To start the read of data, a dummy read to this register starts the read process from the slave. The next read of the I2DR register contains the actual data.</p>

25.3 Functional Description

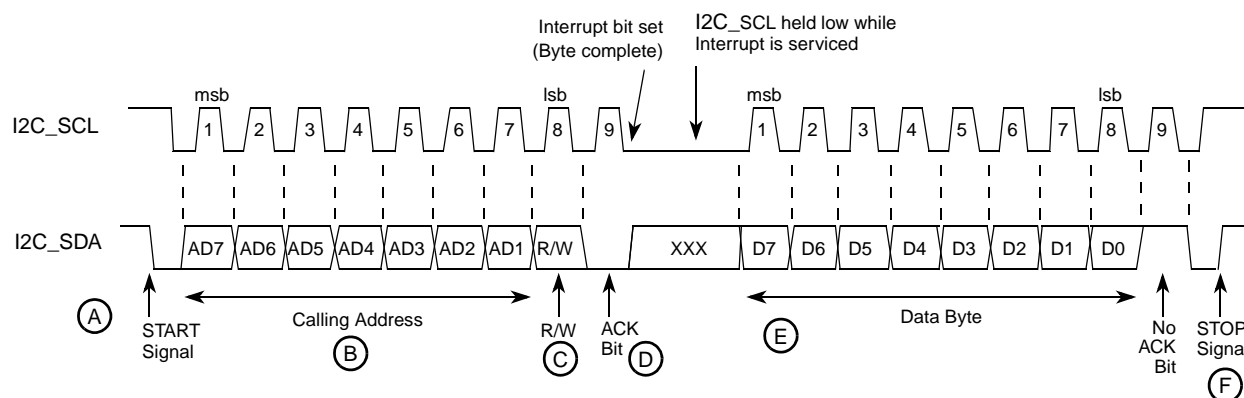
The I²C module uses a serial data line (I2C_SDA) and a serial clock line (I2C_SCL) for data transfer. For I²C compliance, all devices connected to these two signals must have open drain or open collector outputs. The logic AND function is exercised on both lines with external pull-up resistors.

Out of reset, the I²C default state is as a slave receiver. Therefore, when not programmed to be a master or responding to a slave transmit address, the I²C module should return to the default slave receiver state. See [Section 25.4.1, “Initialization Sequence,”](#) for exceptions.

Normally, a standard communication is composed of four parts: START signal, slave address transmission, data transfer, and STOP signal. These are discussed in the following sections.

25.3.1 START Signal

When no other device is bus master (I2C_SCL and I2C_SDA lines are at logic high), a device can initiate communication by sending a START signal (see A in [Figure 25-7](#)). A START signal is defined as a high-to-low transition of I2C_SDA while I2C_SCL is high. This signal denotes the beginning of a data transfer (each data transfer can be several bytes long) and awakens all slaves.

Figure 25-7. I²C Standard Communication Protocol

25.3.2 Slave Address Transmission

The master sends the slave address in the first byte after the START signal (B). After the seven-bit calling address, it sends the R/W bit (C), which tells the slave data transfer direction (0 equals write transfer, 1 equals read transfer).

Each slave must have a unique address. An I²C master must not transmit its own slave address; it cannot be master and slave at the same time.

The slave whose address matches that sent by the master pulls I2C_SDA low at the ninth serial clock (D) to return an acknowledge bit.

25.3.3 Data Transfer

When successful slave addressing is achieved, data transfer can proceed (see E in Figure 25-7) on a byte-by-byte basis in the direction specified by the R/W bit sent by the calling master.

Data can be changed only while I2C_SCL is low and must be held stable while I2C_SCL is high, as Figure 25-7 shows. I2C_SCL is pulsed once for each data bit, with the msb being sent first. The receiving device must acknowledge each byte by pulling I2C_SDA low at the ninth clock; therefore, a data byte transfer takes nine clock pulses. See Figure 25-8.

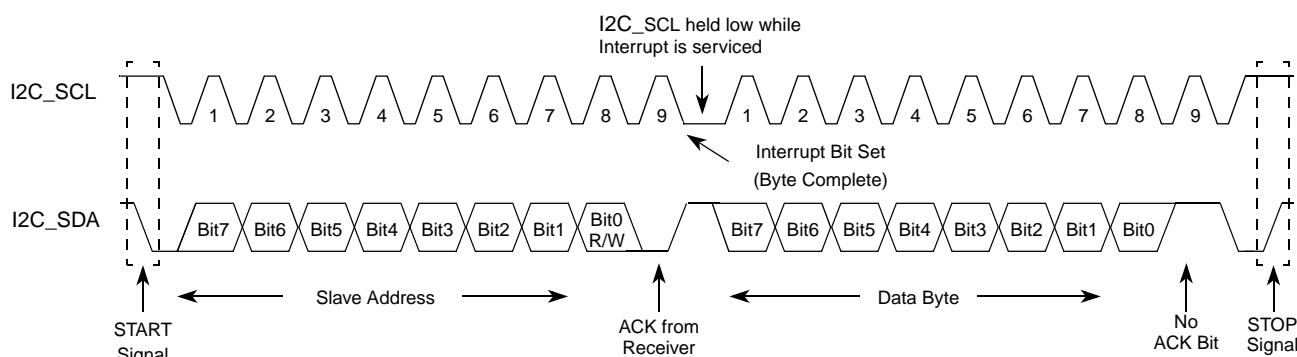


Figure 25-8. Data Transfer

25.3.4 Acknowledge

The transmitter releases the I2C_SDA line high during the acknowledge clock pulse as shown in Figure 25-9. The receiver pulls down the I2C_SDA line during the acknowledge clock pulse so that it remains stable low during the high period of the clock pulse.

If it does not acknowledge the master, the slave receiver must leave I2C_SDA high. The master can then generate a STOP signal to abort data transfer or generate a START signal (repeated start, shown in Figure 25-10 and discussed in Section 25.3.6, “Repeated START”)

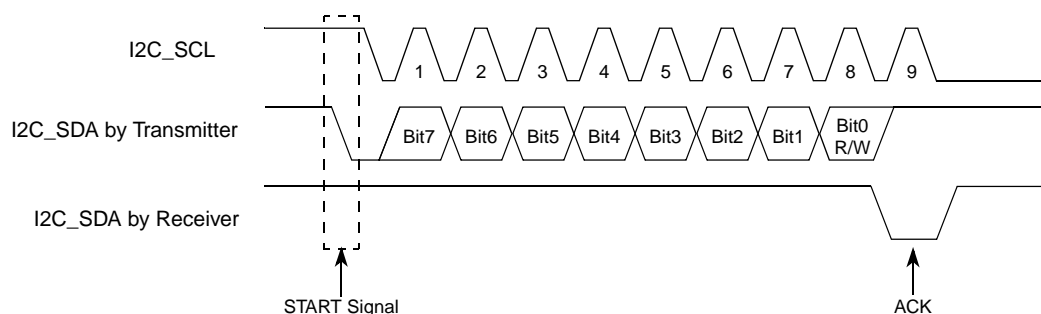


Figure 25-9. Acknowledgement by Receiver

If the master receiver does not acknowledge the slave transmitter after a byte transmission, it means end-of-data to the slave. The slave releases I2C_SDA for the master to generate a STOP or START signal (Figure 25-9).

25.3.5 STOP Signal

The master can terminate communication by generating a STOP signal to free the bus. A STOP signal is defined as a low-to-high transition of I2C_SDA while I2C_SCL is at logical high (see F in Figure 25-7). The master can generate a STOP even if the slave has generated an acknowledgment, at which point the slave must release the bus. The master may also generate a START signal following a calling address, without first generating a STOP signal. Refer to Section 25.3.6, “Repeated START.”

25.3.6 Repeated START

A repeated START signal is a START signal generated without first generating a STOP signal to terminate the communication, as shown in Figure 25-10. The master uses a repeated START to communicate with another slave or with the same slave in a different mode (transmit/receive mode) without releasing the bus.

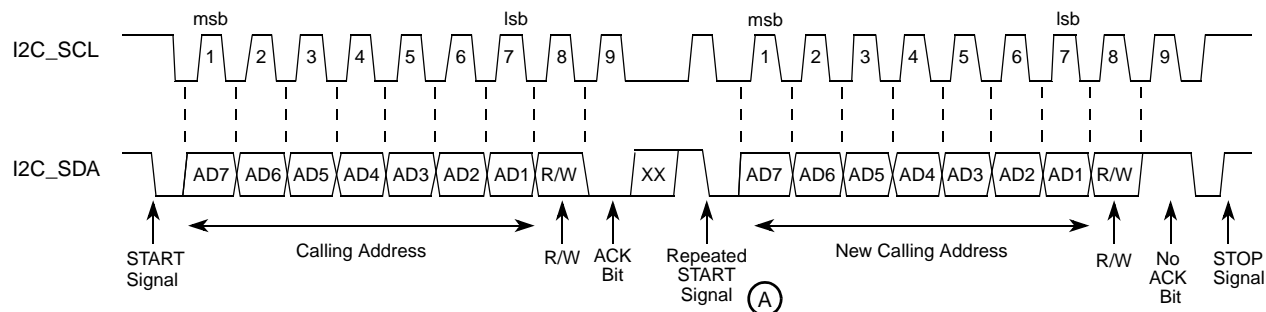


Figure 25-10. Repeated START

Various combinations of read/write formats are then possible:

- The first example in Figure 25-11 is the case of master-transmitter transmitting to slave-receiver. The transfer direction is not changed.
- The second example in Figure 25-11 is the master reading the slave immediately after the first byte. At the moment of the first acknowledge, the master-transmitter becomes a master-receiver and the slave-receiver becomes slave-transmitter.
- In the third example in Figure 25-11, START condition and slave address are repeated using the repeated START signal. This is to communicate with same slave in a different mode without releasing the bus. The master transmits data to the slave first, and then the master reads data from slave by reversing the R/W bit.

ST = Start

SP = Stop

A = Acknowledge (I2C_SDA low)

\bar{A} = Not Acknowledge (I2C_SDA high)

Rept ST = Repeated Start



From Master to Slave



From Slave to Master

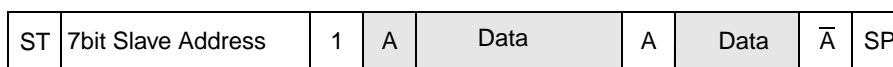
Example 1:

R/W



Example 2:

R/W



Note: No acknowledge on the last byte

Example 3:

R/W

R/W

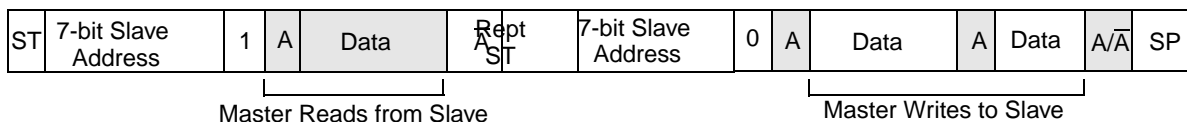


Figure 25-11. Data Transfer, Combined Format

25.3.7 Clock Synchronization and Arbitration

I²C is a true multi-master bus that allows more than one master connected to it. If two or more master devices simultaneously request control of the bus, a clock synchronization procedure determines the bus clock. Because wire-AND logic is performed on the I2C_SCL line, a high-to-low transition on the I2C_SCL line affects all the devices connected on the bus. The devices start counting their low period and after a device's clock has gone low, it holds the I2C_SCL line low until the clock high state is reached. However, change of low to high in this device's clock may not change the state of the I2C_SCL line if another device clock remains within its low period. Therefore, synchronized clock I2C_SCL is held low by the device with the longest low period.

Devices with shorter low periods enter a high wait state during this time (see Figure 25-12). When all devices concerned have counted off their low period, the synchronized clock (I2C_SCL) line is released and pulled high. At this point, the device clocks and the I2C_SCL line are synchronized, and the devices start counting their high periods. The first device to complete its high period pulls the I2C_SCL line low again.

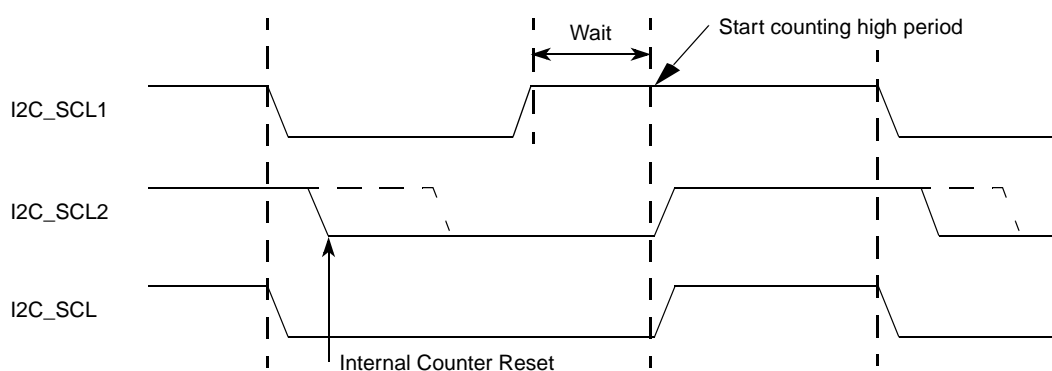


Figure 25-12. Clock Synchronization

A data arbitration procedure determines the relative priority of the contending masters. A bus master loses arbitration if it transmits logic 1 while another master transmits logic 0. The losing masters immediately switch over to slave receive mode and stop driving I2C_SDA output (see Figure 25-13). In this case, transition from master to slave mode does not generate a STOP condition. Meanwhile, hardware sets I2SR[IAL] to indicate loss of arbitration.

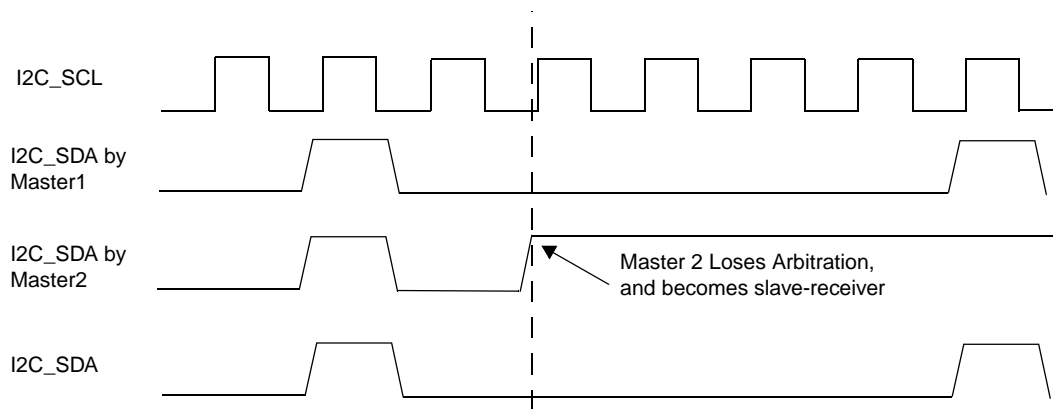


Figure 25-13. Arbitration Procedure

25.3.8 Handshaking and Clock Stretching

The clock synchronization mechanism can act as a handshake in data transfers. Slave devices can hold I2C_SCL low after completing one byte transfer. In such a case, the clock mechanism halts the bus clock and forces the master clock into wait states until the slave releases I2C_SCL.

Slaves may also slow down the transfer bit rate. After the master has driven I2C_SCL low, the slave can drive I2C_SCL low for the required period and then release it. If the slave I2C_SCL low period is longer than the master I2C_SCL low period, the resulting I2C_SCL bus signal low period is stretched.

25.4 Initialization/Application Information

The following examples show programming for initialization, signaling START, post-transfer software response, signaling STOP, and generating a repeated START.

25.4.1 Initialization Sequence

Before the interface can transfer serial data, registers must be initialized:

1. Set I2FDR[IC] to obtain I2C_SCL frequency from the system bus clock. See [Section 25.2.2, “I²C Frequency Divider Register \(I2FDR\).”](#)
2. Update the I2ADR to define its slave address.
3. Set I2CR[IEN] to enable the I²C bus interface system.
4. Modify the I2CR to select or deselect master/slave mode, transmit/receive mode, and interrupt-enable or not.

NOTE

If I2SR[IBB] is set when the I²C bus module is enabled, execute the following pseudocode sequence before proceeding with normal initialization code. This issues a STOP command to the slave device, placing it in idle state as if it were power-cycled on.

```
I2CR = 0x0
I2CR = 0xA0
dummy read of I2DR
I2SR = 0x0
I2CR = 0x0
I2CR = 0x80      ; re-enable
```

25.4.2 Generation of START

After completion of the initialization procedure, serial data can be transmitted by selecting the master transmitter mode. On a multiple-master bus system, I2SR[IBB] must be tested to determine whether the serial bus is free. If the bus is free (IBB is cleared), the START signal and the first byte (the slave address) can be sent. The data written to the data register comprises the address of the desired slave and the lsb indicates the transfer direction.

The free time between a STOP and the next START condition is built into the hardware that generates the START cycle. Depending on the relative frequencies of the system clock and the I2C_SCL period, the

processor may need to wait until the I²C is busy after writing the calling address to the I2DR before proceeding with the following instructions.

The following example signals START and transmits the first byte of data (slave address):

1. Check I2SR[IBB]. If it is set, wait until it is clear.
2. After cleared, set to transmit mode by setting I2CR[MTX].
3. Set master mode by setting I2CR[MSTA]. This generates a START condition.
4. Transmit the calling address via the I2DR.
5. Check I2SR[IBB]. If it is clear, wait until it is set and go to step #1.

25.4.3 Post-Transfer Software Response

Sending or receiving a byte sets the I2SR[ICF], which indicates one byte communication is finished. I2SR[IIF] is also set. An interrupt is generated if the interrupt function is enabled during initialization by setting I2CR[IEN]. Software must first clear I2SR[IIF] in the interrupt routine. Reading from I2DR in receive mode or writing to I2DR in transmit mode can clear I2SR[ICF].

Software can service the I²C I/O in the main program by monitoring the IIF bit if the interrupt function is disabled. Polling should monitor IIF rather than ICF, because that operation is different when arbitration is lost.

When an interrupt occurs at the end of the address cycle, the master is always in transmit mode; the address is sent. If master receive mode is required, I2CR[MTX] should be toggled.

During slave-mode address cycles (I2SR[IAAS] = 1), I2SR[SRW] is read to determine the direction of the next transfer. MTX is programmed accordingly. For slave-mode data cycles (IAAS = 0), SRW is invalid. MTX should be read to determine the current transfer direction.

The following is an example of a software response by a master transmitter in the interrupt routine (see [Figure 25-14](#)).

1. Clear the I2CR[IIF] flag.
2. Check if acknowledge has been received, I2SR[RXAK].
3. If no ACK, end transmission. Else, transmit next byte of data via I2DR.

25.4.4 Generation of STOP

A data transfer ends when the master signals a STOP, which can occur after all data is sent, as in the following example.

1. Check if acknowledge has been received, I2SR[RXAK]. If no ACK, end transmission and go to step #5.
2. Get value from transmitting counter, TXCNT. If no more data, go to step #5.
3. Transmit next byte of data via I2DR.
4. Decrement TXCNT and go to step #1
5. Generate a stop condition by clearing I2CR[MSTA].

For a master receiver to terminate a data transfer, it must inform the slave transmitter by not acknowledging the last data byte. This is done by setting I2CR[TXAK] before reading the next-to-last byte. Before the last byte is read, a STOP signal must be generated, as in the following example.

1. Decrement RXCNT.
2. If last byte (RXCNT = 0) go to step #4.
3. If next to last byte (RXCNT = 1), set I2CR[TXAK] to disable ACK and go to step #5.
4. This is last byte, so clear I2CR[MSTA] to generate a STOP signal.
5. Read data from I2DR.
6. If there is more data to be read (RXCNT \neq 0), go to step #1 if desired.

25.4.5 Generation of Repeated START

If the master wants the bus after the data transfer, it can signal another START followed by another slave address without signaling a STOP, as in the following example.

1. Generate a repeated START by setting I2CR[RSTA].
2. Transmit the calling address via I2DR.

25.4.6 Slave Mode

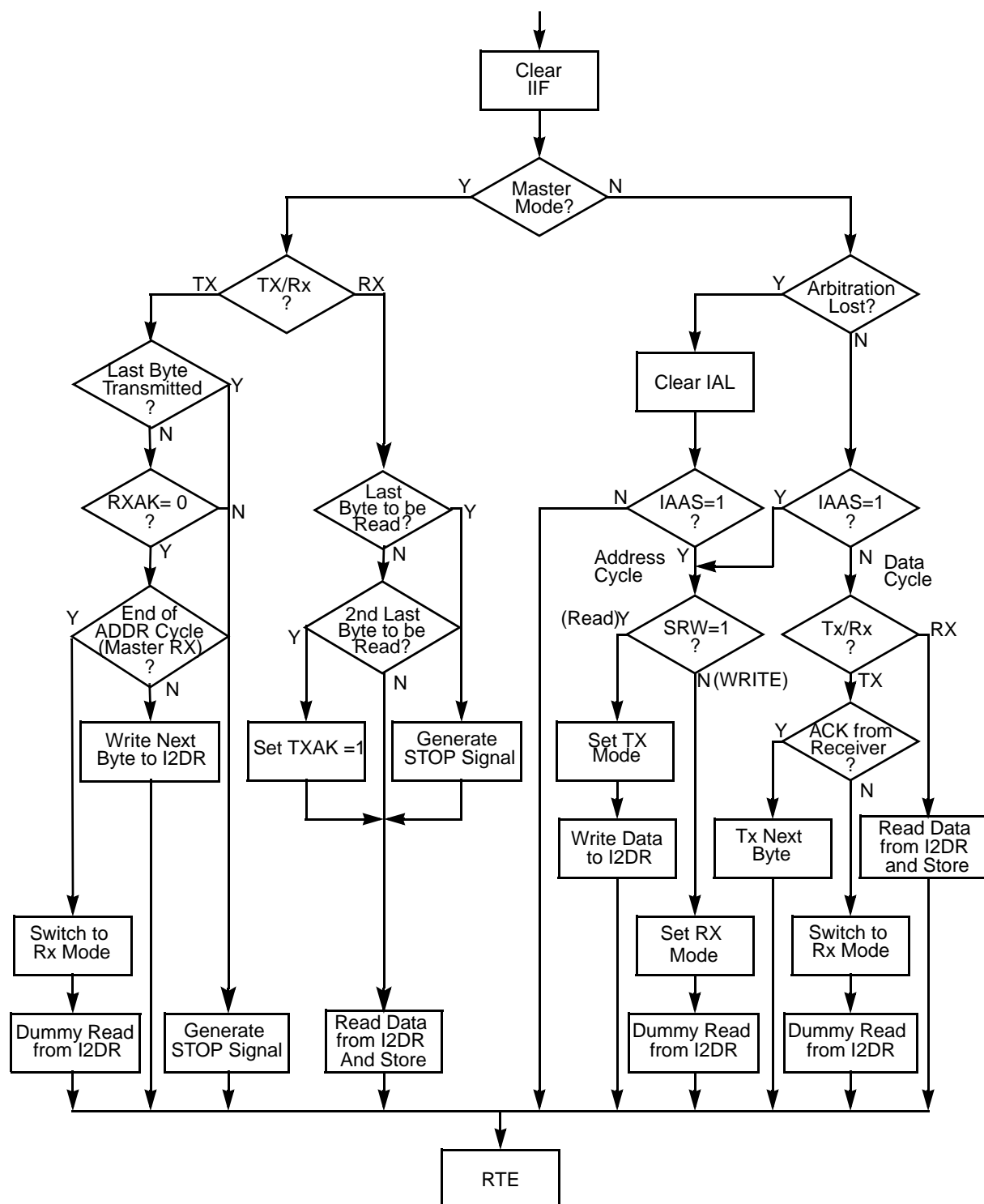
In the slave interrupt service routine, software must poll the I2SR[IAAS] bit to determine if the controller has received its slave address. If IAAS is set, software must set the transmit/receive mode select bit (I2CR[MTX]) according to the I2SR[SRW]. Writing to I2CR clears IAAS automatically. The only time IAAS is read as set is from the interrupt at the end of the address cycle where an address match occurred; interrupts resulting from subsequent data transfers have IAAS cleared. A data transfer can now be initiated by writing information to I2DR for slave transmits, or read from I2DR in slave-receive mode. A dummy read of I2DR in slave/receive mode releases I2C_SCL, allowing the master to send data.

In the slave transmitter routine, I2SR[RXAK] must be tested before sending the next byte of data. Setting RXAK means an end-of-data signal from the master receiver, after which software must switch it from transmitter to receiver mode. Reading I2DR releases I2C_SCL so the master can generate a STOP signal.

25.4.7 Arbitration Lost

If several devices try to engage the bus at the same time, one becomes master. Hardware immediately switches devices that lose arbitration to slave receive mode. Data output to I2C_SDA stops, but I2C_SCL continues generating until the end of the byte during which arbitration is lost. An interrupt occurs at the falling edge of the ninth clock of this transfer with I2SR[IAL] set and I2CR[MSTA] cleared.

If a non-master device tries to transmit or execute a START, hardware inhibits the transmission, clears MSTA without signaling a STOP, generates an interrupt to the CPU, and sets IAL to indicate a failed attempt to engage the bus. When considering these cases, slave service routine should first test IAL and software should clear it if it is set.

Figure 25-14. Flow-Chart of Typical I²C Interrupt Routine

Chapter 26

Debug Module

26.1 Introduction

This chapter describes the revision B+ enhanced hardware debug module.

26.1.1 Block Diagram

The debug module is shown in [Figure 26-1](#).

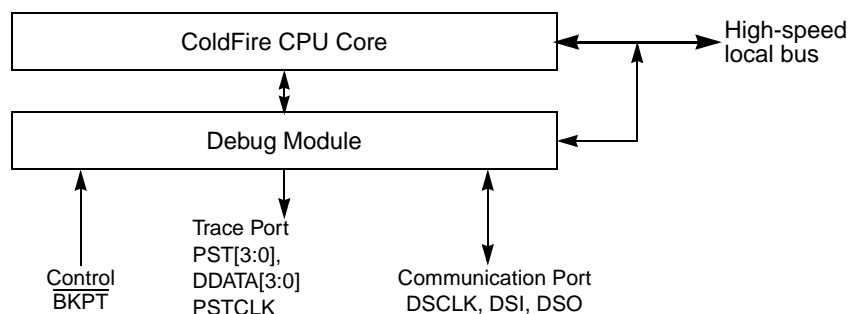


Figure 26-1. Processor/Debug Module Interface

26.1.2 Overview

Debug support is divided into three areas:

- Real-time trace support—The ability to determine the dynamic execution path through an application is fundamental for debugging. The ColdFire solution implements an 8-bit parallel output bus that reports processor execution status and data to an external emulator system. See [Section 26.4.4, “Real-Time Trace Support”](#).
- Background debug mode (BDM)—Provides low-level debugging in the ColdFire processor complex. In BDM, the processor complex is halted and a variety of commands can be sent to the processor to access memory, registers, and peripherals. The external emulator uses a three-pin, serial, full-duplex channel. See [Section 26.4.1, “Background Debug Mode \(BDM\),”](#) and [Section 26.3, “Memory Map/Register Definition”](#).
- Real-time debug support—BDM requires the processor to be halted, which many real-time embedded applications cannot do. Debug interrupts let real-time systems execute a unique service routine that can quickly save the contents of key registers and variables and return the system to normal operation. External development systems can access saved data, because the hardware supports concurrent operation of the processor and BDM-initiated commands. In addition, the option allows interrupts to occur. See [Section 26.4.2, “Real-Time Debug Support”](#).

The first version 2 ColdFire core devices implemented the original debug architecture, now called revision A. Based on feedback from customers and third-party developers, enhancements have been added to succeeding generations of ColdFire cores. For revision A, CSR[HRL] is 0. See [Section 26.3.2, “Configuration/Status Register \(CSR\)”](#).

Revision B (and B+) of the debug architecture offers more flexibility for configuring the hardware breakpoint trigger registers and removing the restrictions involving concurrent BDM processing while hardware breakpoint registers are active. Revision B+ adds three new PC breakpoint registers. For revision B, CSR[HRL] is 1, and for revision B+, CSR[HRL] is 0x9.

The following table summarizes the various debug revisions.

Table 26-1. Debug Revision Summary

Revision	CSR[HRL]		Enhancements
A	0000	—	Initial debug revision
B	0001	—	BDM command execution does not affect hardware breakpoint logic Added BDM address attribute register (BAAR) BKPT configurable interrupt (CSR[BKD]) Level 1 and level 2 triggers on OR condition, in addition to AND SYNC_PC command to display the processor's current PC
B+	1001	—	3 new PC breakpoint registers PBR1–3

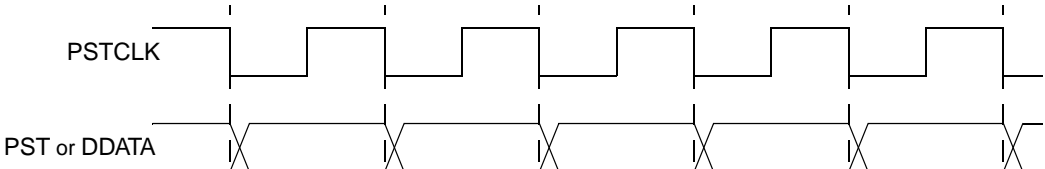
26.2 Signal Descriptions

[Table 26-2](#) describes debug module signals. All ColdFire debug signals are unidirectional and related to a rising edge of the processor core's clock signal. The standard 26-pin debug connector is shown in [Section 26.4.6, “Freescale-Recommended BDM Pinout”](#).

Table 26-2. Debug Module Signals

Signal	Description
Development Serial Clock (DSCLK)	Internally synchronized input. (The logic level on DSCLK is validated if it has the same value on two consecutive rising bus clock edges.) Clocks the serial communication port to the debug module during packet transfers. Maximum frequency is 1/5 the processor status clock (PSTCLK). At the synchronized rising edge of DSCLK, the data input on DSI is sampled and DSO changes state.
Development Serial Input (DSI)	Internally synchronized input that provides data input for the serial communication port to the debug module after the DSCLK has been seen as high (logic 1).
Development Serial Output (DSO)	Provides serial output communication for debug module responses. DSO is registered internally. The output is delayed from the validation of DSCLK high.
Breakpoint ($\overline{\text{BKPT}}$)	Input requests a manual breakpoint. Assertion of $\overline{\text{BKPT}}$ puts the processor into a halted state after the current instruction completes. Halt status is reflected on processor status signals (PST[3:0]) as the value 0xF. If CSR[BKD] is set (disabling normal $\overline{\text{BKPT}}$ functionality), asserting $\overline{\text{BKPT}}$ generates a debug interrupt exception in the processor.

Table 26-2. Debug Module Signals (continued)

Signal	Description
Processor Status Clock (PSTCLK)	<p>Delayed version of the processor clock. Its rising edge appears in the center of valid PST and DDATA output. PSTCLK indicates when the development system should sample PST and DDATA values. The following figure shows PSTCLK timing with respect to PST and DDATA.</p>  <p>If real-time trace is not used, setting CSR[PCD] keeps PSTCLK, PST and DDATA outputs from toggling without disabling triggers. Non-quiescent operation can be reenabled by clearing CSR[PCD], although the external development systems must resynchronize with the PST and DDATA outputs. PSTCLK starts clocking only when the first non-zero PST value (0xC, 0xD, or 0xF) occurs during system reset exception processing. Table 26-24 describes PST values.</p>
Debug Data (DDATA[3:0])	<p>These output signals display the register breakpoint status as a default, or optionally, captured address and operand values. The capturing of data values is controlled by the setting of the CSR. Additionally, execution of the WDDATA instruction by the processor captures operands that are displayed on DDATA. These signals are updated each processor cycle. These signals are not implemented on the QFP devices (MCF5207CABxxx and MCF5208CABxxx).</p>
Processor Status (PST[3:0])	<p>These output signals report the processor status. Table 26-24 shows the encoding of these signals. These outputs indicate the current status of the processor pipeline and, as a result, are not related to the current bus transfer. The PST value is updated each processor cycle. These signals are not implemented on the QFP devices (MCF5207CABxxx and MCF5208CABxxx).</p>
All Processor Status Outputs (ALLPST)	<p>ALLPST is a logical AND of the four PST signals. PST[3:0] and DDATA[3:0] are not available on the QFP devices (MCF5207CABxxx and MCF5208CABxxx). When asserted, reflects that the core is halted.</p>

26.3 Memory Map/Register Definition

In addition to the existing BDM commands that provide access to the processor's registers and the memory subsystem, the debug module contain a number of registers to support the required functionality. These registers are also accessible from the processor's supervisor programming model by executing the WDEBUG instruction (write only). Therefore, the breakpoint hardware in debug module can be read or written by the external development system using the debug serial interface or written by the operating system running on the processor core. Software guarantees that accesses to these resources are serialized and logically consistent. Hardware provides a locking mechanism in CSR to allow external development system to disable any attempted writes by the processor to the breakpoint registers (setting CSR[IPW]). BDM commands must not be issued if the ColdFire processor is using the WDEBUG instruction to access debug module registers, or the resulting behavior is undefined. The DSCLK must be quiescent during operation of the WDEBUG command.

These registers, shown in [Table 26-3](#), are treated as 32-bit quantities, regardless of the number of implemented bits. These registers are also accessed through the BDM port by the commands, WDMREG and RDMREG, described in [Section 26.4.1.5, "BDM Command Set"](#). These commands contain a 5-bit field, DRc, that specifies the register, as shown in [Table 26-3](#).

Table 26-3. Debug Module Memory Map

DRc[4–0]	Register Name	Width (bits)	Access	Reset Value	Section/ Page
0x00	Configuration/status register (CSR)	32	R/W See Note	0x0090_0000	26.3.2/26-5
0x05	BDM address attribute register (BAAR)	32 ¹	W	0x05	26.3.3/26-8
0x06	Address attribute trigger register (AATR)	32 ¹	W	0x0005	26.3.4/26-9
0x07	Trigger definition register (TDR)	32	W	0x0000_0000	26.3.5/26-10
0x08	PC breakpoint register 0 (PBR0)	32	W	Undefined	26.3.6/26-13
0x09	PC breakpoint mask register (PBMR)	32	W	Undefined	26.3.6/26-13
0x0C	Address breakpoint high register (ABHR)	32	W	Undefined	26.3.7/26-15
0x0D	Address breakpoint low register (ABLR)	32	W	Undefined	26.3.7/26-15
0x0E	Data breakpoint register (DBR)	32	W	Undefined	26.3.8/26-16
0x0F	Data breakpoint mask register (DBMR)	32	W	Undefined	26.3.8/26-16
0x18	PC breakpoint register 1 (PBR1)	32	W	See Section	26.3.6/26-13
0x1A	PC breakpoint register 2 (PBR2)	32	W	See Section	26.3.6/26-13
0x1B	PC breakpoint register 3 (PBR3)	32	W	See Section	26.3.6/26-13

¹ Each debug register is accessed as a 32-bit register; reserved fields are not used (don't care).

NOTE

Debug control registers can be written by the external development system or the CPU through the WDEBUG instruction. These control registers are write-only from the programming model and they can be written through the BDM port using the WDMREG command. In addition, the configuration/status register (CSR) can be read through the BDM port using the RDMREG command.

The ColdFire debug architecture supports a number of hardware breakpoint registers, that can be configured into single- or double-level triggers based on the PC or operand address ranges with an optional inclusion of specific data values.

26.3.1 Shared Debug Resources

The debug module revision A implementation provides a common hardware structure for BDM and breakpoint functionality. Certain hardware structures are used for BDM and breakpoint purposes as shown in [Table 26-4](#).

Table 26-4. Shared BDM/Breakpoint Hardware

Register	BDM Function	Breakpoint Function
AATR	Bus attributes for all memory commands	Attributes for address breakpoint
ABHR	Address for all memory commands	Address for address breakpoint
DBR	Data for all BDM write commands	Data for data breakpoint

Therefore, loading a register to perform a specific function that shares hardware resources is destructive to the shared function. For example, if an operand address breakpoint is loaded into the debug module, a BDM command to access memory overwrites an address breakpoint in ABHR. If a data breakpoint is configured, a BDM write command overwrites the data breakpoint in DBR.

Revision B added hardware registers to eliminate these shared functions. The BAAR is used to specify bus attributes for BDM memory commands and has the same format as the LSB of the AATR. The registers containing the BDM memory address and the BDM data are not program visible.

26.3.2 Configuration/Status Register (CSR)

The CSR defines the debug configuration for the processor and memory subsystem and contains status information from the breakpoint logic. CSR is write-only from the programming model. It can be read from and written to through the BDM port. CSR is accessible in supervisor mode as debug control register 0x00 using the WDEBBUG instruction and through the BDM port using the RDMREG and WDMREG commands.

DRc[4:0]: 0x00 (CSR)

Access: Supervisor write-only
BDM read/write

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
R	BSTAT				FOF	TRG	HALT	BKPT	HRL				0	BKD	PCD	IPW
W																
Reset	0	0	0	0	0	0	0	0	1	0	0	1	0	0	0	0
	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	MAP	TRC	EMU	DDC	UHE	BTB			0	NPL	IPI	SSM	0	0	FDBG	DBGH
W																
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Figure 26-2. Configuration/Status Register (CSR)

Table 26-5. CSR Field Descriptions

Field	Description
31–28 BSTAT	Breakpoint Status. Provides read-only status (from the BDM port only) information concerning hardware breakpoints. BSTAT is cleared by a TDR write or by a CSR read when a level-2 breakpoint is triggered or a level-1 breakpoint is triggered and the level-2 breakpoint is disabled. 0000 No breakpoints enabled 0001 Waiting for level-1 breakpoint 0010 Level-1 breakpoint triggered 0101 Waiting for level-2 breakpoint 0110 Level-2 breakpoint triggered
27 FOF	Fault-on-fault. If FOF is set, a catastrophic halt occurred and forced entry into BDM. FOF is cleared when CSR is read (from the BDM port only).
26 TRG	Hardware breakpoint trigger. If TRG is set, a hardware breakpoint halted the processor core and forced entry into BDM. Reset, the debug GO command or reading CSR (from the BDM port only) clear TRG.
25 HALT	Processor halt. If HALT is set, the processor executed a HALT and forced entry into BDM. Reset, the debug GO command, or reading CSR (from the BDM port only) clear HALT.
24 BKPT	Breakpoint assert. If BKPT is set, $\overline{\text{BKPT}}$ was asserted, forcing the processor into BDM. Reset, the debug GO command, or reading CSR (from the BDM port only) clear BKPT.
23–20 HRL	Hardware revision level. Indicates, from the BDM port only, the level of debug module functionality. An emulator could use this information to identify the level of functionality supported. 0000 Revision A 0001 Revision B 0010 Revision C 0011 Revision D 1001 Revision B+ (This is the value used for this device) 1011 Revision D+
19	Reserved, must be cleared.
18 BKD	Breakpoint disable. Disables the normal $\overline{\text{BKPT}}$ input signal functionality, and allows the assertion of this pin to generate a debug interrupt. 0 Normal operation 1 $\overline{\text{BKPT}}$ is edge-sensitive: a high-to-low edge on $\overline{\text{BKPT}}$ signals a debug interrupt to the ColdFire core. The processor makes this interrupt request pending until the next sample point occurs, when the exception is initiated. In the ColdFire architecture, the interrupt sample point occurs once per instruction. There is no support for nesting debug interrupts.
17 PCD	PSTCLK disable. 0 PSTCLK is fully operational 1 Disables the generation of the PSTCLK and PSTDDATA output signals, and forces these signals to remain quiescent Note: When PCD is set, do not execute a wddata instruction or perform any debug captures. Doing so, hangs the device.
16 IPW	Inhibit processor writes. Setting IPW inhibits processor-initiated writes to the debug module's programming model registers. Only commands from the external development system can modify IPW.
15 MAP	Force processor references in emulator mode. 0 All emulator-mode references are mapped into supervisor code and data spaces. 1 The processor maps all references while in emulator mode to a special address space, TT equals 10, TM equals 101 or 110. The internal SRAM and caches are disabled.

Table 26-5. CSR Field Descriptions (continued)

Field	Description
14 TRC	Force emulation mode on trace exception. 0 The processor enters supervisor mode 1 The processor enters emulator mode when a trace exception occurs
13 EMU	Force emulation mode. 0 Do not force emulator mode 1 The processor begins executing in emulator mode. See Section 26.4.2.2, “Emulator Mode” .
12–11 DDC	Debug data control. Controls operand data capture for DDATA, which displays the number of bytes defined by the operand reference size before the actual data; byte displays 8 bits, word displays 16 bits, and long displays 32 bits (one nibble at a time across multiple PSTCLK clock cycles). See Table 26-24 . 00 No operand data is displayed. 01 Capture all write data. 10 Capture all read data. 11 Capture all read and write data.
10 UHE	User halt enable. Selects the CPU privilege level required to execute the HALT instruction. 0 HALT is a supervisor-only instruction. 1 HALT is a supervisor/user instruction.
9–8 BTB	Branch target bytes. Defines the number of bytes of branch target address DDATA displays. 00 0 bytes 01 Lower 2 bytes of the target address 10 Lower 3 bytes of the target address 11 Entire 4-byte target address See Section 26.4.4.1, “Begin Execution of Taken Branch (PST = 0x5)” .
7	Reserved, must be cleared.
6 NPL	Non-pipelined mode. Determines whether the core operates in pipelined mode or not. 0 Pipelined mode 1 Non-pipelined mode. The processor effectively executes one instruction at a time with no overlap. This adds at least 5 cycles to the execution time of each instruction. Given an average execution latency of 1.6 cycles/instruction, throughput in non-pipeline mode would be 6.6 cycles/instruction, approximately 25% or less of pipelined performance. Regardless of the NPL state, a triggered PC breakpoint is always reported before the triggering instruction executes. In normal pipeline operation, occurrence of an address and/or data breakpoint trigger is imprecise. In non-pipeline mode, triggers are always reported before the next instruction begins execution and trigger reporting can be considered precise. An address or data breakpoint should always occur before the next instruction begins execution. Therefore, the occurrence of the address/data breakpoints should be guaranteed.
5 IPI	Ignore pending interrupts. 0 Core services any pending interrupt requests that were signalled while in single-step mode. 1 Core ignores any pending interrupt requests signalled while in single-instruction-step mode.
4 SSM	Single-Step Mode. Setting SSM puts the processor in single-step mode. 0 Normal mode. 1 Single-step mode. The processor halts after execution of each instruction. While halted, any BDM command can be executed. On receipt of the GO command, the processor executes the next instruction and halts again. This process continues until SSM is cleared.
3–2	Reserved, must be cleared.

Table 26-5. CSR Field Descriptions (continued)

Field	Description
1 FDBG	Force the debug mode core output signal (to the on-chip peripherals). The debug mode output is logically defined as: $\text{Debug mode output} = \text{CSR[FDBG]} \mid \overline{\text{CSR[DBGH]}}$ and Core is halted 0 Debug mode output is not forced asserted. 1 Debug mode output core output signal is asserted.
0 DBGH	Disable debug signal assertion during core halt. The debug mode output (to the on-chip peripherals) is logically defined as: $\text{Debug mode output} = \text{CSR[FDBG]} \mid \overline{\text{CSR[DBGH]}}$ and Core is halted 0 Debug mode output is asserted when the core is halted. 1 Debug mode output is not asserted when the core is halted.

26.3.3 BDM Address Attribute Register (BAAR)

The BAAR register defines the address space for memory-referencing BDM commands. BAAR[R, SZ] are loaded directly from the BDM command, while the low-order 5 bits can be programmed from the external development system. To maintain compatibility with revision A, BAAR is loaded any time the AATR is written. The BAAR is initialized to a value of 0x05, setting supervisor data as the default address space.

DRc[4:0]: 0x05 (BAAR)

Access: Supervisor write-only
BDM write-only

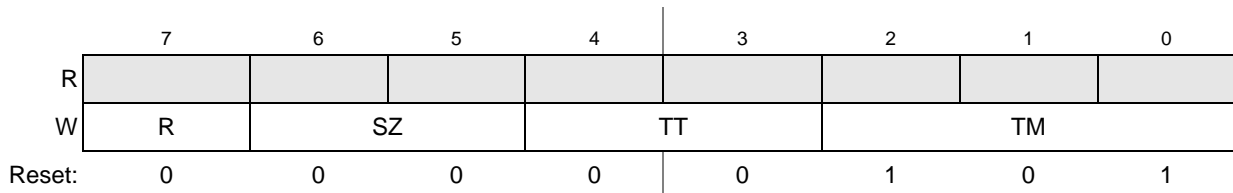


Figure 26-3. BDM Address Attribute Register (BAAR)

Table 26-6. BAAR Field Descriptions

Field	Description
7 R	Read/Write. 0 Write 1 Read
6–5 SZ	Size. 00 Longword 01 Byte 10 Word 11 Reserved
4–3 TT	Transfer Type. See the TT definition in the AATR description, Section 26.3.4, “Address Attribute Trigger Register (AATR)” .
2–0 TM	Transfer Modifier. See the TM definition in the AATR description, Section 26.3.4, “Address Attribute Trigger Register (AATR)” .

26.3.4 Address Attribute Trigger Register (AATR)

The AATR defines address attributes and a mask to be matched in the trigger. The register value is compared with address attribute signals from the processor's local high-speed bus, as defined by the setting of the trigger definition register (TDR). AATR is accessible in supervisor mode as debug control register 0x06 using the WDEBBUG instruction and through the BDM port using the WDMREG command.

DRc[4:0]: 0x06 (AATR)

Access: Supervisor write-only
BDM write-only

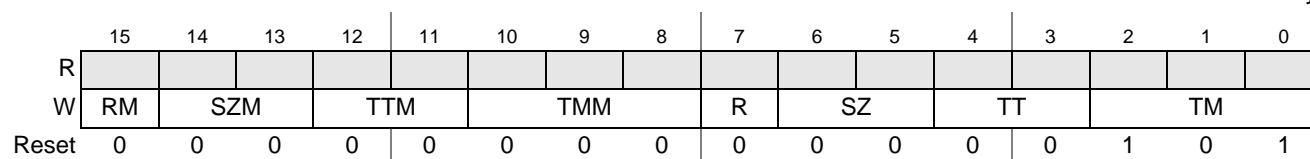


Figure 26-4. Address Attribute Trigger Register (AATR)

Table 26-7. AATR Field Descriptions

Field	Description
15 RM	Read/write Mask. Setting RM masks R in address comparisons.
14–13 SZM	Size Mask. Setting an SZM bit masks the corresponding SZ bit in address comparisons.
12–11 TTM	Transfer Type Mask. Setting a TTM bit masks the corresponding TT bit in address comparisons.
10–8 TMM	Transfer Modifier Mask. Setting a TMM bit masks the corresponding TM bit in address comparisons.
7 R	Read/Write. R is compared with the $\overline{R/W}$ signal of the processor's local bus.
6–5 SZ	Size. Compared to the processor's local bus size signals. 00 Longword 01 Byte 10 Word 11 Reserved

Table 26-7. AATR Field Descriptions (continued)

Field	Description																											
4–3 TT	<p>Transfer Type. Compared with the local bus transfer type signals.</p> <p>00 Normal processor access 01 Reserved 10 Emulator mode access 11</p> <p>These bits also define the TT encoding for BDM memory commands. In this case, the 01 encoding indicates an external or DMA access (for backward compatibility). These bits affect the TM bits.</p>																											
2–0 TM	<p>Transfer Modifier. Compared with the local bus transfer modifier signals, which give supplemental information for each transfer type. These bits also define the TM encoding for BDM memory commands (for backward compatibility).</p> <table><tr><th>TM</th><th>TT=00 (normal mode)</th><th>TT=10 (emulator mode)</th></tr><tr><td>000</td><td>Explicit cache line push</td><td>Reserved</td></tr><tr><td>001</td><td>User data access</td><td>Reserved</td></tr><tr><td>010</td><td>User code access</td><td>Reserved</td></tr><tr><td>011</td><td>Reserved</td><td>Reserved</td></tr><tr><td>100</td><td>Reserved</td><td>Reserved</td></tr><tr><td>101</td><td>Supervisor data access</td><td>Emulator mode access</td></tr><tr><td>110</td><td>Supervisor code access</td><td>Emulator code access</td></tr><tr><td>111</td><td>Reserved</td><td>Reserved</td></tr></table>	TM	TT=00 (normal mode)	TT=10 (emulator mode)	000	Explicit cache line push	Reserved	001	User data access	Reserved	010	User code access	Reserved	011	Reserved	Reserved	100	Reserved	Reserved	101	Supervisor data access	Emulator mode access	110	Supervisor code access	Emulator code access	111	Reserved	Reserved
TM	TT=00 (normal mode)	TT=10 (emulator mode)																										
000	Explicit cache line push	Reserved																										
001	User data access	Reserved																										
010	User code access	Reserved																										
011	Reserved	Reserved																										
100	Reserved	Reserved																										
101	Supervisor data access	Emulator mode access																										
110	Supervisor code access	Emulator code access																										
111	Reserved	Reserved																										

26.3.5 Trigger Definition Register (TDR)

The TDR configures the operation of the hardware breakpoint logic corresponding with the ABHR/ABLR/AATR, PBR/PBR1/PBR2/PBR3/PBMR, and DBR/DBMR registers within the debug module. TDR controls the actions taken under the defined conditions. Breakpoint logic may be configured as a one- or two-level trigger. TDR[31–16] bits define second-level trigger, and bits 15–0 define first-level trigger.

NOTE

The debug module has no hardware interlocks to prevent spurious breakpoint triggers while the breakpoint registers are being loaded. Disable TDR (by clearing TDR[29,13]) before defining triggers.

A write to TDR clears the CSR trigger status bits, CSR[BSTAT]. TDR is accessible in supervisor mode as debug control register 0x07 using the WDEBUG instruction and through the BDM port using the WDMREG command.

DRc[4:0]: 0x07 (TDR)

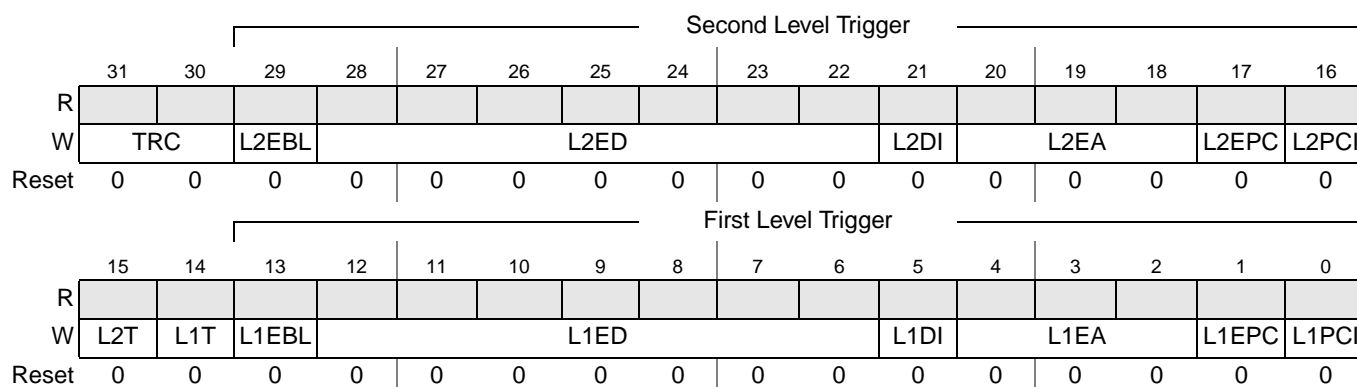
Access: Supervisor write-only
BDM write-only

Figure 26-5. Trigger Definition Register (TDR)

Table 26-8. TDR Field Descriptions

Field	Description																
31–30 TRC	Trigger Response Control. Determines how the processor responds to a completed trigger condition. The trigger response is always displayed on DDATA. 00 Display on DDATA only 01 Processor halt 10 Debug interrupt 11 Reserved																
29 L2EBL	Enable Level 2 Breakpoint. Global enable for the breakpoint trigger. 0 Disables all level 2 breakpoints 1 Enables all level 2 breakpoint triggers																
28–22 L2ED	Enable Level 2 Data Breakpoint. Setting an L2ED bit enables the corresponding data breakpoint condition based on the size and placement on the processor's local data bus. Clearing all ED bits disables data breakpoints. <table border="1"> <tr> <th>TDR Bit</th><th>Description</th></tr> <tr> <td>28</td><td>Data longword. Entire processor's local data bus.</td></tr> <tr> <td>27</td><td>Lower data word.</td></tr> <tr> <td>26</td><td>Upper data word.</td></tr> <tr> <td>25</td><td>Lower lower data byte. Low-order byte of the low-order word.</td></tr> <tr> <td>24</td><td>Lower middle data byte. High-order byte of the low-order word.</td></tr> <tr> <td>23</td><td>Upper middle data byte. Low-order byte of the high-order word.</td></tr> <tr> <td>22</td><td>Upper upper data byte. High-order byte of the high-order word.</td></tr> </table>	TDR Bit	Description	28	Data longword. Entire processor's local data bus.	27	Lower data word.	26	Upper data word.	25	Lower lower data byte. Low-order byte of the low-order word.	24	Lower middle data byte. High-order byte of the low-order word.	23	Upper middle data byte. Low-order byte of the high-order word.	22	Upper upper data byte. High-order byte of the high-order word.
TDR Bit	Description																
28	Data longword. Entire processor's local data bus.																
27	Lower data word.																
26	Upper data word.																
25	Lower lower data byte. Low-order byte of the low-order word.																
24	Lower middle data byte. High-order byte of the low-order word.																
23	Upper middle data byte. Low-order byte of the high-order word.																
22	Upper upper data byte. High-order byte of the high-order word.																
21 L2DI	Level 2 Data Breakpoint Invert. Inverts the logical sense of all the data breakpoint comparators. This can develop a trigger based on the occurrence of a data value other than the DBR contents. 0 No inversion 1 Invert data breakpoint comparators.																

Table 26-8. TDR Field Descriptions (continued)

Field	Description								
20–18 L2EA	<p>Enable Level 2 Address Breakpoint. Setting an L2EA bit enables the corresponding address breakpoint. Clearing all three bits disables the breakpoint.</p> <table> <tr> <th>TDR Bit</th><th>Description</th></tr> <tr> <td>20</td><td>Address breakpoint inverted. Breakpoint is based outside the range between ABLR and ABHR.</td></tr> <tr> <td>19</td><td>Address breakpoint range. The breakpoint is based on the inclusive range defined by ABLR and ABHR.</td></tr> <tr> <td>18</td><td>Address breakpoint low. The breakpoint is based on the address in the ABLR.</td></tr> </table>	TDR Bit	Description	20	Address breakpoint inverted. Breakpoint is based outside the range between ABLR and ABHR.	19	Address breakpoint range. The breakpoint is based on the inclusive range defined by ABLR and ABHR.	18	Address breakpoint low. The breakpoint is based on the address in the ABLR.
TDR Bit	Description								
20	Address breakpoint inverted. Breakpoint is based outside the range between ABLR and ABHR.								
19	Address breakpoint range. The breakpoint is based on the inclusive range defined by ABLR and ABHR.								
18	Address breakpoint low. The breakpoint is based on the address in the ABLR.								
17 L2EPC	<p>Enable Level 2 PC Breakpoint. 0 Disable PC breakpoint 1 Enable PC breakpoint where the trigger is defined by the logical summation of:</p> $(PBR0 \text{ and } \overline{PBMR}) PBR1 PBR2 PBR3$ <p style="text-align: right;"><i>Eqn. 26-1</i></p>								
16 L2PCI	<p>Level 2 PC Breakpoint Invert. 0 The PC breakpoint is defined within the region defined by $PBRn$ and $PBMR$. 1 The PC breakpoint is defined outside the region defined by $PBRn$ and $PBMR$.</p>								
15 L2T	<p>Level 2 Trigger. Determines the logic operation for the trigger between the PC_condition and the (Address_range & Data_condition) where the inclusion of a Data_condition is optional. The ColdFire debug architecture supports the creation of single or double-level triggers. 0 Level 2 trigger = PC_condition & Address_range & Data_condition 1 Level 2 trigger = PC_condition (Address_range & Data_condition) Note: Debug Rev A only had the AND condition available for the triggers.</p>								
14 L1T	<p>Level 1 Trigger. Determines the logic operation for the trigger between the PC_condition and the (Address_range & Data_condition) where the inclusion of a Data_condition is optional. The ColdFire debug architecture supports the creation of single or double-level triggers. 0 Level 1 trigger = PC_condition & Address_range & Data_condition 1 Level 1 trigger = PC_condition (Address_range & Data_condition) Note: Debug Rev A only had the AND condition available for the triggers.</p>								
13 L1EBL	<p>Enable Level 1 Breakpoint. Global enable for the breakpoint trigger. 0 Disables all level 1 breakpoints 1 Enables all level 1 breakpoint triggers</p>								

Table 26-8. TDR Field Descriptions (continued)

Field	Description																
12–6 L1ED	<p>Enable Level 1 Data Breakpoint. Setting an L1ED bit enables the corresponding data breakpoint condition based on the size and placement on the processor's local data bus. Clearing all L1ED bits disables data breakpoints.</p> <table> <tr> <th>TDR Bit</th><th>Description</th></tr> <tr> <td>12</td><td>Data longword. Entire processor's local data bus.</td></tr> <tr> <td>11</td><td>Lower data word.</td></tr> <tr> <td>10</td><td>Upper data word.</td></tr> <tr> <td>9</td><td>Lower lower data byte. Low-order byte of the low-order word.</td></tr> <tr> <td>8</td><td>Lower middle data byte. High-order byte of the low-order word.</td></tr> <tr> <td>7</td><td>Upper middle data byte. Low-order byte of the high-order word.</td></tr> <tr> <td>6</td><td>Upper upper data byte. High-order byte of the high-order word.</td></tr> </table>	TDR Bit	Description	12	Data longword. Entire processor's local data bus.	11	Lower data word.	10	Upper data word.	9	Lower lower data byte. Low-order byte of the low-order word.	8	Lower middle data byte. High-order byte of the low-order word.	7	Upper middle data byte. Low-order byte of the high-order word.	6	Upper upper data byte. High-order byte of the high-order word.
TDR Bit	Description																
12	Data longword. Entire processor's local data bus.																
11	Lower data word.																
10	Upper data word.																
9	Lower lower data byte. Low-order byte of the low-order word.																
8	Lower middle data byte. High-order byte of the low-order word.																
7	Upper middle data byte. Low-order byte of the high-order word.																
6	Upper upper data byte. High-order byte of the high-order word.																
5 L1DI	<p>Level 1 Data Breakpoint Invert. Inverts the logical sense of all the data breakpoint comparators. This can develop a trigger based on the occurrence of a data value other than the DBR contents.</p> <p>0 No inversion 1 Invert data breakpoint comparators.</p>																
4–2 L1EA	<p>Enable Level 1 Address Breakpoint. Setting an L1EA bit enables the corresponding address breakpoint. Clearing all three bits disables the address breakpoint.</p> <table> <tr> <th>TDR Bit</th><th>Description</th></tr> <tr> <td>4</td><td>Enable address breakpoint inverted. Breakpoint is based outside the range between ABLR and ABHR.</td></tr> <tr> <td>3</td><td>Enable address breakpoint range. The breakpoint is based on the inclusive range defined by ABLR and ABHR.</td></tr> <tr> <td>2</td><td>Enable address breakpoint low. The breakpoint is based on the address in the ABLR.</td></tr> </table>	TDR Bit	Description	4	Enable address breakpoint inverted. Breakpoint is based outside the range between ABLR and ABHR.	3	Enable address breakpoint range. The breakpoint is based on the inclusive range defined by ABLR and ABHR.	2	Enable address breakpoint low. The breakpoint is based on the address in the ABLR.								
TDR Bit	Description																
4	Enable address breakpoint inverted. Breakpoint is based outside the range between ABLR and ABHR.																
3	Enable address breakpoint range. The breakpoint is based on the inclusive range defined by ABLR and ABHR.																
2	Enable address breakpoint low. The breakpoint is based on the address in the ABLR.																
1 L1EPC	<p>Enable Level 1 PC breakpoint.</p> <p>0 Disable PC breakpoint 1 Enable PC breakpoint</p>																
0 L1PCI	<p>Level 1 PC Breakpoint Invert.</p> <p>0 The PC breakpoint is defined within the region defined by PBRn and PBMR. 1 The PC breakpoint is defined outside the region defined by PBRn and PBMR.</p>																

26.3.6 Program Counter Breakpoint/Mask Registers (PBR0–3, PBMR)

The PBR n registers define an instruction address for use as part of the trigger. These registers' contents are compared with the processor's program counter register when the appropriate valid bit is set (for PBR1–3) and TDR is configured appropriately. PBR0 bits are masked by setting corresponding PBMR bits (PBMR has no effect on PBR1–3). Results are compared with the processor's program counter register, as defined in TDR. Breakpoint registers, PBR1–3, have no masking associated with them. The

contents of the breakpoint registers are compared with the processor’s program counter register when TDR is configured appropriately.

The PC breakpoint registers are accessible in supervisor mode using the WDEBUG instruction and through the BDM port using the WDMREG command using values shown in [Section 26.4.1.5, “BDM Command Set”](#).

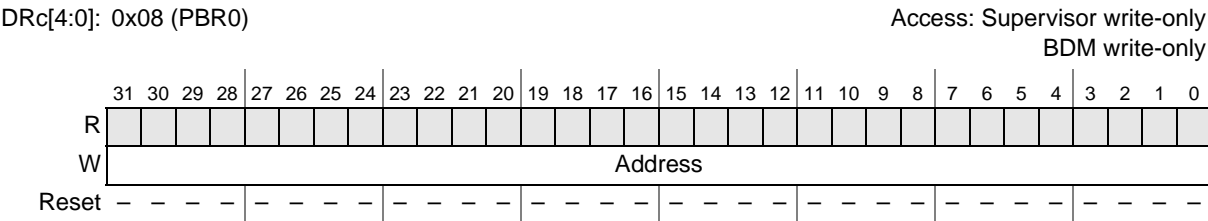


Figure 26-6. PC Breakpoint Register (PBR0)

Table 26-9. PBR0 Field Descriptions

Field	Description
31–0 Address	PC Breakpoint Address. The address to be compared with the PC as a breakpoint trigger. Note: PBR0[0] should always be loaded with a 0.

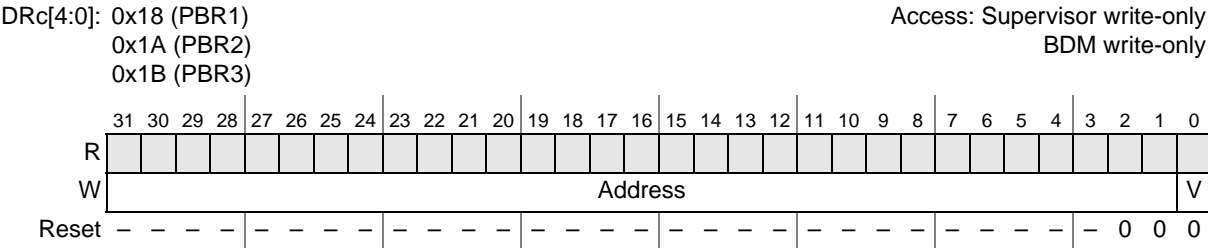


Figure 26-7. PC Breakpoint Register *n* (PBR*n*)

Table 26-10. PBR*n* Field Descriptions

Field	Description
31–1 Address	PC Breakpoint Address. The 31-bit address to be compared with the PC as a breakpoint trigger.
0 V	Valid Bit. This bit must be set for the PC breakpoint to occur at the address specified in the Address field. 0 PBR is disabled. 1 PBR is enabled.

[Figure 26-8](#) shows PBMR. PBMR is accessible in supervisor mode using the WDEBUG instruction and via the BDM port using the WDMREG command. PBMR only masks PBR0.

DRc[4:0]: 0x09 (PBMR)

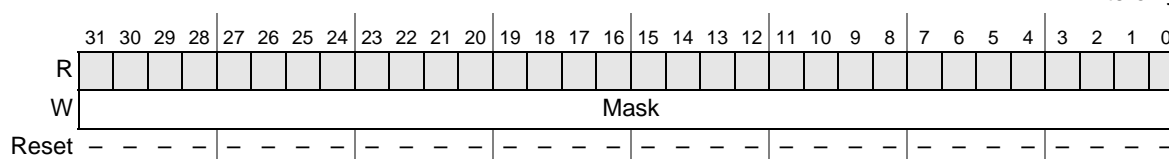
Access: Supervisor write-only
BDM write-only

Figure 26-8. PC Breakpoint Mask Register (PBMR)

Table 26-11. PBMR Field Descriptions

Field	Description
31–0 Mask	PC Breakpoint Mask. 0 The corresponding PBR0 bit is compared to the appropriate PC bit. 1 The corresponding PBR0 bit is ignored.

26.3.7 Address Breakpoint Registers (ABLR, ABHR)

The ABLR and ABHR define regions in the processor's data address space that can act as part of the trigger. These register values are compared with the address for each transfer on the processor's high-speed local bus. The trigger definition register (TDR) identifies the trigger as one of three cases:

- Identically the value in ABLR
- Inside the range bound by ABLR and ABHR inclusive
- Outside that same range

ABLR and ABHR are accessible in supervisor mode using the WDEBUG instruction and via the BDM port using the WDMREG command.

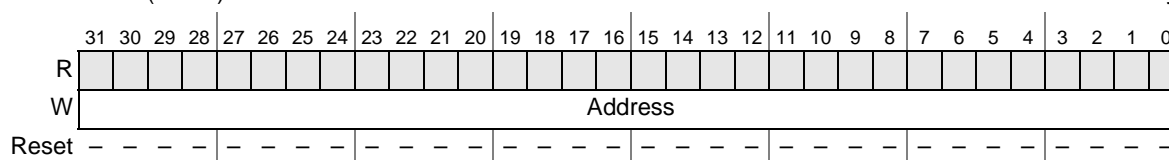
DRc[4:0]: 0x0C (ABHR)
0x0D (ABLR)Access: Supervisor write-only
BDM write-only

Figure 26-9. Address Breakpoint Registers (ABLR, ABHR,)

Table 26-12. ABLR Field Description

Field	Description
31–0 Address	Low Address. Holds the 32-bit address marking the lower bound of the address breakpoint range. Breakpoints for specific single addresses are programmed into ABLR.

Table 26-13. ABHR Field Description

Field	Description
31–0 Address	High Address. Holds the 32-bit address marking the upper bound of the address breakpoint range.

26.3.8 Data Breakpoint and Mask Registers (DBR, DBMR)

The data breakpoint register (DBR), specify data patterns used as part of the trigger into debug mode. DBR bits are masked by setting corresponding DBMR bits, as defined in TDR.

DBR and DBMR are accessible in supervisor mode using the WDEBBUG instruction and through the BDM port using the WDMREG command.

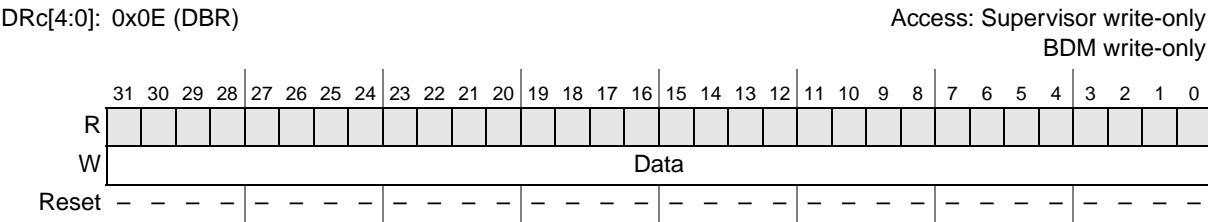


Figure 26-10. Data Breakpoint Registers (DBR)

Table 26-14. DBR Field Descriptions

Field	Description
31–0 Data	Data Breakpoint Value. Contains the value to be compared with the data value from the processor's local bus as a breakpoint trigger.

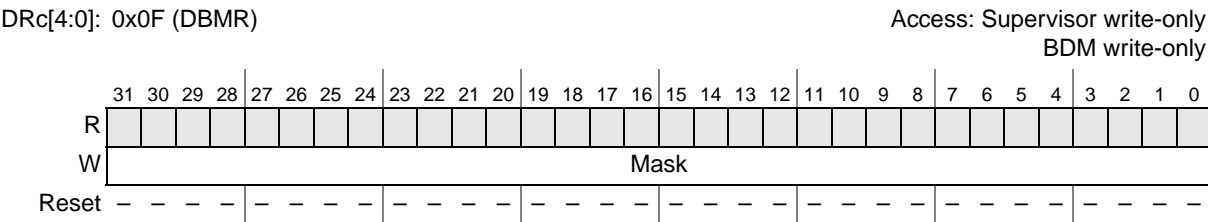


Figure 26-11. Data Breakpoint Mask Registers (DBMR)

Table 26-15. DBMR Field Descriptions

Field	Description
31–0 Mask	Data Breakpoint Mask. The 32-bit mask for the data breakpoint trigger. Clearing a DBMR bit allows the corresponding DBR bit to be compared to the appropriate bit of the processor's local data bus. Setting a DBMR bit causes that bit to be ignored.

The DBR supports aligned and misaligned references. [Table 26-16](#) shows relationships between processor address, access size, and location within the 32-bit data bus.

Table 26-16. Address, Access Size, and Operand Data Location

Address[1:0]	Access Size	Operand Location
00	Byte	D[31:24]
01	Byte	D[23:16]
10	Byte	D[15:8]
11	Byte	D[7:0]
0x	Word	D[31:16]
1x	Word	D[15:0]
xx	Longword	D[31:0]

26.4 Functional Description

26.4.1 Background Debug Mode (BDM)

The ColdFire family implements a low-level system debugger in the microprocessor in a dedicated hardware module. Communication with the development system is managed through a dedicated, high-speed serial command interface. Although some BDM operations, such as CPU register accesses, require the CPU to be halted, other BDM commands, such as memory accesses, can be executed while the processor is running.

BDM is useful because:

- In-circuit emulation is not needed, so physical and electrical characteristics of the system are not affected.
- BDM is always available for debugging the system and provides a communication link for upgrading firmware in existing systems.
- Provides high-speed cache downloading (500 Kbytes/sec), especially useful for flash programming
- Provides absolute control of the processor, and thus the system. This feature allows quick hardware debugging with the same tool set used for firmware development.

26.4.1.1 CPU Halt

Although most BDM operations can occur in parallel with CPU operations, unrestricted BDM operation requires the CPU to be halted. The sources that can cause the CPU to halt are listed below in order of priority:

1. A catastrophic fault-on-fault condition automatically halts the processor.
2. A hardware breakpoint trigger can generate a pending halt condition similar to the assertion of BKPT. This type of halt is always first marked as pending in the processor, which samples for pending halt and interrupt conditions once per instruction. When a pending condition is asserted, the processor halts execution at the next sample point. See [Section 26.4.2.1, “Theory of Operation”](#).

3. The execution of a HALT instruction immediately suspends execution. Attempting to execute HALT in user mode while CSR[UHE] is cleared generates a privilege violation exception. If CSR[UHE] is set, HALT can be executed in user mode. After HALT executes, the processor can be restarted by serial shifting a GO command into the debug module. Execution continues at the instruction after HALT.
4. The assertion of the $\overline{\text{BKPT}}$ input is treated as a pseudo-interrupt; asserting $\overline{\text{BKPT}}$ creates a pending halt postponed until the processor core samples for halts/interrupts. The processor samples for these conditions once during the execution of each instruction; if a pending halt is detected, the processor suspends execution and enters the halted state.

There are two special cases involving the assertion of $\overline{\text{BKPT}}$:

- After the system reset signal is negated, the processor waits for 16 processor clock cycles before beginning reset exception processing. If the $\overline{\text{BKPT}}$ input is asserted within eight cycles after $\overline{\text{RESET}}$ is negated, the processor enters the halt state, signaling halt status (0xF) on the PST outputs. While the processor is in this state, all resources accessible through the debug module can be referenced. This is the only chance to force the processor into emulation mode through CSR[EMU].
- After system initialization, the processor's response to the GO command depends on the set of BDM commands performed while it is halted for a breakpoint. Specifically, if the PC register was loaded, the GO command causes the processor to exit halted state and pass control to the instruction address in the PC, bypassing normal reset exception processing. If the PC was not loaded, the GO command causes the processor to exit halted state and continue reset exception processing.
- The ColdFire architecture also manages a special case of $\overline{\text{BKPT}}$ asserted while the processor is stopped by execution of the STOP instruction. For this case, the processor exits the stopped mode and enters the halted state, at which point all BDM commands may be exercised. When restarted, the processor continues by executing the next sequential instruction, which follows the STOP opcode.

The CSR[27–24] bits indicate the halt source, showing the highest priority source for multiple halt conditions.

26.4.1.2 BDM Serial Interface

When the CPU is halted and PST reflects the halt status, the development system can send unrestricted commands to the debug module. The debug module implements a synchronous serial protocol using two inputs (DSCLK and DSI) and one output (DSO), where DSO is specified as a delay relative to the rising edge of the processor clock. See [Table 26-2](#). The development system serves as the serial communication channel master and must generate DSCLK.

The serial channel operates at a frequency from DC to 1/5 of the PSTCLK frequency. The channel uses full-duplex mode, where data is sent and received simultaneously by master and slave devices. The transmission consists of 17-bit packets composed of a status/control bit and a 16-bit data word. As shown in [Figure 26-12](#), all state transitions are enabled on a rising edge of the PSTCLK clock when DSCLK is high; DSI is sampled and DSO is driven.

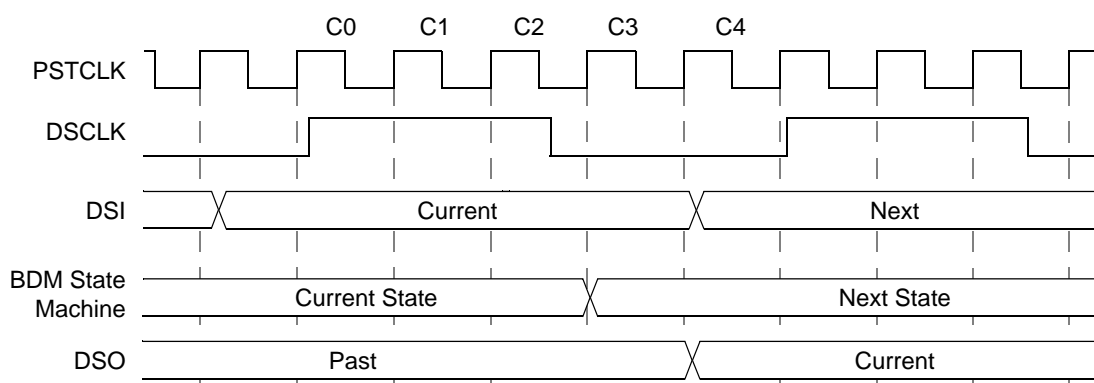


Figure 26-12. Maximum BDM Serial Interface Timing

DSCLK and DSI are synchronized inputs. DSCLK acts as a pseudo clock enable and is sampled, along with DSI, on the rising edge of PSTCLK. DSO is delayed from the DSCLK-enabled PSTCLK rising edge (registered after a BDM state machine state change). All events in the debug module's serial state machine are based on the PSTCLK rising edge. DSCLK must also be sampled low (on a positive edge of PSTCLK) between each bit exchange. The msb is sent first. Because DSO changes state based on an internally recognized rising edge of DSCLK, DSO cannot be used to indicate the start of a serial transfer. The development system must count clock cycles in a given transfer. C0–C4 are described as:

- C0: Set the state of the DSI bit
- C1: First synchronization cycle for DSI (DSCLK is high)
- C2: Second synchronization cycle for DSI (DSCLK is high)
- C3: BDM state machine changes state depending upon DSI and whether the entire input data transfer has been transmitted
- C4: DSO changes to next value

NOTE

A not-ready response can be ignored except during a memory-referencing cycle. Otherwise, the debug module can accept a new serial transfer after 32 processor clock periods.

26.4.1.3 Receive Packet Format

The basic receive packet consists of 16 data bits and 1 status bit

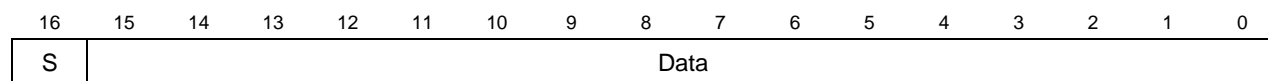


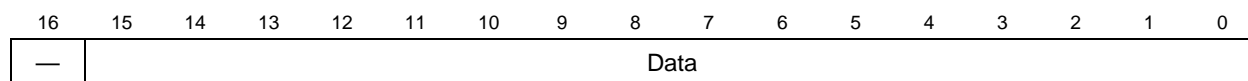
Figure 26-13. Receive BDM Packet

Table 26-17. Receive BDM Packet Field Description

Field	Description																		
16 S	<p>Status. Indicates the status of CPU-generated messages listed below. The not-ready response can be ignored unless a memory-referencing cycle is in progress. Otherwise, the debug module can accept a new serial transfer after 32 processor clock periods.</p> <table><tr><th>S</th><th>Data</th><th>Message</th></tr><tr><td>0</td><td>xxxx</td><td>Valid data transfer</td></tr><tr><td>0</td><td>FFFF</td><td>Status OK</td></tr><tr><td>1</td><td>0000</td><td>Not ready with response; come again</td></tr><tr><td>1</td><td>0001</td><td>Error-Terminated bus cycle; data invalid</td></tr><tr><td>1</td><td>FFFF</td><td>Illegal Command</td></tr></table>	S	Data	Message	0	xxxx	Valid data transfer	0	FFFF	Status OK	1	0000	Not ready with response; come again	1	0001	Error-Terminated bus cycle; data invalid	1	FFFF	Illegal Command
S	Data	Message																	
0	xxxx	Valid data transfer																	
0	FFFF	Status OK																	
1	0000	Not ready with response; come again																	
1	0001	Error-Terminated bus cycle; data invalid																	
1	FFFF	Illegal Command																	
15–0 Data	<p>Data. Contains the message to be sent from the debug module to the development system. The response message is always a single word, with the data field encoded as shown above.</p>																		

26.4.1.3.1 Transmit Packet Format

The basic transmit packet consists of 16 data bits and 1 reserved bit.

**Figure 26-14. Transmit BDM Packet****Table 26-18. Transmit BDM Packet Field Description**

Field	Description
16	Reserved, must be cleared.
15–0 Data	Data bits 15–0. Contains the data to be sent from the development system to the debug module.

26.4.1.3.2 BDM Command Format

All ColdFire family BDM commands include a 16-bit operation word followed by an optional set of one or more extension words.

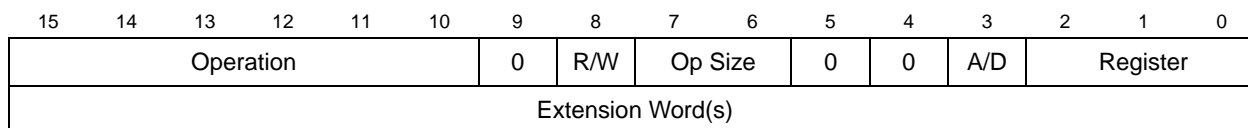
**Figure 26-15. BDM Command Format**

Table 26-19. BDM Field Descriptions

Field	Description															
15–10 Operation	Specifies the command. These values are listed in Table 26-20 .															
9	Reserved, must be cleared.															
8 R/W	Direction of operand transfer. 0 Data is written to the CPU or to memory from the development system. 1 The transfer is from the CPU to the development system.															
7–6 Op Size	Operand Data Size for Sized Operations. Addresses are expressed as 32-bit absolute values. A command performing a byte-sized memory read leaves the upper 8 bits of the response data undefined. Referenced data is returned in the lower 8 bits of the response. <table><tr><th></th><th>Operand Size</th><th>Bit Values</th></tr><tr><td>00</td><td>Byte</td><td>8 bits</td></tr><tr><td>01</td><td>Word</td><td>16 bits</td></tr><tr><td>10</td><td>Longword</td><td>32 bits</td></tr><tr><td>11</td><td>Reserved</td><td>—</td></tr></table>		Operand Size	Bit Values	00	Byte	8 bits	01	Word	16 bits	10	Longword	32 bits	11	Reserved	—
	Operand Size	Bit Values														
00	Byte	8 bits														
01	Word	16 bits														
10	Longword	32 bits														
11	Reserved	—														
5–4	Reserved, must be cleared.															
3 A/D	Address/Data. Determines whether the register field specifies a data or address register. 0 Data register. 1 Address register.															
2–0 Register	Contains the register number in commands that operate on processor registers. See Table 26-21 .															

26.4.1.3.3 Extension Words as Required

Some commands require extension words for addresses and/or immediate data. Addresses require two extension words because only absolute long addressing is permitted. Longword accesses are forcibly longword-aligned and word accesses are forcibly word-aligned. Immediate data can be 1 or 2 words long. Byte and word data each requires a single extension word, while longword data requires two extension words.

Operands and addresses are transferred most-significant word first. In the following descriptions of the BDM command set, the optional set of extension words is defined as address, data, or operand data.

26.4.1.4 Command Sequence Diagrams

The command sequence diagram in [Figure 26-16](#) shows serial bus traffic for commands. Each bubble represents a 17-bit bus transfer. The top half of each bubble indicates the data the development system sends to the debug module; the bottom half indicates the debug module's response to the previous development system commands. Command and result transactions overlap to minimize latency.

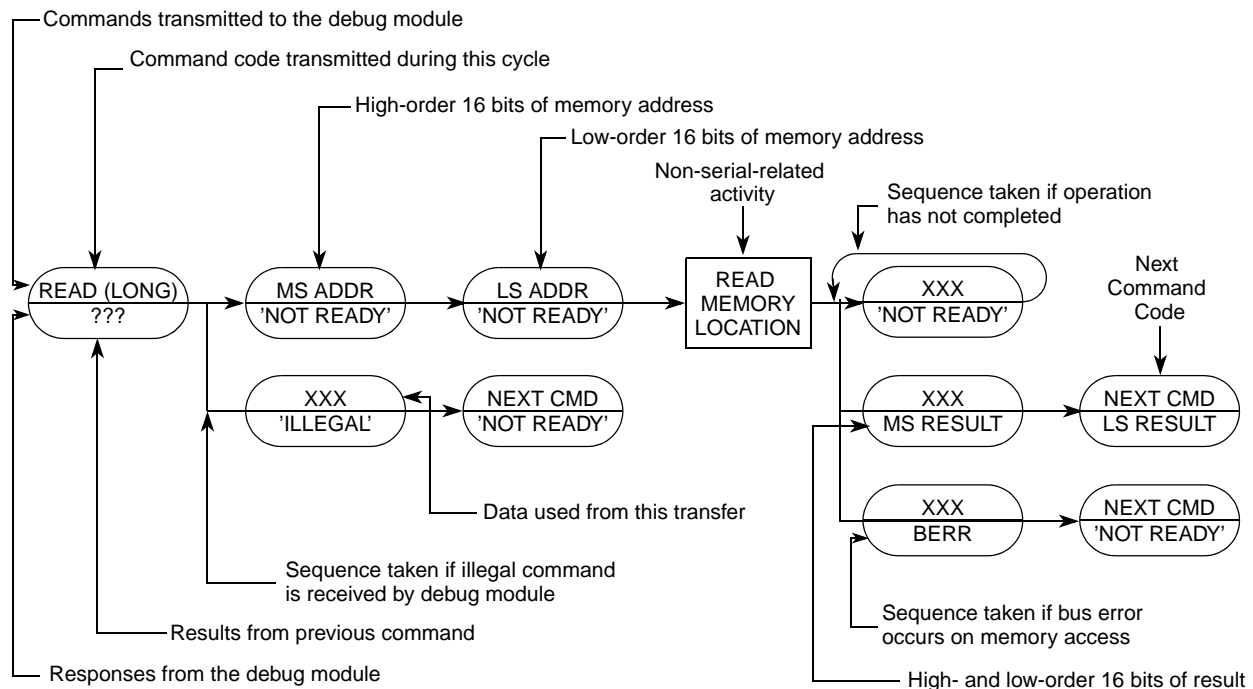


Figure 26-16. Command Sequence Diagram

The sequence is as follows:

- In cycle 1, the development system command is issued (READ in this example). The debug module responds with the low-order results of the previous command or a command complete status of the previous command, if no results are required.
- In cycle 2, the development system supplies the high-order 16 address bits. The debug module returns a not-ready response unless the received command is decoded as unimplemented, which is indicated by the illegal command encoding. If this occurs, the development system should retransmit the command.

NOTE

A not-ready response can be ignored except during a memory-referencing cycle. Otherwise, the debug module can accept a new serial transfer after 32 processor clock periods.

- In cycle 3, the development system supplies the low-order 16 address bits. The debug module always returns a not-ready response.
- At the completion of cycle 3, the debug module initiates a memory read operation. Any serial transfers that begin during a memory access return a not-ready response.
- Results are returned in the two serial transfer cycles after the memory access completes. For any command performing a byte-sized memory read operation, the upper 8 bits of the response data are undefined and the referenced data is returned in the lower 8 bits. The next command's opcode is sent to the debug module during the final transfer. If a bus error terminates a memory or register access, error status ($S = 1$, $DATA = 0x0001$) returns instead of result data.

26.4.1.5 BDM Command Set

Table 26-20 summarizes the BDM command set. Subsequent sections contain detailed descriptions of each command. Issuing a BDM command when the processor is accessing debug module registers using the WDEBUI instruction causes undefined behavior. See Table 26-21 for register address encodings.

Table 26-20. BDM Command Summary

Command	Mnemonic	Description	CPU State ¹	Section/Page	Command (Hex)
Read A/D register	RAREG/ RDREG	Read the selected address or data register and return the results through the serial interface.	Halted	26.4.1.5.1/26-24	0x218 {A/D, Reg[2:0]}
Write A/D register	WAREG/ WDREG	Write the data operand to the specified address or data register.	Halted	26.4.1.5.2/26-24	0x208 {A/D, Reg[2:0]}
Read memory location	READ	Read the data at the memory location specified by the longword address.	Steal	26.4.1.5.3/26-25	0x1900—byte 0x1940—word 0x1980—lword
Write memory location	WRITE	Write the operand data to the memory location specified by the longword address.	Steal	26.4.1.5.4/26-26	0x1800—byte 0x1840—word 0x1880—lword
Dump memory block	DUMP	Used with READ to dump large blocks of memory. An initial READ executes to set up the starting address of the block and to retrieve the first result. A DUMP command retrieves subsequent operands.	Steal	26.4.1.5.5/26-28	0x1D00—byte 0x1D40—word 0x1D80—lword
Fill memory block	FILL	Used with WRITE to fill large blocks of memory. An initial WRITE executes to set up the starting address of the block and to supply the first operand. A FILL command writes subsequent operands.	Steal	26.4.1.5.6/26-30	0x1C00—byte 0x1C40—word 0x1C80—lword
Resume execution	GO	The pipeline is flushed and refilled before resuming instruction execution at the current PC.	Halted	26.4.1.5.7/26-31	0x0C00
No operation	NOP	Perform no operation; may be used as a null command.	Parallel	26.4.1.5.8/26-32	0x0000
Output the current PC	SYNC_PC	Capture the current PC and display it on the PST/DDATA outputs.	Parallel	26.4.1.5.9/26-32	0x0001
Read control register	RCREG	Read the system control register.	Halted	26.4.1.5.10/26-33	0x2980
Write control register	WCREG	Write the operand data to the system control register.	Halted	26.4.1.5.13/26-35	0x2880
Read debug module register	RDMREG	Read the debug module register.	Parallel	26.4.1.5.14/26-36	0x2D {0x4 ² DRc[4:0]}
Write debug module register	WDMREG	Write the operand data to the debug module register.	Parallel	26.4.1.5.15/26-37	0x2C {0x4 ² DRc[4:0]}

¹ General command effect and/or requirements on CPU operation:

- Halted: The CPU must be halted to perform this command.
- Steal: Command generates bus cycles that can be interleaved with bus accesses.
- Parallel: Command is executed in parallel with CPU activity.

² 0x4 is a three-bit field.

Freescale reserves unassigned command opcodes. All unused command formats within any revision level perform a NOP and return the illegal command response.

The following sections describe the commands summarized in [Table 26-20](#).

NOTE

The BDM status bit (S) is 0 for normally completed commands. S is set for illegal commands, not-ready responses, and transfers with bus-errors. [Section 26.4.1.2, “BDM Serial Interface,”](#) describes the receive packet format.

26.4.1.5.1 Read A/D Register (RAREG/RDREG)

Read the selected address or data register and return the 32-bit result. A bus error response is returned if the CPU core is not halted.

Command/Result Formats:

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Command	0x2				0x1				0x8				A/D	Register		
Result	D[31:16]															
	D[15:0]															

Figure 26-17. RAREG/RDREG Command Format

Command Sequence:

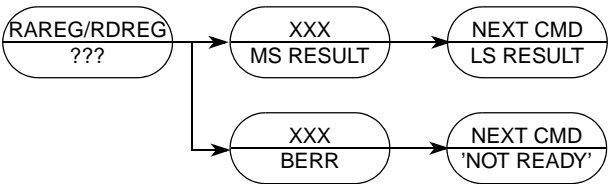


Figure 26-18. RAREG/RDREG Command Sequence

Operand Data: None

Result Data: The contents of the selected register are returned as a longword value, most-significant word first.

26.4.1.5.2 Write A/D Register (WAREG/WDREG)

The operand longword data is written to the specified address or data register. A write alters all 32 register bits. A bus error response is returned if the CPU core is not halted.

Command Format:

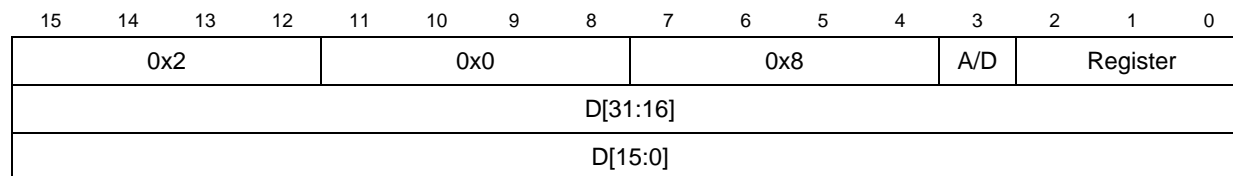


Figure 26-19. WAREG/WDREG Command Format

Command Sequence:

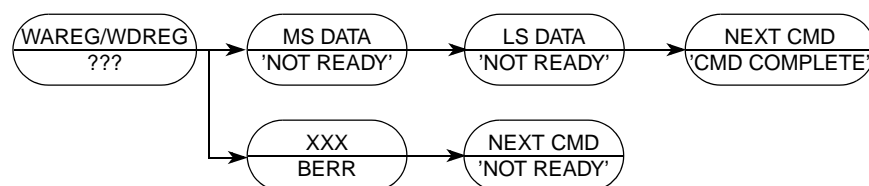


Figure 26-20. WAREG/WDREG Command Sequence

Operand Data: Longword data is written into the specified address or data register. The data is supplied most-significant word first.

Result Data: Command complete status is indicated by returning 0xFFFF (with S cleared) when the register write is complete.

26.4.1.5.3 Read Memory Location (READ)

Read data at the longword address. Address space is defined by BAAR[TT,TM]. Hardware forces low-order address bits to 0s for word and longword accesses to ensure that word addresses are word-aligned and longword addresses are longword-aligned.

Command/Result Formats:

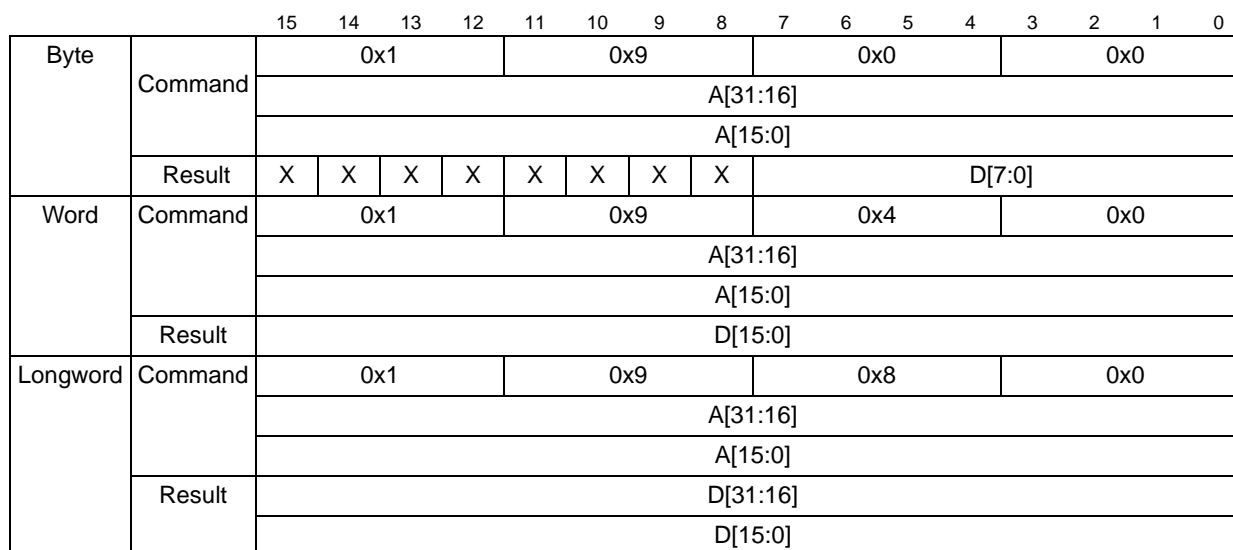


Figure 26-21. READ Command/Result Formats

Command Sequence:

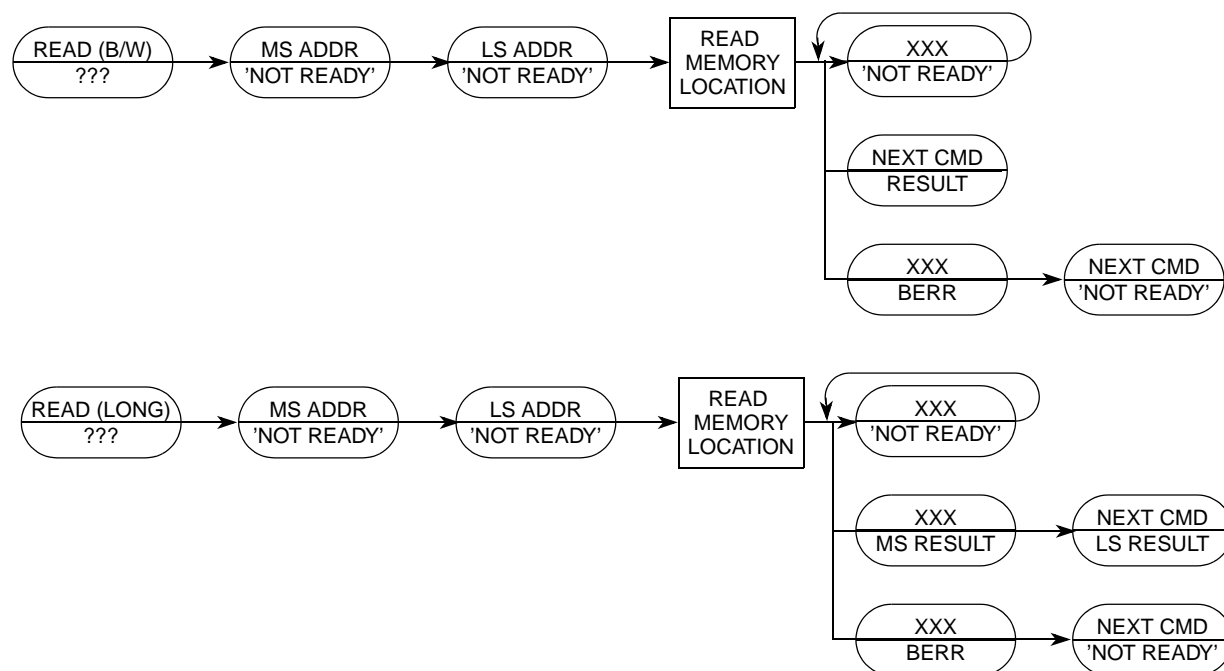


Figure 26-22. READ Command Sequence

Operand Data: The only operand is the longword address of the requested location.

Result Data: Word results return 16 bits of data; longword results return 32. Bytes are returned in the LSB of a word result; the upper byte is undefined. 0x0001 (S = 1) is returned if a bus error occurs.

26.4.1.5.4 Write Memory Location (WRITE)

Write data to the memory location specified by the longword address. BAAR[TT,TM] defines address space. Hardware forces low-order address bits to 0s for word and longword accesses to ensure that word addresses are word-aligned and longword addresses are longword-aligned.

Command Formats:

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Byte	0x1				0x8				0x0				0x0			
	A[31:16]															
	A[15:0]															
	X	X	X	X	X	X	X	X	D[7:0]							
Word	0x1				0x8				0x4				0x0			
	A[31:16]															
	A[15:0]															
	D[15:0]															
Longword	0x1				0x8				0x8				0x0			
	A[31:16]															
	A[15:0]															
	D[31:16]															
	D[15:0]															

Figure 26-23. WRITE Command Format

Command Sequence:

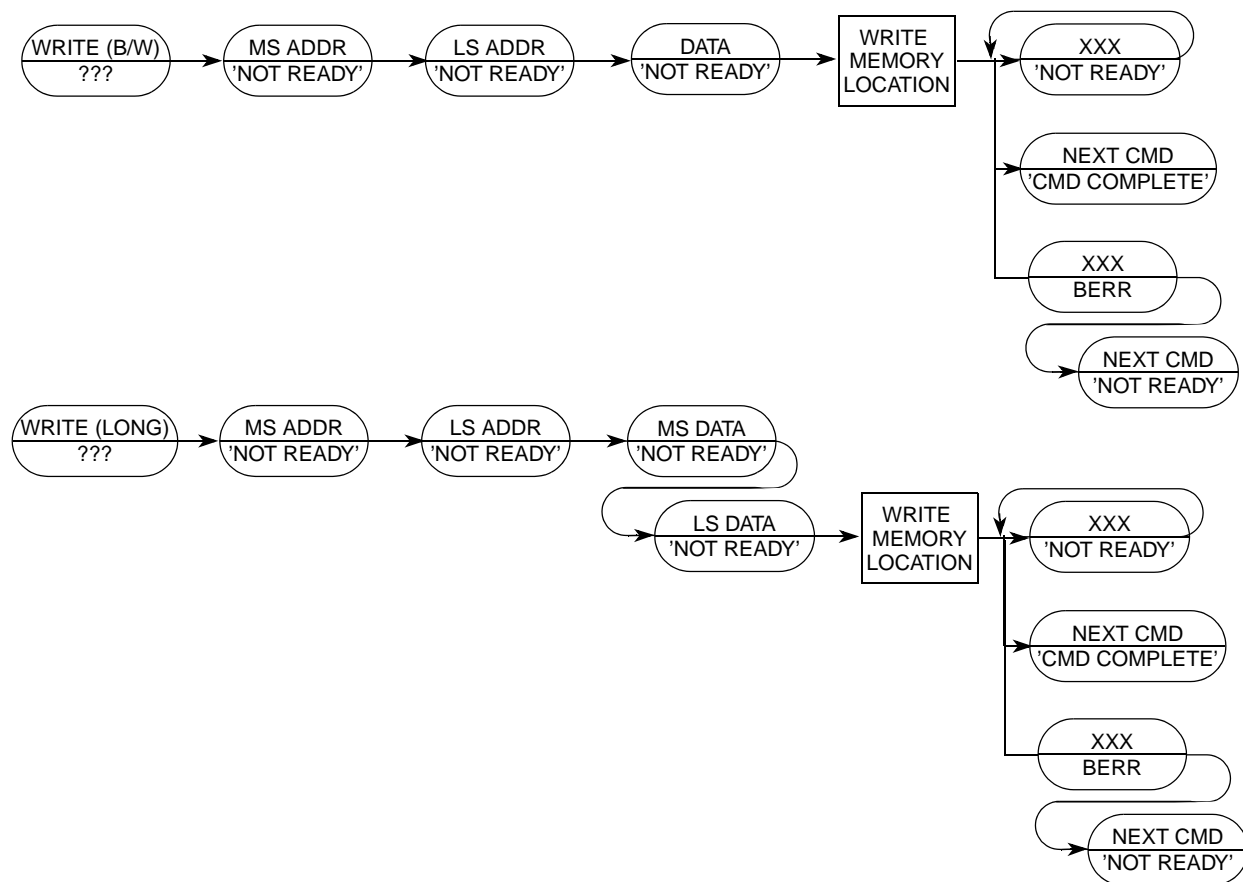


Figure 26-24. WRITE Command Sequence

- Operand Data:** This two-operand instruction requires a longword absolute address that specifies a location the data operand is written. Byte data is sent as a 16-bit word, justified in the LSB; 16- and 32-bit operands are sent as 16 and 32 bits, respectively.
- Result Data:** Command complete status is indicated by returning 0xFFFF (with S cleared) when the register write is complete. A value of 0x0001 (with S set) is returned if a bus error occurs.

26.4.1.5.5 Dump Memory Block (DUMP)

DUMP is used with the READ command to access large blocks of memory. An initial READ is executed to set up the starting address of the block and to retrieve the first result. If an initial READ is not executed before the first DUMP, an illegal command response is returned. The DUMP command retrieves subsequent operands. The initial address increments by the operand size (1, 2, or 4) and saves in a temporary register. Subsequent DUMP commands use this address, perform the memory read, increment it by the current operand size, and store the updated address in the temporary register.

NOTE

DUMP does not check for a valid address; it is a valid command only when preceded by NOP, READ, or another DUMP command. Otherwise, an illegal command response is returned. NOP can be used for intercommand padding without corrupting the address pointer.

The size field is examined each time a DUMP command is processed, allowing the operand size to be dynamically altered.

Command/Result Formats:

		15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Byte	Command	0x1				0xD				0x0				0x0			
	Result	X	X	X	X	X	X	X	X	D[7:0]							
Word	Command	0x1				0xD				0x4				0x0			
	Result	D[15:0]															
Longword	Command	0x1				0xD				0x8				0x0			
	Result	D[31:16]															
		D[15:0]															

Figure 26-25. DUMP Command/Result Formats

Command Sequence:

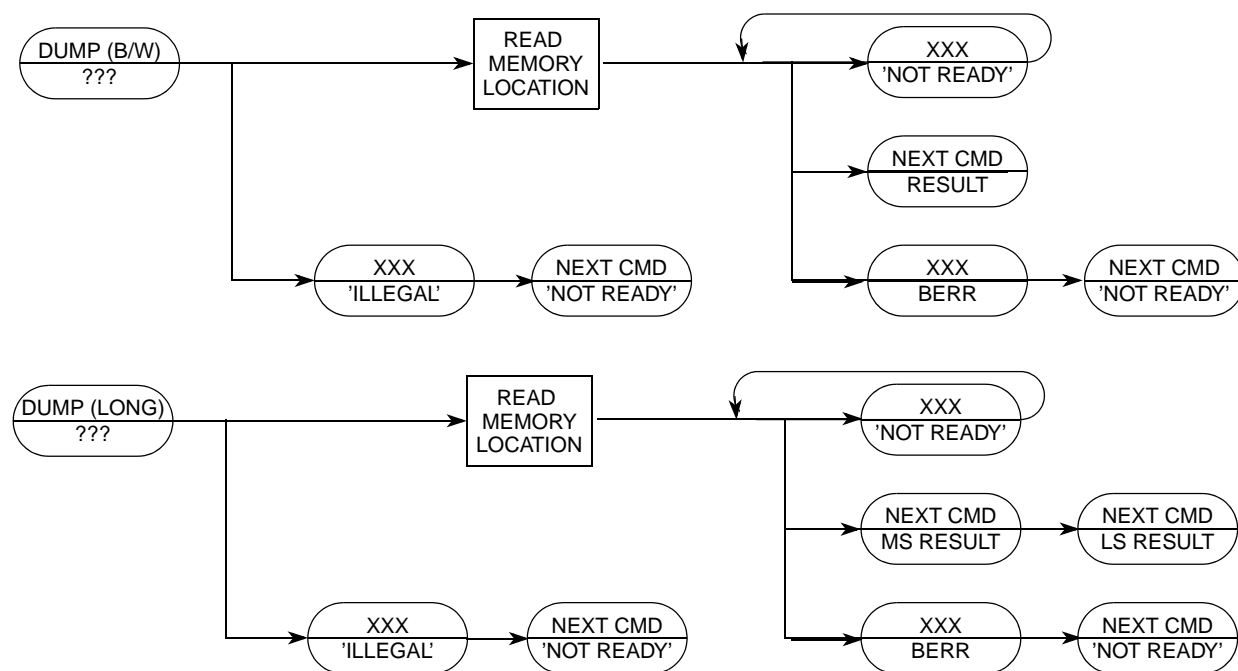


Figure 26-26. DUMP Command Sequence

Operand Data: None

Result Data: Requested data is returned as a word or longword. Byte data is returned in the least-significant byte of a word result. Word results return 16 bits of significant data; longword results return 32 bits. A value of 0x0001 (with S set) is returned if a bus error occurs.

26.4.1.5.6 Fill Memory Block (FILL)

A FILL command is used with the WRITE command to access large blocks of memory. An initial WRITE is executed to set up the starting address of the block and to supply the first operand. The FILL command writes subsequent operands. The initial address increments by the operand size (1, 2, or 4) and saves in a temporary register after the memory write. Subsequent FILL commands use this address, perform the write, increment it by the current operand size, and store the updated address in the temporary register.

If an initial WRITE is not executed preceding the first FILL command, the illegal command response is returned.

NOTE

The FILL command does not check for a valid address: FILL is a valid command only when preceded by another FILL, a NOP, or a WRITE command. Otherwise, an illegal command response is returned. The NOP command can be used for intercommand padding without corrupting the address pointer.

The size field is examined each time a FILL command is processed, allowing the operand size to be altered dynamically.

Command Formats:

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Byte	0x1				0xC				0x0				0x0			
	X	X	X	X	X	X	X	X	D[7:0]							
Word	0x1				0xC				0x4				0x0			
	D[15:0]															
Longword	0x1				0xC				0x8				0x0			
	D[31:16]															
	D[15:0]															

Figure 26-27. FILL Command Format

Command Sequence:

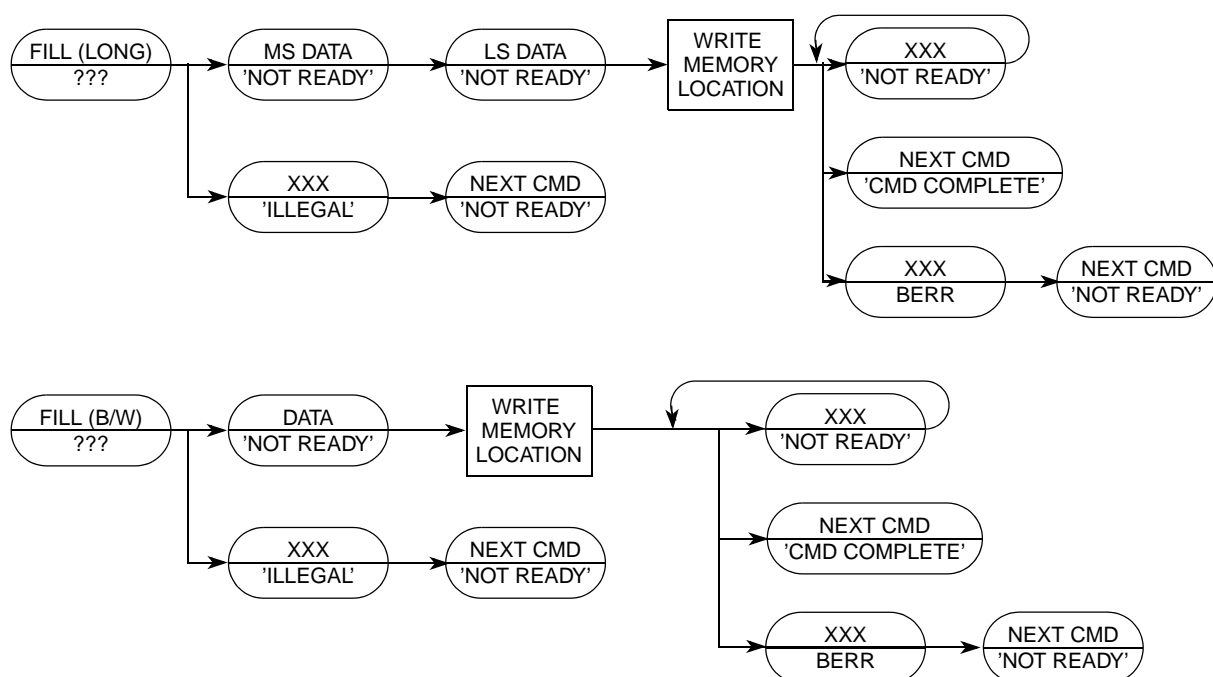


Figure 26-28. FILL Command Sequence

Operand Data: A single operand is data to be written to the memory location. Byte data is sent as a 16-bit word, justified in the least-significant byte; 16- and 32-bit operands are sent as 16 and 32 bits, respectively.

Result Data: Command complete status (0xFFFF) is returned when the register write is complete. A value of 0x0001 (with S set) is returned if a bus error occurs.

26.4.1.5.7 Resume Execution (go)

The pipeline is flushed and refilled before normal instruction execution resumes. Prefetching begins at the current address in the PC and at the current privilege level. If any register (such as the PC or SR) is altered by a BDM command while the processor is halted, the updated value is used when prefetching resumes. If a GO command issues and the CPU is not halted, the command is ignored.

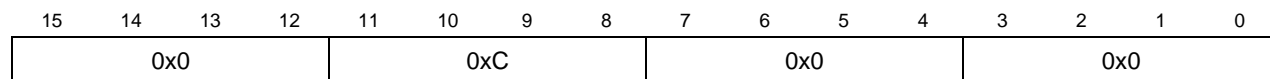


Figure 26-29. go Command Format

Command Sequence:

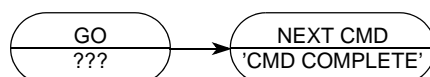


Figure 26-30. go Command Sequence

Operand Data: None

Result Data: The command-complete response (0xFFFF) is returned during the next shift operation.

26.4.1.5.8 No Operation (NOP)

NOP performs no operation and may be used as a null command where required.

Command Formats:

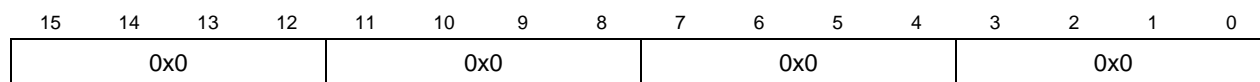


Figure 26-31. NOP Command Format

Command Sequence:

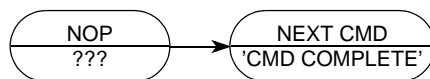


Figure 26-32. NOP Command Sequence

Operand Data: None

Result Data: The command-complete response, 0xFFFF (with S cleared), is returned during the next shift operation.

26.4.1.5.9 Synchronize PC to the PST/DDATA Lines (SYNC_PC)

The SYNC_PC command captures the current PC and displays it on the PST/DDATA outputs. After the debug module receives the command, it sends a signal to the ColdFire processor that the current PC must be displayed. The processor then forces an instruction fetch at the next PC with the address being captured in the DDATA logic under control of the CSR[BTB] bits. The specific sequence of PST and DDATA values is defined below:

1. Debug signals a SYNC_PC command is pending.
2. CPU completes the current instruction.
3. CPU forces an instruction fetch to the next PC, generates a PST equaling 0x5 value indicating a taken branch and signals the capture of DDATA.
4. The instruction address corresponding to the PC is captured.
5. The PST marker (0x9–0xB) is generated and displayed as defined by the CSR[BTB] bit followed by the captured PC address.

The SYNC_PC command can be used to dynamically access the PC for performance monitoring. The execution of this command is considerably less obtrusive to the real-time operation of an application than a HALT-CPU/READ-PC/RESUME command sequence.

Command Formats:

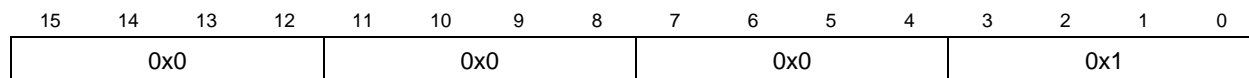


Figure 26-33. SYNC_PC Command Format

Command Sequence:

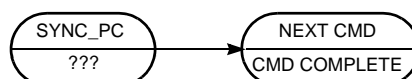


Figure 26-34. SYNC_PC Command Sequence

Operand Data: None

Result Data: Command complete status (0xFFFF) is returned when the register write is complete.

26.4.1.5.10 Read Control Register (RCREG)

Read the selected control register and return the 32-bit result. Accesses to the processor/memory control registers are always 32 bits wide, regardless of register width. The second and third words of the command form a 32-bit address, which the debug module uses to generate a special bus cycle to access the specified control register. The 12-bit Rc field is the same the processor's MOVEC instruction uses.

Command/Result Formats:

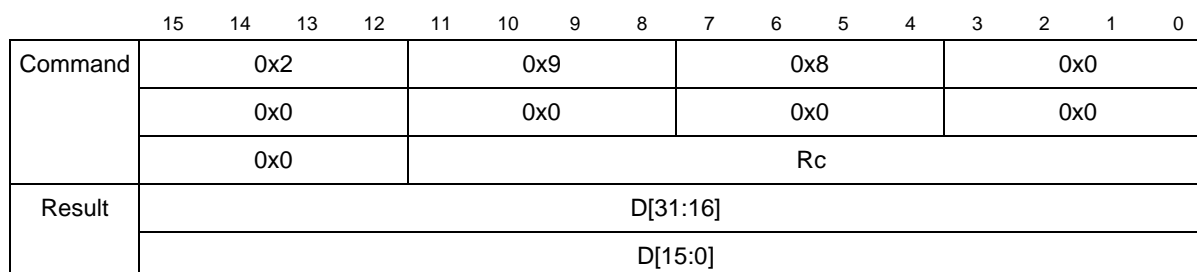


Figure 26-35. RCREG Command/Result Formats

Command Sequence:

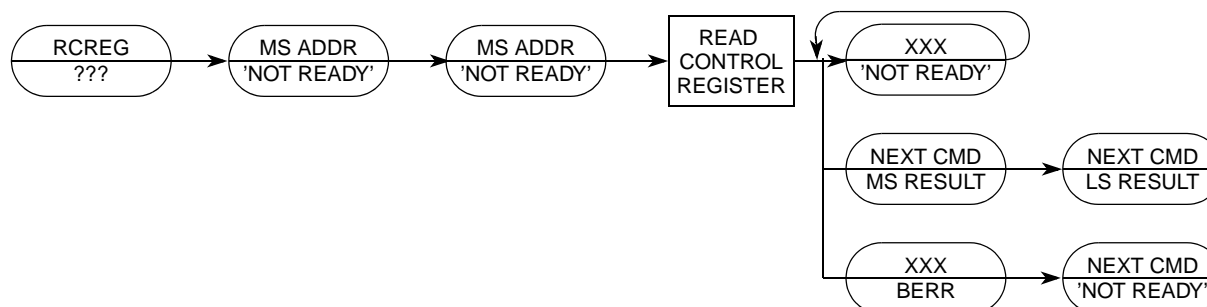


Figure 26-36. RCREG Command Sequence

Operand Data: The only operand is the 32-bit Rc control register select field.

Result Data: Control register contents are returned as a longword, most-significant word first. The implemented portion of registers smaller than 32 bits is guaranteed correct; other bits are undefined.

Rc encoding: See [Table 26-21](#).

Table 26-21. Control Register Map

Rc	Register Definition
0x002	Cache Control Register (CACR)
0x004	Access Control Register (ACR0)
0x005	Access Control Register (ACR1)
0x009	RGPIO Base Address Register (RGPIOBAR) ¹
0x(0,1)80 – 0x(0,1)87	Data Registers 0–7 (0 = load, 1 = store)
0x(0,1)88 – 0x(0,1)8F	Address Registers 0–7 (0 = load, 1 = store) (A7 is user stack pointer)
0x800	Other Stack Pointer (OTHER_A7)
0x801	Vector Base Register (VBR)
0x804	MAC Status Register (MACSR)
0x805	MAC Mask Register (MASK)
0x806	MAC Accumulator 0 (ACC0)
0x807	MAC Accumulator 0,1 Extension Bytes (ACCEXT01)
0x808	MAC Accumulator 2,3 Extension Bytes (ACCEXT23)
0x809	MAC Accumulator 1 (ACC1)
0x80A	MAC Accumulator 2 (ACC2)
0x80B	MAC Accumulator 3 (ACC3)
0x80E	Status Register (SR)
0x80F	Program Register (PC)
0xC05	RAM Base Address Register (RAMBAR)

¹ If an RGPIO module is available on this device.

26.4.1.5.11 BDM Accesses of the Stack Pointer Registers (A7: SSP and USP)

The ColdFire core supports two unique stack pointer (A7) registers: the supervisor stack pointer (SSP) and the user stack pointer (USP). The hardware implementation of these two programmable-visible 32-bit registers does not uniquely identify one as the SSP and the other as the USP. Rather, the hardware uses one 32-bit register as the currently-active A7; the other is named the OTHER_A7. Therefore, the contents of the two hardware registers is a function of the operating mode of the processor:

```

if SR[S] = 1
then      A7 = Supervisor Stack Pointer
          OTHER_A7 = User Stack Pointer
else      A7 = User Stack Pointer
          OTHER_A7 = Supervisor Stack Pointer

```

The BDM programming model supports reads and writes to A7 and OTHER_A7 directly. It is the responsibility of the external development system to determine the mapping of A7 and OTHER_A7 to the two program-visible definitions (supervisor and user stack pointers), based on the SR[S] bit.

26.4.1.5.12 BDM Accesses of the EMAC Registers

The presence of rounding logic in the output datapath of the EMAC requires special care for BDM-initiated reads and writes of its programming model. In particular, any result rounding modes must be disabled during the read/write process so the exact bit-wise EMAC register contents are accessed.

For example, a BDM read of an accumulator (ACCx) must be preceded by two commands accessing the MAC status register, as shown in the following sequence:

```
BdmReadACCx (
    rcreg    macsr;           // read current macsr contents and save
    wcreg    #0,macsr;        // disable all rounding modes
    rcreg    ACCx;            // read the desired accumulator
    wcreg    #saved_data,macsr; // restore the original macsr
)
```

Likewise, to write an accumulator register, the following BDM sequence is needed:

```
BdmWriteACCx (
    rcreg    macsr;           // read current macsr contents and save
    wcreg    #0,macsr;        // disable all rounding modes
    wcreg    #data,ACCx;      // write the desired accumulator
    wcreg    #saved_data,macsr; // restore the original macsr
)
```

Additionally, writes to the accumulator extension registers must be performed after the corresponding accumulators are updated because a write to any accumulator alters the corresponding extension register contents.

For more information on saving and restoring the complete EMAC programming model, see [Section 4.3.1.2, “Saving and Restoring the EMAC Programming Model.”](#)

26.4.1.5.13 Write Control Register (WCREG)

The operand (longword) data is written to the specified control register. The write alters all 32 register bits. See the RCREG instruction description for the Rc encoding and for additional notes on writes to the A7 stack pointers and the EMAC programming model.

Command/Result Formats:

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Command	0x2				0x8				0x8				0x0			
	0x0				0x0				0x0				0x0			
	0x0				Rc											
Result	D[31:16]															
	D[15:0]															

Figure 26-37. WCREG Command/Result Formats

Command Sequence:

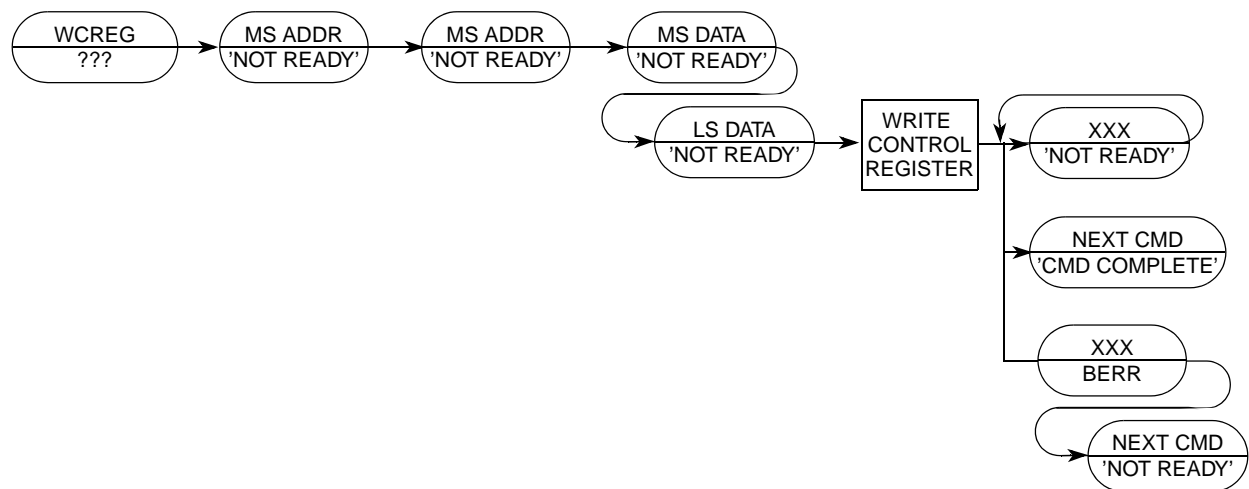


Figure 26-38. WCREG Command Sequence

Operand Data: This instruction requires two longword operands. The first selects the register to the operand data writes to; the second contains the data.

Result Data: Successful write operations return 0xFFFF. Bus errors on the write cycle are indicated by the setting of bit 16 in the status message and by a data pattern of 0x0001.

26.4.1.5.14 Read Debug Module Register (RDMREG)

Read the selected debug module register and return the 32-bit result. The only valid register selection for the RDMREG command is CSR.

Command/Result Formats:

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Command	0x2				0xD				100			DRc				
Result	D[31:16]															
	D[15:0]															

Figure 26-39. RDMREG Command/Result Formats

Table 26-22 shows the definition of DRc encoding.

Table 26-22. Definition of DRc Encoding—Read

DRc[4:0]	Debug Register Definition	Mnemonic
0x00	Configuration/Status	CSR

Command Sequence:

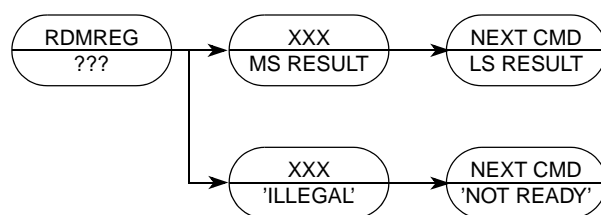


Figure 26-40. RDMREG Command Sequence

Operand Data: None

Result Data: The contents of the selected debug register are returned as a longword value. The data is returned most-significant word first.

26.4.1.5.15 Write Debug Module Register (WDMREG)

The operand (longword) data is written to the specified debug module register. All 32 bits of the register are altered by the write. DSCLK must be inactive while the debug module register writes from the CPU accesses are performed using the WDEBUG instruction.

Command Format:

Figure 26-41. WDMREG BDM Command Format

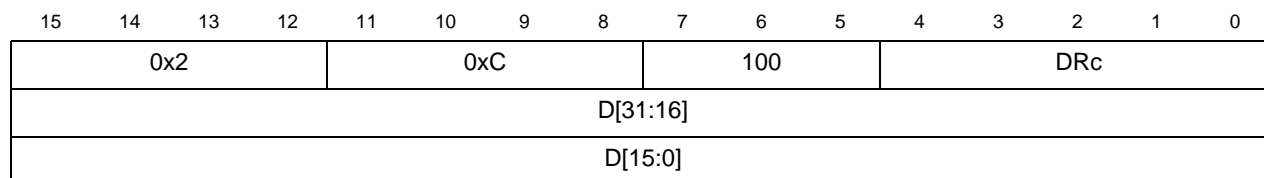


Table 26-3 shows the definition of the DRc write encoding.

Command Sequence:

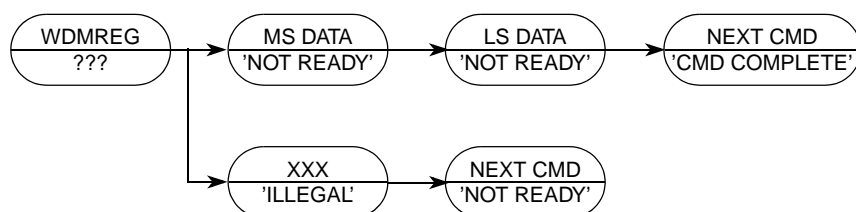


Figure 26-42. WDMREG Command Sequence

Operand Data: Longword data is written into the specified debug register. The data is supplied most-significant word first.

Result Data: Command complete status (0xFFFF) is returned when register write is complete.

26.4.2 Real-Time Debug Support

The ColdFire family provides support debugging real-time applications. For these types of embedded systems, the processor must continue to operate during debug. The foundation of this area of debug support is that while the processor cannot be halted to allow debugging, the system can generally tolerate the small intrusions of the BDM inserting instructions into the pipeline with minimal effect on real-time operation.

The debug module provides four types of breakpoints: PC with mask, PC without mask, operand address range, and data with mask. These breakpoints can be configured into one- or two-level triggers with the exact trigger response also programmable. The debug module programming model can be written from the external development system using the debug serial interface or from the processor's supervisor programming model using the WDEBUG instruction. Only CSR is readable using the external development system.

26.4.2.1 Theory of Operation

Breakpoint hardware can be configured through TDR[TCR] to respond to triggers by displaying DDATA, initiating a processor halt, or generating a debug interrupt. As shown in Table 26-23, when a breakpoint is triggered, an indication (CSR[BSTAT]) is provided on the DDATA output port when it is not displaying captured processor status, operands, or branch addresses.

Table 26-23. DDATA[3:0]/CSR[BSTAT] Breakpoint Response

DDATA[3:0] ¹	CSR[BSTAT] ¹	Breakpoint Status
0000	0000	No breakpoints enabled
0010	0001	Waiting for level-1 breakpoint
0100	0010	Level-1 breakpoint triggered
1010	0101	Waiting for level-2 breakpoint
1100	0110	Level-2 breakpoint triggered

¹ Encodings not shown are reserved for future use.

The breakpoint status is also posted in the CSR. CSR[BSTAT] is cleared by a CSR read when a level-2 breakpoint is triggered or a level-1 breakpoint is triggered and a level-2 breakpoint is not enabled. Status is also cleared by writing to TDR to disable trigger options.

BDM instructions use the appropriate registers to load and configure breakpoints. As the system operates, a breakpoint trigger generates the response defined in TDR.

PC breakpoints are treated in a precise manner—exception recognition and processing are initiated before the excepting instruction executes. All other breakpoint events are recognized on the processor's local bus, but are made pending to the processor and sampled like other interrupt conditions. As a result, these interrupts are imprecise.

In systems that tolerate the processor being halted, a BDM-entry can be used. With TDR[TRC] equals 01, a breakpoint trigger causes the core to halt (PST = 0xF).

If the processor core cannot be halted, the debug interrupt can be used. With this configuration, TDR[TRC] equals 10, breakpoint trigger becomes a debug interrupt to the processor, which is treated

higher than the nonmaskable level-7 interrupt request. As with all interrupts, it is made pending until the processor reaches a sample point, which occurs once per instruction. Again, the hardware forces the PC breakpoint to occur before the targeted instruction executes and is precise. This is possible because the PC breakpoint is enabled when interrupt sampling occurs. For address and data breakpoints, reporting is considered imprecise, because several instructions may execute after the triggering address or data is detected.

As soon as the debug interrupt is recognized, the processor aborts execution and initiates exception processing. This event is signaled externally by the assertion of a unique PST value ($PST = 0xD$) for multiple cycles. The core enters emulator mode when exception processing begins. After the standard 8-byte exception stack is created, the processor fetches a unique exception vector, 12, from the vector table. Refer to the *ColdFire Programmer's Reference Manual* for more information.

Execution continues at the instruction address in the vector corresponding to the debug interrupt. All interrupts are ignored while the processor is in emulator mode. The debug interrupt handler can use supervisor instructions to save the necessary context, such as the state of all program-visible registers into a reserved memory area.

When debug interrupt operations complete, the RTE instruction executes and the processor exits emulator mode. After the debug interrupt handler completes execution, the external development system can use BDM commands to read the reserved memory locations.

In revision B/B+, the hardware inhibits generation of another debug interrupt during the first instruction after the RTE exits emulator mode. This behavior is consistent with the logic involving trace mode where the first instruction executes before another trace exception is generated. Thus, all hardware breakpoints are disabled until the first instruction after the RTE completes execution, regardless of the programmed trigger response.

26.4.2.2 Emulator Mode

Emulator mode facilitates non-intrusive emulator functionality. This mode can be entered in three different ways:

- Setting CSR[EMU] forces the processor into emulator mode. EMU is examined only if \overline{RSTI} is negated and the processor begins reset exception processing. It can be set while the processor is halted before reset exception processing begins. See [Section 26.4.1.1, “CPU Halt”](#).
- A debug interrupt always puts the processor in emulation mode when debug interrupt exception processing begins.
- Setting CSR[TRC] forces the processor into emulation mode when trace exception processing begins.

While operating in emulation mode, the processor exhibits the following properties:

- All interrupts are ignored, including level-7 interrupts.
- If CSR[MAP] is set, all caching of memory and the SRAM module are disabled. All memory accesses are forced into a specially mapped address space signaled by TT equals 0x2, TM equals 0x5, or 0x6. This includes stack frame writes and vector fetch for the exception that forced entry into this mode.

The RTE instruction exits emulation mode. The processor status output port provides a unique encoding for emulator mode entry (0xD) and exit (0x7).

26.4.3 Concurrent BDM and Processor Operation

The debug module supports concurrent operation of the processor and most BDM commands. BDM commands may be executed while the processor is running, except these following operations that access processor/memory registers:

- Read/write address and data registers
- Read/write control registers

For BDM commands that access memory, the debug module requests the processor's local bus. The processor responds by stalling the instruction fetch pipeline and waiting for current bus activity to complete before freeing the local bus for the debug module to perform its access. After the debug module bus cycle, the processor reclaims the bus.

NOTE

Breakpoint registers must be carefully configured in a development system if the processor is executing. The debug module contains no hardware interlocks, so TDR should be disabled while breakpoint registers are loaded, after which TDR can be written to define the exact trigger. This prevents spurious breakpoint triggers.

Because there are no hardware interlocks in the debug unit, no BDM operations are allowed while the CPU is writing the debug's registers (DSCLK must be inactive).

NOTE

The debug module requires the use of the internal bus to perform BDM commands. For this processor core, if the processor is executing a tight loop contained within a single aligned longword, the processor may never grant the internal bus to the debug module, for example:

```

                align4
label1:  nop
                bra.b label1
or
                align4
label2:  bra.w label2

```

The processor grants the internal bus if these loops are forced across two longwords.

26.4.4 Real-Time Trace Support

Real-time trace, which defines the dynamic execution path and is also known as instruction trace, is a fundamental debug function. The ColdFire solution is to include a parallel output port providing encoded processor status and data to an external development system. This port is partitioned into two 4-bit nibbles: one nibble allows the processor to transmit processor status, (PST), and the other allows operand data to

be displayed (debug data, DDATA). The processor status may not be related to the current bus transfer, due to the decoupling FIFOs.

External development systems can use PST outputs with an external image of the program to completely track the dynamic execution path. This tracking is complicated by any change in flow, where branch target address calculation is based on the contents of a program-visible register (variant addressing). DDATA outputs can display the target address of such instructions in sequential nibble increments across multiple processor clock cycles, as described in [Section 26.4.4.1, “Begin Execution of Taken Branch \(PST = 0x5\)”](#). Two 32-bit storage elements form a FIFO buffer connecting the processor’s high-speed local bus to the external development system through PST[3:0] and DDATA[3:0]. The buffer captures branch target addresses and certain data values for eventual display on the DDATA port, one nibble at a time starting with the least significant bit (lsb).

Execution speed is affected only when both storage elements contain valid data to be dumped to the DDATA port. The core stalls until one FIFO entry is available.

[Table 26-24](#) shows the encoding of these signals.

Table 26-24. Processor Status Encoding

PST[3:0]	Definition
0x0	Continue execution. Many instructions execute in one processor cycle. If an instruction requires more clock cycles, subsequent clock cycles are indicated by driving PST outputs with this encoding.
0x1	Begin execution of one instruction. For most instructions, this encoding signals the first processor clock cycle of an instruction’s execution. Certain change-of-flow opcodes, plus the PULSE and WDDATA instructions, generate different encodings.
0x2	Reserved
0x3	Entry into user-mode. Signaled after execution of the instruction that caused the ColdFire processor to enter user mode.
0x4	Begin execution of PULSE and WDDATA instructions. PULSE defines logic analyzer triggers for debug and/or performance analysis. WDDATA lets the core write any operand (byte, word, or longword) directly to the DDATA port, independent of debug module configuration. When WDDATA is executed, a value of 0x4 is signaled on the PST port, followed by the appropriate marker, and then the data transfer on the DDATA port. Transfer length depends on the WDDATA operand size.
0x5	Begin execution of taken branch or SYNC_PC command issued. For some opcodes, a branch target address may be displayed on DDATA depending on the CSR settings. CSR also controls the number of address bytes displayed, indicated by the PST marker value preceding the DDATA nibble that begins the data output. See Section 26.4.4.1, “Begin Execution of Taken Branch (PST = 0x5)” . Also indicates that the SYNC_PC command has been issued.
0x6	Reserved
0x7	Begin execution of return from exception (RTE) instruction.
0x8–0xB	Indicates the number of bytes to be displayed on the DDATA port on subsequent clock cycles. The value is driven onto the PST port one PSTCLK cycle before the data is displayed on DDATA. 0x8 Begin 1-byte transfer on DDATA. 0x9 Begin 2-byte transfer on DDATA. 0xA Begin 3-byte transfer on DDATA. 0xB Begin 4-byte transfer on DDATA.

Table 26-24. Processor Status Encoding (continued)

PST[3:0]	Definition
0xC	Normal exception processing. Exceptions that enter emulation mode (debug interrupt or optionally trace) generate a different encoding, as described below. Because the 0xC encoding defines a multiple-cycle mode, PST outputs are driven with 0xC until exception processing completes.
0xD	Emulator mode exception processing. Displayed during emulation mode (debug interrupt or optionally trace). Because this encoding defines a multiple-cycle mode, PST outputs are driven with 0xD until exception processing completes.
0xE	Processor is stopped. Appears in multiple-cycle format when the processor executes a STOP instruction. The ColdFire processor remains stopped until an interrupt occurs, thus PST outputs display 0xE until the stopped mode is exited.
0xF	Processor is halted. Because this encoding defines a multiple-cycle mode, the PST outputs display 0xF until the processor is restarted or reset. See Section 26.4.1.1, “CPU Halt” .

26.4.4.1 Begin Execution of Taken Branch (PST = 0x5)

PST is 0x5 when a taken branch is executed. For some opcodes, a branch target address may be displayed on DDATA depending on the CSR settings. CSR also controls the number of address bytes displayed, which is indicated by the PST marker value immediately preceding the DDATA nibble that begins the data output.

Multiple byte DDATA values are displayed in least-to-most-significant order. The processor captures only those target addresses associated with taken branches that use a variant addressing mode (RTE and RTS instructions, JMP and JSR instructions using address register indirect or indexed addressing modes, and all exception vectors).

The simplest example of a branch instruction using a variant address is the compiled code for a C language case statement. Typically, the evaluation of this statement uses the variable of an expression as an index into a table of offsets, where each offset points to a unique case within the structure. For such change-of-flow operations, the ColdFire processor uses the debug pins to output the following sequence of information on two successive processor clock cycles:

1. Use PST (0x5) to identify that a taken branch is executed.
2. Using the PST pins, optionally signal the target address to be displayed sequentially on the DDATA pins. Encodings 0x9–0xB identify the number of bytes displayed.
3. The new target address is optionally available on subsequent cycles using the DDATA port. The number of bytes of displayed on this port is configurable (2, 3, or 4 bytes, where the DDATA encoding is 0x9, 0xA, and 0xB, respectively).

Another example of a variant branch instruction would be a JMP (A0) instruction. [Figure 26-43](#) shows the PST and DDATA outputs that indicate a JMP (A0) execution, assuming the CSR was programmed to display the lower 2 bytes of an address.

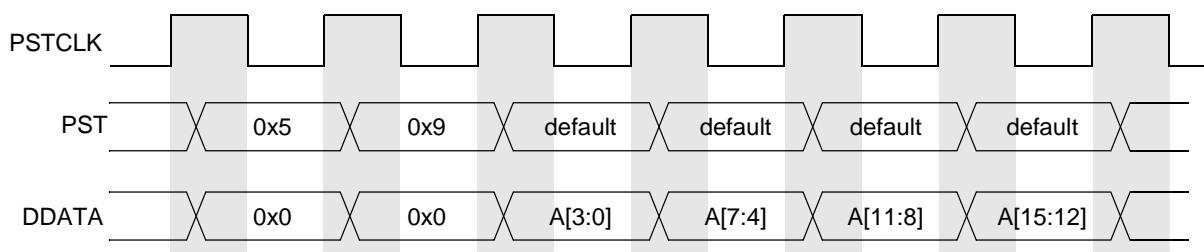


Figure 26-43. Example JMP Instruction Output on PST/DDATA

PST of 0x5 indicates a taken branch and the marker value 0x9 indicates a 2-byte address. Therefore, the subsequent 4 nibbles of DDATA display the lower two bytes of address register A0 in least-to-most-significant nibble order. The PST output after the JMP instruction completes depends on the target instruction. The PST can continue with the next instruction before the address has completely displayed on DDATA because of the DDATA FIFO. If the FIFO is full and the next instruction has captured values to display on DDATA, the pipeline stalls (PST = 0x0) until space is available in the FIFO.

26.4.5 Processor Status, Debug Data Definition

This section specifies the ColdFire processor and debug module's generation of the processor status (PST) and debug data (DDATA) output on an instruction basis. In general, the PST/DDATA output for an instruction is defined as follows:

PST = 0x1, {PST = [0x89B], DDATA = operand}

where the {...} definition is optional operand information defined by the setting of the CSR.

The CSR provides capabilities to display operands based on reference type (read, write, or both). A PST value {0x8, 0x9, or 0xB} identifies the size and presence of valid data to follow on the DDATA output {1, 2, or 4 bytes}. Additionally, for certain change-of-flow branch instructions, CSR[BTB] provides the capability to display the target instruction address on the DDATA output {2, 3, or 4 bytes} using a PST value of {0x9, 0xA, or 0xB}.

26.4.5.1 User Instruction Set

Table 26-25 shows the PST/DDATA specification for user-mode instructions. Rn represents any {Dn, An} register. In this definition, the y suffix generally denotes the source, and x denotes the destination operand. For a given instruction, the optional operand data is displayed only for those effective addresses referencing memory. The DD nomenclature refers to the DDATA outputs.

Table 26-25. PST/DDATA Specification for User-Mode Instructions

Instruction	Operand Syntax	PST/DDATA
add.l	<ea>y,Dx	PST = 0x1, {PST = 0xB, DD = source operand}
add.l	Dy,<ea>x	PST = 0x1, {PST = 0xB, DD = source}, {PST = 0xB, DD = destination}
adda.l	<ea>y,Ax	PST = 0x1, {PST = 0xB, DD = source operand}
addi.l	#<data>,Dx	PST = 0x1

Table 26-25. PST/DDATA Specification for User-Mode Instructions (continued)

Instruction	Operand Syntax	PST/DDATA
addq.l	#<data>,<ea>x	PST = 0x1, {PST = 0xB, DD = source}, {PST = 0xB, DD = destination}
addx.l	Dy,Dx	PST = 0x1
and.l	<ea>y,Dx	PST = 0x1, {PST = 0xB, DD = source operand}
and.l	Dy,<ea>x	PST = 0x1, {PST = 0xB, DD = source}, {PST = 0xB, DD = destination}
andi.l	#<data>,Dx	PST = 0x1
asl.l	{Dy,#<data>},Dx	PST = 0x1
asr.l	{Dy,#<data>},Dx	PST = 0x1
bcc.{b,w}		if taken, then PST = 0x5, else PST = 0x1
bchg.{b,l}	#<data>,<ea>x	PST = 0x1, {PST = 0x8, DD = source}, {PST = 0x8, DD = destination}
bchg.{b,l}	Dy,<ea>x	PST = 0x1, {PST = 0x8, DD = source}, {PST = 0x8, DD = destination}
bclr.{b,l}	#<data>,<ea>x	PST = 0x1, {PST = 0x8, DD = source}, {PST = 0x8, DD = destination}
bclr.{b,l}	Dy,<ea>x	PST = 0x1, {PST = 0x8, DD = source}, {PST = 0x8, DD = destination}
bitrev.l	Dx	PST = 0x1
bra.{b,w}		PST = 0x5
bset.{b,l}	#<data>,<ea>x	PST = 0x1, {PST = 0x8, DD = source}, {PST = 0x8, DD = destination}
bset.{b,l}	Dy,<ea>x	PST = 0x1, {PST = 0x8, DD = source}, {PST = 0x8, DD = destination}
bsr.{b,w}		PST = 0x5, {PST = 0xB, DD = destination operand}
btst.{b,l}	#<data>,<ea>x	PST = 0x1, {PST = 0x8, DD = source operand}
btst.{b,l}	Dy,<ea>x	PST = 0x1, {PST = 0x8, DD = source operand}
byterev.l	Dx	PST = 0x1
clr.b	<ea>x	PST = 0x1, {PST = 0x8, DD = destination operand}
clr.l	<ea>x	PST = 0x1, {PST = 0xB, DD = destination operand}
clr.w	<ea>x	PST = 0x1, {PST = 0x9, DD = destination operand}
cmp.l	<ea>y,Dx	PST = 0x1, {PST = 0xB, DD = source operand}
cmpa.l	<ea>y,Ax	PST = 0x1, {PST = 0xB, DD = source operand}
cmpi.l	#<data>,Dx	PST = 0x1
divs.l	<ea>y,Dx	PST = 0x1, {PST = 0xB, DD = source operand}
divs.w	<ea>y,Dx	PST = 0x1, {PST = 0x9, DD = source operand}
divu.l	<ea>y,Dx	PST = 0x1, {PST = 0xB, DD = source operand}
divu.w	<ea>y,Dx	PST = 0x1, {PST = 0x9, DD = source operand}
eor.l	Dy,<ea>x	PST = 0x1, {PST = 0xB, DD = source}, {PST = 0xB, DD = destination}
eorl.l	#<data>,Dx	PST = 0x1
ext.l	Dx	PST = 0x1

Table 26-25. PST/DDATA Specification for User-Mode Instructions (continued)

Instruction	Operand Syntax	PST/DDATA
ext.w	Dx	PST = 0x1
extb.l	Dx	PST = 0x1
illegal		PST = 0x1 ¹
jmp	<ea>y	PST = 0x5, {PST = [0x9AB], DD = target address} ²
jsr	<ea>y	PST = 0x5, {PST = [0x9AB], DD = target address}, {PST = 0xB, DD = destination operand} ²
lea.l	<ea>y,Ax	PST = 0x1
link.w	Ay,#<displacement>	PST = 0x1, {PST = 0xB, DD = destination operand}
lsl.l	{Dy,#<data>},Dx	PST = 0x1
lsr.l	{Dy,#<data>},Dx	PST = 0x1
move.b	<ea>y,<ea>x	PST = 0x1, {PST = 0x8, DD = source}, {PST = 0x8, DD = destination}
move.l	<ea>y,<ea>x	PST = 0x1, {PST = 0xB, DD = source}, {PST = 0xB, DD = destination}
move.w	<ea>y,<ea>x	PST = 0x1, {PST = 0x9, DD = source}, {PST = 0x9, DD = destination}
move.w	CCR,Dx	PST = 0x1
move.w	{Dy,#<data>},CCR	PST = 0x1
movea.l	<ea>y,Ax	PST = 0x1, {PST = 0xB, DD = source}
movea.w	<ea>y,Ax	PST = 0x1, {PST = 0x9, DD = source}
movem.l	#list,<ea>x	PST = 0x1, {PST = 0xB, DD = destination},... ³
movem.l	<ea>y,#list	PST = 0x1, {PST = 0xB, DD = source},... ³
moveq.l	#<data>,Dx	PST = 0x1
muls.l	<ea>y,Dx	PST = 0x1, {PST = 0xB, DD = source operand}
muls.w	<ea>y,Dx	PST = 0x1, {PST = 0x9, DD = source operand}
mulu.l	<ea>y,Dx	PST = 0x1, {PST = 0xB, DD = source operand}
mulu.w	<ea>y,Dx	PST = 0x1, {PST = 0x9, DD = source operand}
neg.l	Dx	PST = 0x1
negx.l	Dx	PST = 0x1
nop		PST = 0x1
not.l	Dx	PST = 0x1
or.l	<ea>y,Dx	PST = 0x1, {PST = 0xB, DD = source operand}
or.l	Dy,<ea>x	PST = 0x1, {PST = 0xB, DD = source}, {PST = 0xB, DD = destination}
ori.l	#<data>,Dx	PST = 0x1
pea.l	<ea>y	PST = 0x1, {PST = 0xB, DD = destination operand}
pulse		PST = 0x4

Table 26-25. PST/DDATA Specification for User-Mode Instructions (continued)

Instruction	Operand Syntax	PST/DDATA
rems.l	<ea>y,Dw:Dx	PST = 0x1, {PST = 0xB, DD = source operand}
remu.l	<ea>y,Dw:Dx	PST = 0x1, {PST = 0xB, DD = source operand}
rts		PST = 0x1, {PST = 0xB, DD = source operand}, PST = 0x5, {PST = [0x9AB], DD = target address}
scc.b	Dx	PST = 0x1
sub.l	<ea>y,Dx	PST = 0x1, {PST = 0xB, DD = source operand}
sub.l	Dy,<ea>x	PST = 0x1, {PST = 0xB, DD = source}, {PST = 0xB, DD = destination}
suba.l	<ea>y,Ax	PST = 0x1, {PST = 0xB, DD = source operand}
subi.l	#<data>,Dx	PST = 0x1
subq.l	#<data>,<ea>x	PST = 0x1, {PST = 0xB, DD = source}, {PST = 0xB, DD = destination}
subx.l	Dy,Dx	PST = 0x1
swap.w	Dx	PST = 0x1
tpf		PST = 0x1
tpf.l	#<data>	PST = 0x1
tpf.w	#<data>	PST = 0x1
trap	#<data>	PST = 0x1 ¹
tst.b	<ea>x	PST = 0x1, {PST = 0x8, DD = source operand}
tst.l	<ea>y	PST = 0x1, {PST = 0xB, DD = source operand}
tst.w	<ea>y	PST = 0x1, {PST = 0x9, DD = source operand}
unlk	Ax	PST = 0x1, {PST = 0xB, DD = destination operand}
wddata.b	<ea>y	PST = 0x4, {PST = 0x8, DD = source operand}
wddata.l	<ea>y	PST = 0x4, {PST = 0xB, DD = source operand}
wddata.w	<ea>y	PST = 0x4, {PST = 0x9, DD = source operand}

- ¹ During normal exception processing, the PST output is driven to a 0xC indicating the exception processing state. The exception stack write operands, as well as the vector read and target address of the exception handler may also be displayed.

Exception Processing:

```
PST = 0xC,
{PST = 0xB, DD = destination},          // stack frame
{PST = 0xB, DD = destination},          // stack frame
{PST = 0xB, DD = source},               // vector read
PST = 0x5, {PST = [0x9AB], DD = target} // handler PC
```

The PST/DDATA specification for the reset exception is shown below:

Exception Processing:

```
PST = 0xC,
PST = 0x5, {PST = [0x9AB], DD = target} // handler PC
```

The initial references at address 0 and 4 are never captured nor displayed because these accesses are treated as instruction fetches.

For all types of exception processing, the PST = 0xC value is driven at all times, unless the PST output is needed for one of the optional marker values or for the taken branch indicator (0x5).

- ² For JMP and JSR instructions, the optional target instruction address is displayed only for those effective address fields defining variant addressing modes. This includes the following <ea>x values: (An), (d16,An), (d8,An,Xi), (d8,PC,Xi).
- ³ For move multiple instructions (MOVEM), the processor automatically generates line-sized transfers if the operand address reaches a 0-modulo-16 boundary and there are four or more registers to be transferred. For these line-sized transfers, the operand data is never captured nor displayed, regardless of the CSR value. The automatic line-sized burst transfers are provided to maximize performance during these sequential memory access operations.

Table 26-26 shows the PST/DDATA specification for multiply-accumulate instructions.

Table 26-26. PST/DDATA Values for User-Mode Multiply-Accumulate Instructions

Instruction	Operand Syntax	PST/DDATA
mac.l	Ry,Rx,ACCx	PST = 0x1
mac.l	Ry,Rx,<ea>y,Rw,ACCx	PST = 0x1, {PST = 0xB, DD = source operand}
mac.w	Ry,Rx,ACCx	PST = 0x1
mac.w	Ry,Rx,ea,Rw,ACCx	PST = 0x1, {PST = 0xB, DD = source operand}
move.l	{Ry,#<data>},ACCx	PST = 0x1
move.l	{Ry,#<data>},MACSR	PST = 0x1
move.l	{Ry,#<data>},MASK	PST = 0x1
move.l	{Ry,#<data>},ACCext01	PST = 0x1
move.l	{Ry,#<data>},ACCext23	PST = 0x1
move.l	ACCext01,Rx	PST = 0x1
move.l	ACCext23,Rx	PST = 0x1
move.l	ACCy,ACCx	PST = 0x1
move.l	ACCy,Rx	PST = 0x1
move.l	MACSR,CCR	PST = 0x1

Table 26-26. PST/DDATA Values for User-Mode Multiply-Accumulate Instructions (continued)

Instruction	Operand Syntax	PST/DDATA
move.l	MACSR,Rx	PST = 0x1
move.l	MASK,Rx	PST = 0x1
msac.l	Ry,Rx,ACCx	PST = 0x1
msac.l	Ry,Rx,<ea>y,Rw,ACCx	PST = 0x1, {PST = 0xB, DD = source operand}
msac.w	Ry,Rx,ACCx	PST = 0x1
msac.w	Ry,Rx,<ea>y,Rw,ACCx	PST = 0x1, {PST = 0xB, DD = source operand}

26.4.5.2 Supervisor Instruction Set

The supervisor instruction set has complete access to the user mode instructions plus the opcodes shown below. The PST/DDATA specification for these opcodes is shown in [Table 26-27](#).

Table 26-27. PST/DDATA Specification for Supervisor-Mode Instructions

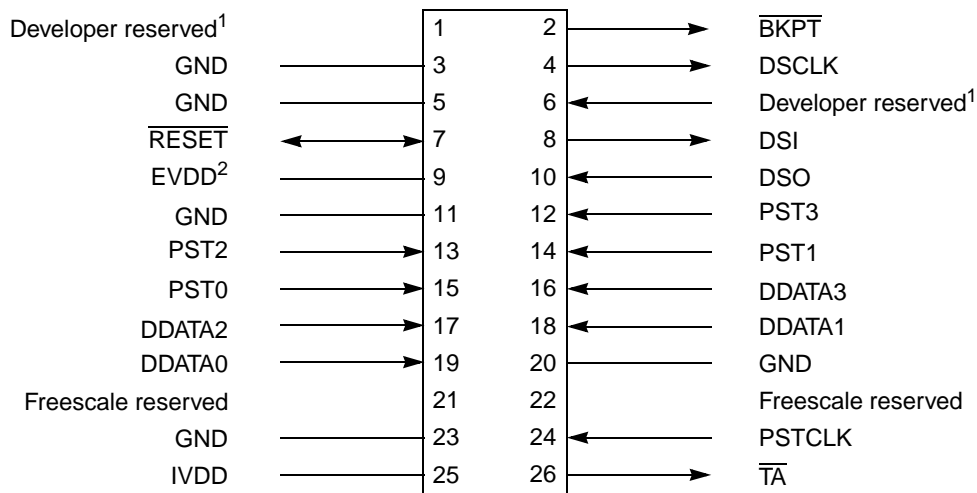
Instruction	Operand Syntax	PST/DDATA
cpushl	(Ax)	PST = 0x1
halt		PST = 0x1, PST = 0xF
move.l	Ay,USP	PST = 0x1
move.l	USP,Ax	PST = 0x1
move.w	SR,Dx	PST = 0x1
move.w	{Dy,#<data>},SR	PST = 0x1, {PST = 0x3}
movec.l	Ry,Rc	PST = 0x1
rte		PST = 0x7, {PST = 0xB, DD = source operand}, {PST = 0x3}, {PST = 0xB, DD = source operand}, PST = 0x5, {[PST = 0x9AB], DD = target address}
stldsr.w	#imm	PST = 0x1, {PST = 0xA, DD = destination operand, PST = 0x3}
stop	#<data>	PST = 0x1, PST = 0xE
wdebug.l	<ea>y	PST = 0x1, {PST = 0xB, DD = source, PST = 0xB, DD = source}

The move-to-SR and RTE instructions include an optional PST = 0x3 value, indicating an entry into user mode. Additionally, if the execution of a RTE instruction returns the processor to emulator mode, a multiple-cycle status of 0xD is signaled.

Similar to the exception processing mode, the stopped state (PST = 0xE) and the halted state (PST = 0xFF) display this status throughout the entire time the ColdFire processor is in the given mode.

26.4.6 Freescale-Recommended BDM Pinout

The ColdFire BDM connector is a 26-pin Berg connector arranged 2 x 13 as shown below.



¹ Pins reserved for BDM developer use.

² Supplied by target

Figure 26-44. Recommended BDM Connector

Chapter 27

IEEE 1149.1 Test Access Port (JTAG)

27.1 Introduction

The Joint Test Action Group (JTAG) is a dedicated user-accessible test logic compliant with the IEEE 1149.1 standard for boundary-scan testability, which helps with system diagnostic and manufacturing testing.

This architecture provides access to all data and chip control pins from the board-edge connector through the standard four-pin test access port (TAP) and the JTAG reset pin, $\overline{\text{TRST}}$.

27.1.1 Block Diagram

Figure 27-1 shows the block diagram of the JTAG module.

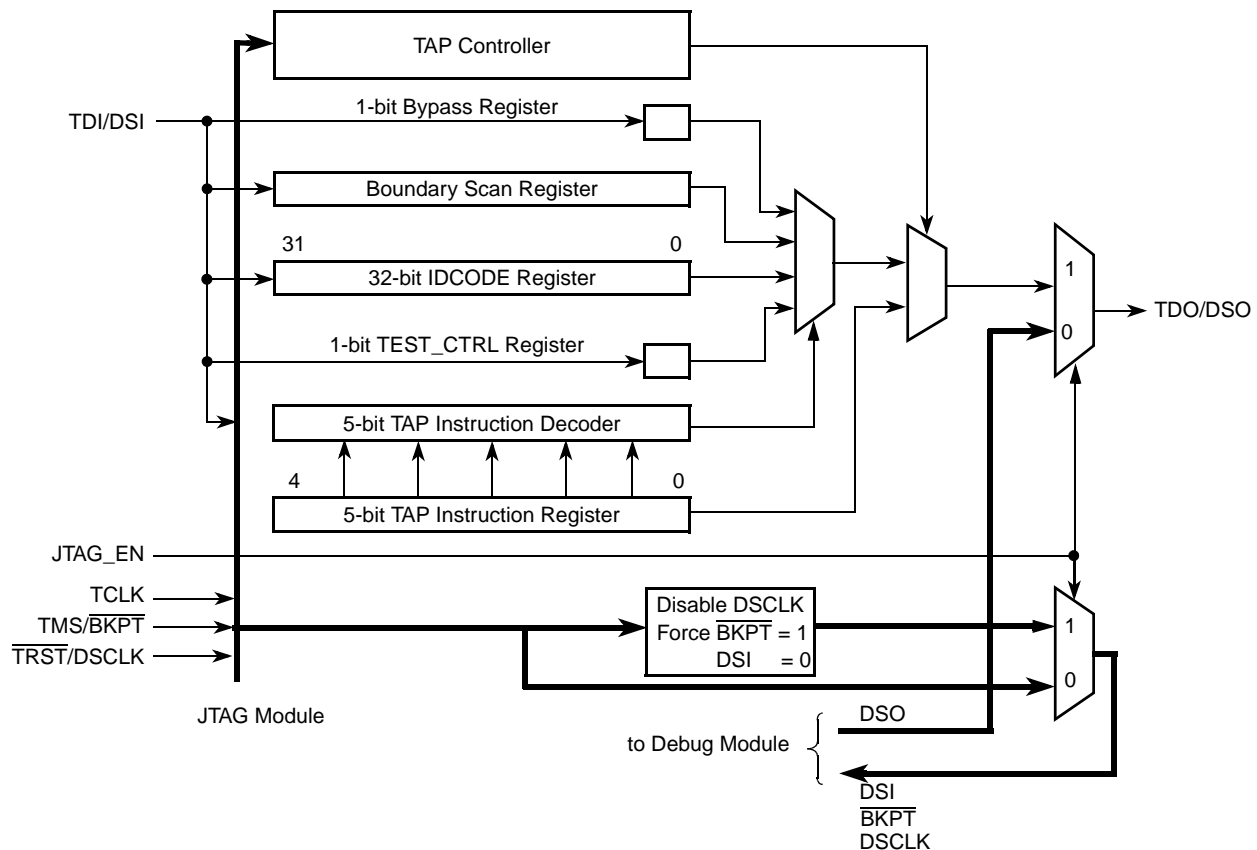


Figure 27-1. JTAG Block Diagram

27.1.2 Features

The basic features of the JTAG module are the following:

- Performs boundary-scan operations to test circuit board electrical continuity
- Bypasses instruction to reduce the shift register path to a single cell
- Sets chip output pins to safety states while executing the bypass instruction
- Samples the system pins during operation and transparently shifts out the result
- Selects between JTAG TAP controller and Background Debug Module (BDM) using a dedicated JTAG_EN pin

27.1.3 Modes of Operation

The JTAG_EN pin can select between the following modes of operation:

- JTAG mode (JTAG_EN = 1)
- Background debug mode (BDM)—for more information, refer to [Section 26.4.1, “Background Debug Mode \(BDM\)”](#); (JTAG_EN = 0).

27.2 External Signal Description

The JTAG module has five input and one output external signals, as described in [Table 27-1](#).

Table 27-1. Signal Properties

Name	Direction	Function	Reset State	Pull up
JTAG_EN	Input	JTAG/BDM selector input	—	—
TCLK	Input	JTAG Test clock input	—	Active
TMS/BKPT	Input	JTAG Test mode select / BDM Breakpoint	—	Active
TDI/DSI	Input	JTAG Test data input / BDM Development serial input	—	Active
TRST/DSCLK	Input	JTAG Test reset input / BDM Development serial clock	—	Active
TDO/DSO	Output	JTAG Test data output / BDM Development serial output	Hi-Z / 0	—

27.2.1 JTAG Enable (JTAG_EN)

The JTAG_EN pin selects between the debug module and JTAG. If JTAG_EN is low, the debug module is selected; if it is high, the JTAG is selected. [Table 27-2](#) summarizes the pin function selected depending on JTAG_EN logic state.

Table 27-2. Pin Function Selected

	JTAG_EN = 0	JTAG_EN = 1	Pin Name
Module selected	BDM	JTAG	—
Pin Function	— $\overline{\text{BKPT}}$ DSI DSO DSCLK	TCLK TMS TDI TDO $\overline{\text{TRST}}$	TCLK $\overline{\text{BKPT}}$ DSI DSO DSCLK

When one module is selected, the inputs into the other module are disabled or forced to a known logic level, as shown in [Table 27-3](#), to disable the corresponding module.

Table 27-3. Signal State to the Disable Module

	JTAG_EN = 0	JTAG_EN = 1
Disabling JTAG	$\overline{\text{TRST}} = 0$ TMS = 1	—
Disabling BDM	—	Disable DSCLK DSI = 0 $\overline{\text{BKPT}} = 1$

NOTE

The JTAG_EN does not support dynamic switching between JTAG and BDM modes.

27.2.2 Test Clock Input (TCLK)

The TCLK pin is a dedicated JTAG clock input to synchronize the test logic. Pulses on TCLK shift data and instructions into the TDI pin on the rising edge and out of the TDO pin on the falling edge. TCLK is independent of the processor clock. The TCLK pin has an internal pull-up resistor, and holding TCLK high or low for an indefinite period does not cause JTAG test logic to lose state information.

27.2.3 Test Mode Select/Breakpoint (TMS/ $\overline{\text{BKPT}}$)

The TMS pin is the test mode select input that sequences the TAP state machine. TMS is sampled on the rising edge of TCLK. The TMS pin has an internal pull-up resistor.

The $\overline{\text{BKPT}}$ pin is used to request an external breakpoint. Assertion of $\overline{\text{BKPT}}$ puts the processor into a halted state after the current instruction completes.

27.2.4 Test Data Input/Development Serial Input (TDI/DSI)

The TDI pin receives serial test and data, which is sampled on the rising edge of TCLK. Register values are shifted in least significant bit (lsb) first. The TDI pin has an internal pull-up resistor.

The DSI pin provides data input for the debug module serial communication port.

27.2.5 Test Reset/Development Serial Clock ($\overline{\text{TRST}}$ /DSCLK)

The $\overline{\text{TRST}}$ pin is an active low asynchronous reset input with an internal pull-up resistor that forces the TAP controller to the test-logic-reset state.

The DSCLK pin clocks the serial communication port to the debug module. Maximum frequency is 1/5 the processor clock speed. At the rising edge of DSCLK, data input on DSI is sampled and DSO changes state.

27.2.6 Test Data Output/Development Serial Output (TDO/DSO)

The TDO pin is the lsb-first data output. Data is clocked out of TDO on the falling edge of TCLK. TDO is tri-stateable and actively driven in the shift-IR and shift-DR controller states.

The DSO pin provides serial output data in BDM mode.

27.3 Memory Map/Register Definition

The JTAG module registers are not memory mapped and are only accessible through the TDO/DSO pin.

27.3.1 Instruction Shift Register (IR)

The JTAG module uses a 5-bit shift register with no parity. The IR transfers its value to a parallel hold register and applies an instruction on the falling edge of TCLK when the TAP state machine is in the update-IR state. To load an instruction into the shift portion of the IR, place the serial data on the TDI pin before each rising edge of TCLK. The msb of the IR is the bit closest to the TDI pin, and the lsb is the bit closest to the TDO pin. See [Section 27.4.3, “JTAG Instructions”](#) for a list of possible instruction codes.

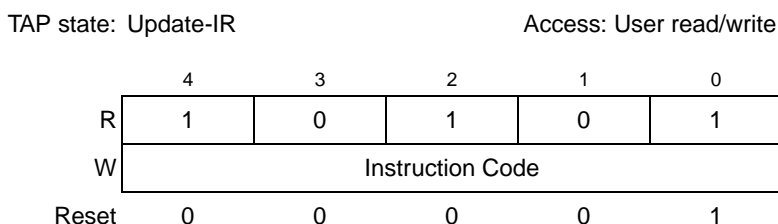


Figure 27-2. 5-Bit Instruction Register (IR)

27.3.2 IDCODE Register

The IDCODE is a read-only register; its value is chip dependent. For more information, see [Section 27.4.3.1, “IDCODE Instruction”](#).

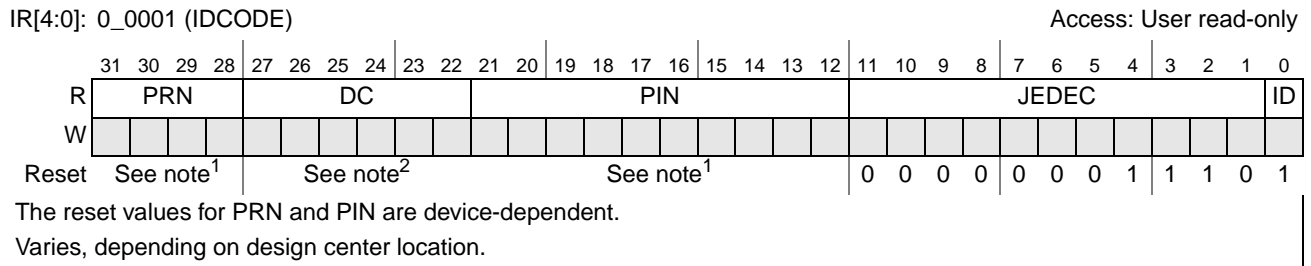


Figure 27-3. IDCODE Register

Table 27-4. IDCODE Field Descriptions

Field	Description
31–28 PRN	Part revision number. Indicate the revision number of the device.
27–22 DC	Freescall design center number.
21–12 PIN	Part identification number. Indicate the device number. 0x044 MCF5208 0x045 MCF5207
11–1 JEDEC	Joint Electron Device Engineering Council ID bits. Indicate the reduced JEDEC ID for Freescall (0x0E).
0 ID	IDCODE register ID. This bit is set to 1 to identify the register as the IDCODE register and not the bypass register according to the IEEE standard 1149.1.

27.3.3 Bypass Register

The bypass register is a single-bit shift register path from TDI to TDO when the BYPASS, CLAMP, or HIGHZ instructions are selected. After entry into the capture-DR state, the single-bit shift register is set to a logic 0. Therefore, the first bit shifted out after selecting the bypass register is always a logic 0.

27.3.4 TEST_CTRL Register

The TEST_CTRL register is a 1-bit shift register path from TDI to TDO when the ENABLE_TEST_CTRL instruction is selected. The TEST_CTRL transfers its value to a parallel hold register on the rising edge of TCLK when the TAP state machine is in the update-DR state. The DSE bit selects the drive strength used in JTAG mode.

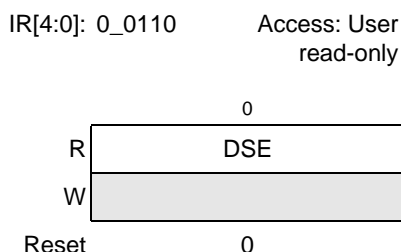


Figure 27-4. 1-Bit TEST_CTRL Register

27.3.5 Boundary Scan Register

The boundary scan register is connected between TDI and TDO when the EXTEST or SAMPLE/PRELOAD instruction is selected. It captures input pin data, forces fixed values on output pins, and selects a logic value and direction for bidirectional pins or high impedance for tri-stated pins.

The boundary scan register contains bits for bonded-out and non bonded-out signals, excluding JTAG signals, analog signals, power supplies, compliance enable pins, device configuration pins, and clock signals.

27.4 Functional Description

27.4.1 JTAG Module

The JTAG module consists of a TAP controller state machine, which is responsible for generating all control signals that execute the JTAG instructions and read/write data registers.

27.4.2 TAP Controller

The TAP controller is a state machine that changes state based on the sequence of logical values on the TMS pin. [Figure 27-5](#) shows the machine's states. The value shown next to each state is the value of the TMS signal sampled on the rising edge of the TCLK signal.

Asserting the $\overline{\text{TRST}}$ signal asynchronously resets the TAP controller to the test-logic-reset state. As [Figure 27-5](#) shows, holding TMS at logic 1 while clocking TCLK through at least five rising edges also causes the state machine to enter the test-logic-reset state, whatever the initial state.

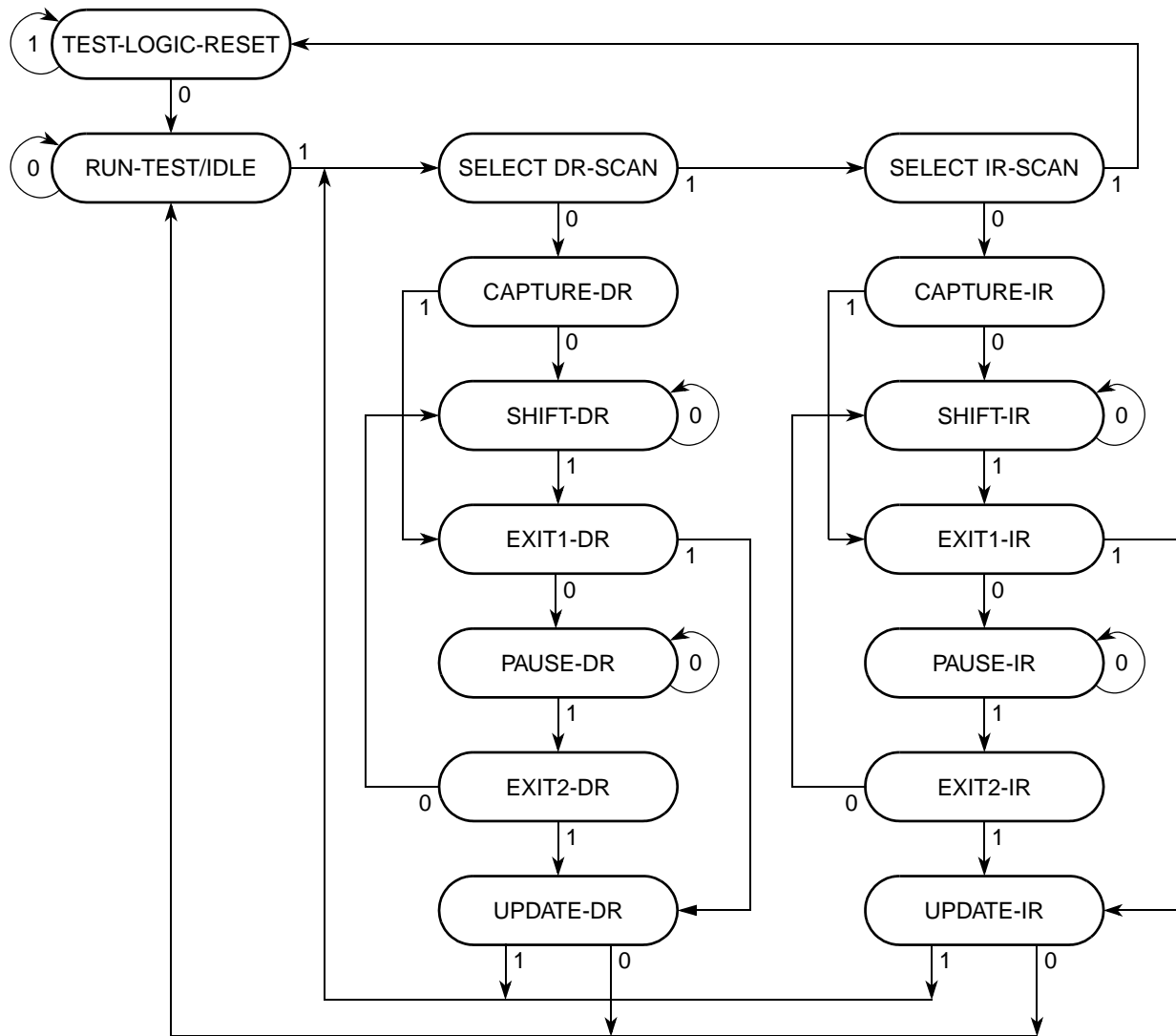


Figure 27-5. TAP Controller State Machine Flow

27.4.3 JTAG Instructions

Table 27-5 describes public and private instructions.

Table 27-5. JTAG Instructions

Instruction	IR[4:0]	Instruction Summary
IDCODE	00001	Selects IDCODE register for shift
SAMPLE/PRELOAD	00010	Selects boundary scan register for shifting, sampling, and preloading without disturbing functional operation
SAMPLE	00011	Selects boundary scan register for shifting and sampling without disturbing functional operation

Table 27-5. JTAG Instructions (continued)

Instruction	IR[4:0]	Instruction Summary
EXTEST	00100	Selects boundary scan register while applying preloaded values to output pins and asserting functional reset
ENABLE_TEST_CTRL	00110	Selects TEST_CTRL register
HIGHZ	01001	Selects bypass register while tri-stating all output pins and asserting functional reset
CLAMP	01100	Selects bypass while applying fixed values to output pins and asserting functional reset
BYPASS	11111	Selects bypass register for data operations
Reserved	all others ¹	Decoded to select bypass register

¹ Freescale reserves the right to change the decoding of the unused opcodes in the future.

27.4.3.1 IDCODE Instruction

The IDCODE instruction selects the 32-bit IDCODE register for connection as a shift path between the TDI and TDO pin. This instruction allows interrogation of the MCU to determine its version number and other part identification data. The shift register lsb is forced to logic 1 on the rising edge of TCLK following entry into the capture-DR state. Therefore, the first bit to be shifted out after selecting the IDCODE register is always a logic 1. The remaining 31 bits are also forced to fixed values on the rising edge of TCLK following entry into the capture-DR state.

IDCODE is the default instruction placed into the instruction register when the TAP resets. Thus, after a TAP reset, the IDCODE register is selected automatically.

27.4.3.2 SAMPLE/PRELOAD Instruction

The SAMPLE/PRELOAD instruction has two functions:

- SAMPLE - See [Section 27.4.3.3, “SAMPLE Instruction,”](#) for description of this function.
- PRELOAD - initialize the boundary scan register update cells before selecting EXTEST or CLAMP. This is achieved by ignoring the data shifting out on the TDO pin and shifting in initialization data. The update-DR state and the falling edge of TCLK can then transfer this data to the update cells. The data is applied to the external output pins by the EXTEST or CLAMP instruction.

27.4.3.3 SAMPLE Instruction

The SAMPLE instruction obtains a sample of the system data and control signals present at the MCU input pins and before the boundary scan cell at the output pins. This sampling occurs on the rising edge of TCLK in the capture-DR state when the IR contains the 0x2 opcode. The sampled data is accessible by shifting it through the boundary scan register to the TDO output by using the shift-DR state. The data capture and the shift operation are transparent to system operation.

NOTE

External synchronization is required to achieve meaningful results because there is no internal synchronization between TCLK and the system clock.

27.4.3.4 EXTEST Instruction

The external test (EXTEST) instruction selects the boundary scan register. It forces all output pins and bidirectional pins configured as outputs to the values preloaded with the SAMPLE/PRELOAD instruction and held in the boundary scan update registers. EXTEST can also configure the direction of bidirectional pins and establish high-impedance states on some pins. EXTEST asserts internal reset for the MCU system logic to force a predictable internal state while performing external boundary scan operations.

27.4.3.5 ENABLE_TEST_CTRL Instruction

The ENABLE_TEST_CTRL instruction selects a 1-bit shift register (TEST_CTRL) for connection as a shift path between the TDI and TDO pin. When the user transitions the TAP controller to the UPDATE_DR state, the register transfers its value to a parallel hold register.

27.4.3.6 HIGHZ Instruction

The HIGHZ instruction eliminates the need to backdrive the output pins during circuit-board testing. HIGHZ turns off all output drivers, including the 2-state drivers, and selects the bypass register. HIGHZ also asserts internal reset for the MCU system logic to force a predictable internal state.

27.4.3.7 CLAMP Instruction

The CLAMP instruction selects the 1-bit bypass register and asserts internal reset while simultaneously forcing all output pins and bidirectional pins configured as outputs to the fixed values that are preloaded and held in the boundary scan update register. CLAMP enhances test efficiency by reducing the overall shift path to a single bit (the bypass register) while conducting an EXTEST type of instruction through the boundary scan register.

27.4.3.8 BYPASS Instruction

The BYPASS instruction selects the bypass register, creating a single-bit shift register path from the TDI pin to the TDO pin. BYPASS enhances test efficiency by reducing the overall shift path when a device other than the ColdFire processor is the device under test on a board design with multiple chips on the overall boundary scan chain. The shift register lsb is forced to logic 0 on the rising edge of TCLK after entry into the capture-DR state. Therefore, the first bit shifted out after selecting the bypass register is always logic 0. This differentiates parts that support an IDCODE register from parts that support only the bypass register.

27.5 Initialization/Application Information

27.5.1 Restrictions

The test logic is a static logic design, and TCLK can be stopped in a high or low state without loss of data. However, the system clock is not synchronized to TCLK internally. Any mixed operation using the test logic and system functional logic requires external synchronization.

Using the EXTEST instruction requires a circuit-board test environment that avoids device-destructive configurations in which MCU output drivers are enabled into actively driven networks.

Low-power stop mode considerations:

- The TAP controller must be in the test-logic-reset state to enter or remain in the low-power stop mode. Leaving the test-logic-reset state negates the ability to achieve low-power, but does not otherwise affect device functionality.
- The TCLK input is not blocked in low-power stop mode. To consume minimal power, the TCLK input should be externally connected to EV_{DD} .
- The TMS, TDI, and \overline{TRST} pins include on-chip pull-up resistors. For minimal power consumption in low-power stop mode, these three pins should be connected to EV_{DD} or left unconnected.

27.5.2 Nonscan Chain Operation

Keeping the TAP controller in the test-logic-reset state ensures that the scan chain test logic is transparent to the system logic. It is recommended that TMS, TDI, TCLK, and \overline{TRST} be pulled up. \overline{TRST} could be connected to ground. However, because there is a pull-up on \overline{TRST} , some amount of current results. The internal power-on reset input initializes the TAP controller to the test-logic-reset state on power-up without asserting \overline{TRST} .

Appendix A

Register Memory Map Quick Reference

A.1 Register Memory Map

Table A-1 illustrates the overall device memory map. Table A-2 lists the base address for each peripheral within the peripheral controller space. Each module is then detailed in Table A-5 through Table A-24. Table A-3 and Table A-4 summarize the ColdFire core and debug registers, which are not accessible through the memory map but are included here for completeness.

Table A-1. Device Memory Map Overview

Address Range	Module	Size
0x0000_0000–0x3FFF_FFFF	FlexBus	1024 MB
0x4000_0000–0x7FFF_FFFF	SDRAM Controller	1024 MB
0x8000_0000–0x8FFF_FFFF	Internal SRAM Backdoor	256 MB
0xC000_0000–0xDFFF_FFFF	FlexBus	512 MB
0xF000_0000–0xFFFF_FFFF ¹	On-chip Peripheral Controller 0	256 MB

¹ See the various tables below or the peripheral chapters for their memory maps. Any unused space by these peripherals within this memory range is reserved and should not be accessed.

NOTE

This memory map provides two disjoint regions mapped to the FlexBus controller to support glueless connections to external memories (e.g., flash and SRAM) as well as a second space with one (or more) unique chip-selects that can be used for non-cacheable, non-memory devices (addresses 0xC000_0000–0xDFFF_FFFF). Additionally, this mapping is selected because it easily maps into the ColdFire access control registers, which provide a coarse association between memory addresses and their attributes (e.g., cacheable, non-cacheable). For this device, one possible configuration defines the default memory attribute as non-cacheable, and one ACR is then used to identify cacheable addresses, e.g., ADDR[31]=0 identifies the cacheable space.

Table A-2. Peripheral Controller 0 Base Addresses

Base Address	Slot Number	Peripheral	Module Memory Map
0xFC00_0000	0	SCM (MPR1, PACRs, & BMT1)	Table A-5
0xFC00_4000	1	Cross-bar switch	Table A-6

Table A-2. Peripheral Controller 0 Base Addresses (continued)

Base Address	Slot Number	Peripheral	Module Memory Map
0xFC00_8000	2	FlexBus	Table A-7
0xFC03_0000	12	FEC	Table A-9
0xFC04_0000	16	SCM (CWT & Core Fault Registers)	Table A-5
0xFC04_4000	17	eDMA Controller	Table A-10
0xFC04_8000	18	Interrupt Controller 0	Table A-11
0xFC05_4000	21	Interrupt Controller IACK	
0xFC05_8000	22	I ² C	Table A-12
0xFC05_C000	23	QSPI	Table A-13
0xFC06_0000	24	UART0	Table A-14
0xFC06_4000	25	UART1	
0xFC06_8000	26	UART2	
0xFC07_0000	28	DMA Timer 0	Table A-15
0xFC07_4000	29	DMA Timer 1	
0xFC07_8000	30	DMA Timer 2	
0xFC07_C000	31	DMA Timer 3	
0xFC08_0000	32	PIT 0	Table A-16
0xFC08_4000	33	PIT 1	
0xFC08_8000	34	Edge Port	Table A-17
0xFC08_C000	35	On-chip Watchdog Timer	Table A-18
0xFC09_0000	36	PLL	Table A-19
0xFC0A_0000	40	CCM, Reset Controller, Power Management	Table A-20 , Table A-21 , Table A-22
0xFC0A_4000	41	GPIO Module	Table A-23
0xFC0A_8000	42	SDRAM Controller	Table A-24

Table A-3. ColdFire Core Programming Model

BDM ¹	Register	Width (bits)	Access	Reset Value	Written with MOVEC	Section/Page
Supervisor/User Access Registers						
Load: 0x080 Store: 0x180	Data Register 0 (D0)	32	R/W	0xCF20_60	No	3.2.1/3-4
Load: 0x081 Store: 0x181	Data Register 1 (D1)	32	R/W	0x1500_1060	No	3.2.1/3-4

Table A-3. ColdFire Core Programming Model (continued)

BDM ¹	Register	Width (bits)	Access	Reset Value	Written with MOVEC	Section/Page
Load: 0x082–7 Store: 0x182–7	Data Register 2–7 (D2–D7)	32	R/W	Undefined	No	3.2.1/3-4
Load: 0x088–8E Store: 0x188–8E	Address Register 0–6 (A0–A6)	32	R/W	Undefined	No	3.2.2/3-4
Load: 0x08F Store: 0x18F	Supervisor/User A7 Stack Pointer (A7)	32	R/W	Undefined	No	3.2.3/3-5
0x804	MAC Status Register (MACSR)	32	R/W	0x0000_0000	No	4.2.1/4-3
0x805	MAC Address Mask Register (MASK)	32	R/W	0xFFFF_FFFF	No	4.2.2/4-5
0x806, 0x809, 0x80A, 0x80B	MAC Accumulators 0–3 (ACC0–3)	32	R/W	Undefined	No	4.2.3/4-6
0x807	MAC Accumulator 0,1 Extension Bytes (ACCext01)	32	R/W	Undefined	No	4.2.4/4-7
0x808	MAC Accumulator 2,3 Extension Bytes (ACCext23)	32	R/W	Undefined	No	4.2.4/4-7
0x80E	Condition Code Register (CCR)	8	R/W	Undefined	No	3.2.4/3-6
0x80F	Program Counter (PC)	32	R/W	Contents of location 0x0000_0004	No	3.2.5/3-7
Supervisor Access Only Registers						
0x002	Cache Control Register (CACR)	32	R/W	0x0000_0000	Yes	3.2.6/3-7
0x004–5	Access Control Register 0–1 (ACR0–1)	32	R/W	See Section	Yes	3.2.7/3-7
0x800	User/Supervisor A7 Stack Pointer (OTHER_A7)	32	R/W	Contents of location 0x0000_0000	No	3.2.3/3-5
0x801	Vector Base Register (VBR)	32	R/W	0x0000_0000	Yes	3.2.8/3-7
0x80E	Status Register (SR)	16	R/W	0x27--	No	3.2.9/3-8
0xC05	RAM Base Address Register (RAMBAR)	32	R/W	See Section	Yes	3.2.10/3-8

¹ The values listed in this column represent the Rc field used when accessing the core registers via the BDM port. For more information see [Chapter 26, “Debug Module”](#).

Table A-4. Debug Module Memory Map

DRc[4–0]	Register Name	Width (bits)	Access	Reset Value	Section/ Page
0x00	Configuration/status register (CSR)	32	R/W See Note	0x0090_0000	26.3.2/26-5
0x05	BDM address attribute register (BAAR)	32 ¹	W	0x05	26.3.3/26-8
0x06	Address attribute trigger register (AATR)	32 ¹	W	0x0005	26.3.4/26-9

Table A-4. Debug Module Memory Map (continued)

DRc[4–0]	Register Name	Width (bits)	Access	Reset Value	Section/ Page
0x07	Trigger definition register (TDR)	32	W	0x0000_0000	26.3.5/26-10
0x08	PC breakpoint register 0 (PBR0)	32	W	Undefined	26.3.6/26-13
0x09	PC breakpoint mask register (PBMR)	32	W	Undefined	26.3.6/26-13
0x0C	Address breakpoint high register (ABHR)	32	W	Undefined	26.3.7/26-15
0x0D	Address breakpoint low register (ABLR)	32	W	Undefined	26.3.7/26-15
0x0E	Data breakpoint register (DBR)	32	W	Undefined	26.3.8/26-16
0x0F	Data breakpoint mask register (DBMR)	32	W	Undefined	26.3.8/26-16
0x18	PC breakpoint register 1 (PBR1)	32	W	See Section	26.3.6/26-13
0x1A	PC breakpoint register 2 (PBR2)	32	W	See Section	26.3.6/26-13
0x1B	PC breakpoint register 3 (PBR3)	32	W	See Section	26.3.6/26-13

¹ Each debug register is accessed as a 32-bit register; reserved fields are not used (don't care).

NOTE

Debug control registers can be written by the external development system or the CPU through the WDEBUG instruction. CSR is write-only from the programming model. It can be read or written through the BDM port using the RDMREG and WDMREG commands.

Table A-5. SCM Memory Map

Address	Register	Width (bits)	Access	Reset Value	Section/Page
0xFC00_0000	Master Privilege Register (MPR)	32	R/W	0x7777_7777	11.2.1/11-2
0xFC00_0020	Peripheral Access Control Register A (PACRA)	32	R/W	0x5444_4444	11.2.2/11-3
0xFC00_0024	Peripheral Access Control Register B (PACRB)	32	R/W	0x4444_4444	11.2.2/11-3
0xFC00_0028	Peripheral Access Control Register C (PACRC)	32	R/W	0x4444_4444	11.2.2/11-3
0xFC00_002C	Peripheral Access Control Register D (PACRD)	32	R/W	0x4444_4444	11.2.2/11-3
0xFC00_0040	Peripheral Access Control Register E (PACRE)	32	R/W	0x4444_4444	11.2.2/11-3
0xFC00_0044	Peripheral Access Control Register F (PACRF)	32	R/W	0x4444_4444	11.2.2/11-3
0xFC00_0054	Bus Monitor Timeout (BMT)	32	R/W	0x0000_0008	11.2.3/11-6
0xFC04_0013	Wakeup Control Register (WCR) ¹	8	R/W	0x00	8.2.1/8-2
0xFC04_0016	Core Watchdog Control Register (CWCR)	16	R/W	0x0000	11.2.4/11-7
0xFC04_001B	Core Watchdog Service Register (CWSR)	8	R/W	Undefined	11.2.5/11-8
0xFC04_001F	SCM Interrupt Status Register (SCMISR)	8	R/W	0x00	11.2.6/11-8
0xFC04_0070	Core Fault Address Register (CFADR)	32	R	0x0000_0000	11.2.7/11-9

Table A-5. SCM Memory Map (continued)

Address	Register	Width (bits)	Access	Reset Value	Section/Page
0xFC04_0075	Core Fault Interrupt Enable Register (CFIER)	8	R/W	0x00	11.2.8/11-10
0xFC04_0076	Core Fault Location Register (CFLOC)	8	R	Undefined	11.2.9/11-10
0xFC04_0077	Core Fault Attributes Register (CFATR)	8	R	Undefined	11.2.10/11-10
0xFC04_007C	Core Fault Data Register (CFDTR)	32	R	Undefined	11.2.11/11-11

¹ The WCR register is described in [Chapter 8, “Power Management.”](#)

Table A-6. XBS Memory Map

Address	Register	Width (bits)	Access	Reset Value	Section/Page
0xFC00_4100	Priority Register Slave 1 (XBS_PRS1)	32	R/W	0x3000_0210	12.4.1/12-3
0xFC00_4110	Control Register Slave 1 (XBS_CRS1)	32	R/W	0x0000_0000	12.4.2/12-4
0xFC00_4400	Priority Register Slave 4 (XBS_PRS4)	32	R/W	0x3000_0210	12.4.1/12-3
0xFC00_4410	Control Register Slave 4 (XBS_CRS4)	32	R/W	0x0000_0000	12.4.2/12-4
0xFC00_4700	Priority Register Slave 7 (XBS_PRS7)	32	R/W	0x3000_0210	12.4.1/12-3
0xFC00_4710	Control Register Slave 7 (XBS_CRS7)	32	R/W	0x0000_0000	12.4.2/12-4

Table A-7. FlexBus Chip Select Memory Map

Address	Register	Width (bits)	Access	Reset Value	Section/ Page
0xFC00_8000 + ($n \times 0xC$)	Chip-Select Address Register (CSAR $_n$) $n = 0 - 5$	32	R/W	0x0000_0000	17.3.1/17-4
0xFC00_8004 + ($n \times 0xC$)	Chip-Select Mask Register (CSMR $_n$) $n = 0 - 5$	32	R/W	0x0000_0000	17.3.2/17-5
0xFC00_8008 + ($n \times 0xC$)	Chip-Select Control Register (CSCR $_n$) $n = 0 - 5$	32	R/W	See Section	17.3.3/17-6

Table A-8. FlexCAN Memory Map

	Register	Width (bits)	Affected by Hard Reset	Affected by Soft Reset	Access	Reset Value	Section/Page
FlexCAN							
Supervisor-only Access Registers							
0x000	FlexCAN Module Configuration Register (CANMCR)	32	Y	Y	R/W	0xD890_000F	23.3.1/23-6
Supervisor/User Access Registers							
0x004	FlexCAN Control Register (CANCTRL)	32	Y	N	R/W	0x0000_0000	23.3.2/23-8

Table A-8. FlexCAN Memory Map (continued)

FlexCAN	Register	Width (bits)	Affected by Hard Reset	Affected by Soft Reset	Access	Reset Value	Section/Page
0x008	Free Running Timer (TIMER)	32	Y	Y	R/W	0x0000_0000	23.3.3/23-10
0x010	Rx Global Mask (RXGMASK)	32	Y	N	R/W	0x1FFF_FFFF	23.3.4/23-11
0x014	Rx Buffer 14 Mask (RX14MASK)	32	Y	N	R/W	0x1FFF_FFFF	23.3.4/23-11
0x018	Rx Buffer 15 Mask (RX15MASK)	32	Y	N	R/W	0x1FFF_FFFF	23.3.4/23-11
0x01C	Error Counter Register (ERRCNT)	32	Y	Y	R/W	0x0000_0000	23.3.5/23-12
0x020	Error and Status Register (ERRSTAT)	32	Y	Y	R/W	0x0000_0000	23.3.6/23-13
0x028	Interrupt Mask Register (IMASK)	32	Y	Y	R/W	0x0000_0000	23.3.7/23-15
0x030	Interrupt Flag Register (IFLAG)	32	Y	Y	R/W	0x0000_0000	23.3.8/23-16
0x080	Message Buffers 0–15 (MB0–15)	2048	N	N	R/W	—	23.3.8/23-16

Table A-9. FEC Register Memory Map

Address	Register	Width (bits)	Access	Reset Value	Section/Page
0xFC03_0004	Interrupt Event Register (EIR)	32	R/W	0x0000_0000	19.4.2/19-9
0xFC03_0008	Interrupt Mask Register (EIMR)	32	R/W	0x0000_0000	19.4.3/19-11
0xFC03_0010	Receive Descriptor Active Register (RDAR)	32	R/W	0x0000_0000	19.4.4/19-11
0xFC03_0014	Transmit Descriptor Active Register (TDAR)	32	R/W	0x0000_0000	19.4.5/19-12
0xFC03_0024	Ethernet Control Register (ECR)	32	R/W	0xF000_0000	19.4.6/19-13
0xFC03_0040	MII Management Frame Register (MMFR)	32	R/W	Undefined	19.4.7/19-13
0xFC03_0044	MII Speed Control Register (MSCR)	32	R/W	0x0000_0000	19.4.8/19-15
0xFC03_0064	MIB Control/Status Register (MIBC)	32	R/W	0x0000_0000	19.4.9/19-16
0xFC03_0084	Receive Control Register (RCR)	32	R/W	0x05EE_0001	19.4.10/19-16
0xFC03_00C4	Transmit Control Register (TCR)	32	R/W	0x0000_0000	19.4.11/19-17
0xFC03_00E4	Physical Address Low Register (PALR)	32	R/W	Undefined	19.4.12/19-18
0xFC03_00E8	Physical Address High Register (PAUR)	32	R/W	See Section	19.4.13/19-19
0xFC03_00EC	Opcode/Pause Duration (OPD)	32	R/W	See Section	19.4.14/19-19
0xFC03_0118	Descriptor Individual Upper Address Register (IAUR)	32	R/W	Undefined	19.4.15/19-20
0xFC03_011C	Descriptor Individual Lower Address Register (IALR)	32	R/W	Undefined	19.4.16/19-20
0xFC03_0120	Descriptor Group Upper Address Register (GAUR)	32	R/W	Undefined	19.4.17/19-21
0xFC03_0124	Descriptor Group Lower Address Register (GALR)	32	R/W	Undefined	19.4.18/19-21
0xFC03_0144	Transmit FIFO Watermark (TFWR)	32	R/W	0x0000_0000	19.4.19/19-21

Table A-9. FEC Register Memory Map (continued)

Address	Register	Width (bits)	Access	Reset Value	Section/Page
0xFC03_014C	FIFO Receive Bound Register (FRBR)	32	R	0x0000_0600	19.4.20/19-22
0xFC03_0150	FIFO Receive FIFO Start Register (FRSR)	32	R	0x0000_0500	19.4.21/19-22
0xFC03_0180	Pointer to Receive Descriptor Ring (ERDSR)	32	R/W	Undefined	19.4.22/19-23
0xFC03_0184	Pointer to Transmit Descriptor Ring (ETDSR)	32	R/W	Undefined	19.4.23/19-23
0xFC03_0188	Maximum Receive Buffer Size (EMRBR)	32	R/W	Undefined	19.4.24/19-24

Table A-10. eDMA Controller Memory Map

Address	Register	Width (bits)	Access	Reset Value	Section/Page
0xFC04_4000	eDMA Control Register (EDMA_CR)	32	R/W	0x0000_0000	16.6.1/16-4
0xFC04_4004	eDMA Error Status Register (EDMA_ES)	32	R	0x0000_0000	16.6.2/16-5
0xFC04_400E	eDMA Enable Request Register (EDMA_ERQ)	16	R/W	0x0000	16.6.3/16-8
0xFC04_4016	eDMA Enable Error Interrupt Register (EDMA_EEI)	16	R/W	0x0000	16.6.4/16-9
0xFC04_4018	eDMA Set Enable Request (EDMA_SERQ)	8	W	0x00	16.6.5/16-9
0xFC04_4019	eDMA Clear Enable Request (EDMA_CERQ)	8	W	0x00	16.6.6/16-10
0xFC04_401A	eDMA Set Enable Error Interrupt Register (EDMA_SEEI)	8	W	0x00	16.6.7/16-11
0xFC04_401B	eDMA Clear Enable Error Interrupt Register (EDMA_CEEI)	8	W	0x00	16.6.8/16-11
0xFC04_401C	eDMA Clear Interrupt Request Register (EDMA_CINT)	8	W	0x00	16.6.9/16-12
0xFC04_401D	eDMA Clear Error Register (EDMA_CERR)	8	W	0x00	16.6.10/16-13
0xFC04_401E	eDMA Set START Bit Register (EDMA_SSRT)	8	W	0x00	16.6.11/16-13
0xFC04_401F	eDMA Clear DONE Status Bit Register (EDMA_CDNE)	8	W	0x00	16.6.12/16-14
0xFC04_4026	eDMA Interrupt Request Register (EDMA_INT)	32	R/W	0x0000	16.6.13/16-15
0xFC04_402E	eDMA Error Register (EDMA_ERR)	32	R/W	0x0000	16.6.14/16-15
0xFC04_4100 + hex(<i>n</i>)	eDMA Channel <i>n</i> Priority Register (DCHPRI <i>n</i>) for <i>n</i> = 0 – 15	8	R/W	See Section	16.6.15/16-16
0xFC04_5000 + hex(32× <i>n</i>)	Transfer Control Descriptor (TCD <i>n</i>) for <i>n</i> = 0 – 15	256	R/W	See Section	16.6.16/16-17

Table A-11. Interrupt Controller Memory Map

Address	Register	Width (bits)	Access	Reset Value	Section/ Page
Interrupt Controller 0					
0xFC04_8000	Interrupt Pending Register High (IPRH)	32	R	0x0000_0000	14.2.1/14-3
0xFC04_8004	Interrupt Pending Register Low (IPRL)	32	R	0x0000_0000	14.2.1/14-3

Table A-11. Interrupt Controller Memory Map (continued)

Address	Register	Width (bits)	Access	Reset Value	Section/Page
0xFC04_8008	Interrupt Mask Register High (IMRH)	32	R/W	0xFFFF_FFFF	14.2.2/14-4
0xFC04_800C	Interrupt Mask Register Low (IMRL)	32	R/W	0xFFFF_FFFF	14.2.2/14-4
0xFC04_8010	Interrupt Force Register High (INTFRCH)	32	R/W	0x0000_0000	14.2.3/14-6
0xFC04_8014	Interrupt Force Register Low (INTFRCL)	32	R/W	0x0000_0000	14.2.3/14-6
0xFC04_801A	Interrupt Configuration Register (ICONFIG)	16	R/W	0x0000	14.2.4/14-6
0xFC04_801C	Set Interrupt Mask (SIMR)	8	W	0x00	14.2.5/14-7
0xFC04_801D	Clear Interrupt Mask (CIMR)	8	W	0x00	14.2.6/14-8
0xFC04_801E	Current Level Mask (CLMASK)	8	R/W	0x0F	14.2.7/14-8
0xFC04_801F	Saved Level Mask (SLMASK)	8	R/W	0x0F	14.2.8/14-9
0xFC04_8040 + n ($n=0:63$)	Interrupt Control Registers (ICR n)	8	R/W	0x00	14.2.9/14-10
0xFC04_80E0	Software Interrupt Acknowledge (SWIACK)	8	R	0x00	14.2.10/14-12
0xFC04_80E0 + $4n$ ($n=1:7$)	Level n Interrupt Acknowledge Registers (L n IACK)	8	R	0x18	14.2.10/14-12

Table A-12. I²C Module Memory Map

Address	Register	Access	Reset Value	Section/Page
0xFC05_8000	I ² C Address Register (I2ADR)	R/W	0x00	25.2.1/25-3
0xFC05_8004	I ² C Frequency Divider Register (I2FDR)	R/W	0x00	25.2.2/25-3
0xFC05_8008	I ² C Control Register (I2CR)	R/W	0x00	25.2.3/25-4
0xFC05_800C	I ² C Status Register (I2SR)	R/W	0x81	25.2.4/25-5
0xFC05_8010	I ² C Data I/O Register (I2DR)	R/W	0x00	25.2.5/25-6

Table A-13. QSPI Memory Map

Address ¹	Register	Width (bits)	Access	Reset Value	Section/Page
0xFC05_C000	QSPI Mode Register (QMR)	16	R/W	0x0104	23.3.1/23-3
0xFC05_C004	QSPI Delay Register (QDLYR)	16	R/W	0x0404	23.3.2/23-5
0xFC05_C008	QSPI Wrap Register (QWR)	16	R/W ²	0x0000	23.3.3/23-6
0xFC05_C00C	QSPI Interrupt Register (QIR)	16	R/W ²	0x0000	23.3.4/23-6
0xFC05_C010	QSPI Address Register (QAR)	16	R/W ²	0x0000	23.3.5/23-7
0xFC05_C014	QSPI Data Register (QDR)	16	R/W	0x0000	23.3.6/23-8

¹ Addresses not assigned to a register and undefined register bits are reserved for expansion.² See the register description for special cases. Some bits may be read- or write-only.

Table A-14. UART Module Memory Map

Address	Register	Width (bit)	Access	Reset Value	Section/Page
UART0 UART1 UART2					
0xFC06_0000 0xFC06_4000 0xFC06_8000	UART Mode Registers ¹ (UMR1 <i>n</i>), (UMR2 <i>n</i>)	8	R/W	0x00	24.3.1/24-5 24.3.2/24-6
0xFC06_0004 0xFC06_4004 0xFC06_8004	UART Status Register (USR <i>n</i>)	8	R	0x00	24.3.3/24-8
	UART Clock Select Register ¹ (UCSR <i>n</i>)	8	W	See Section	24.3.4/24-9
0xFC06_0008 0xFC06_4008 0xFC06_8008	UART Command Registers (UCR <i>n</i>)	8	W	0x00	24.3.5/24-9
0xFC06_000C 0xFC06_400C 0xFC06_800C	UART Receive Buffers (URB <i>n</i>)	8	R	0xFF	24.3.6/24-11
	UART Transmit Buffers (UTB <i>n</i>)	8	W	0x00	24.3.7/24-12
0xFC06_0010 0xFC06_4010 0xFC06_8010	UART Input Port Change Register (UIPCR <i>n</i>)	8	R	See Section	24.3.8/24-12
	UART Auxiliary Control Register (UACR <i>n</i>)	8	W	0x00	24.3.9/24-13
0xFC06_0014 0xFC06_4014 0xFC06_8014	UART Interrupt Status Register (UISR <i>n</i>)	8	R	0x00	24.3.10/24-13
	UART Interrupt Mask Register (UIMR <i>n</i>)	8	W	0x00	24.3.10/24-13
0xFC06_0018 0xFC06_4018 0xFC06_8018	UART Baud Rate Generator Register (UBG1 <i>n</i>)	8	W ²	0x00	24.3.11/24-15
0xFC06_001C 0xFC06_401C 0xFC06_801C	UART Baud Rate Generator Register (UBG2 <i>n</i>)	8	W ²	0x00	24.3.11/24-15
0xFC06_0034 0xFC06_4034 0xFC06_8034	UART Input Port Register (UIP <i>n</i>)	8	R	0xFF	24.3.12/24-15
0xFC06_0038 0xFC06_4038 0xFC06_8038	UART Output Port Bit Set Command Register (UOP1 <i>n</i>)	8	W ²	0x00	24.3.13/24-16
0xFC06_003C 0xFC06_403C 0xFC06_803C	UART Output Port Bit Reset Command Register (UOP0 <i>n</i>)	8	W ²	0x00	24.3.13/24-16

¹ UMR1*n*, UMR2*n*, and UCSR*n* must be changed only after the receiver/transmitter is issued a software reset command. If operation is not disabled, undesirable results may occur.

² Reading this register results in undesired effects and possible incorrect transmission or reception of characters. Register contents may also be changed.

Table A-15. DMA Timer Module Memory Map

Address	Register	Width (bits)	Access	Reset Value	Section/Page
DMA Timer 0 DMA Timer 1 DMA Timer 2 DMA Timer 3					
0xFC07_0000 0xFC07_4000 0xFC07_8000 0xFC07_C000	DMA Timer <i>n</i> Mode Register (DTMR <i>n</i>)	16	R/W	0x0000	22.2.1/22-3
0xFC07_0002 0xFC07_4002 0xFC07_8002 0xFC07_C002	DMA Timer <i>n</i> Extended Mode Register (DTXMR <i>n</i>)	8	R/W	0x00	22.2.2/22-4
0xFC07_0003 0xFC07_4003 0xFC07_8003 0xFC07_C003	DMA Timer <i>n</i> Event Register (DTER <i>n</i>)	8	R/W	0x00	22.2.3/22-5
0xFC07_0004 0xFC07_4004 0xFC07_8004 0xFC07_C004	DMA Timer <i>n</i> Reference Register (DTRR <i>n</i>)	32	R/W	0xFFFF_FFFF	22.2.4/22-6
0xFC07_0008 0xFC07_4008 0xFC07_8008 0xFC07_C008	DMA Timer <i>n</i> Capture Register (DTCR <i>n</i>)	32	R/W	0x0000_0000	22.2.5/22-7
0xFC07_000C 0xFC07_400C 0xFC07_800C 0xFC07_C00C	DMA Timer <i>n</i> Counter Register (DTCN <i>n</i>)	32	R	0x0000_0000	22.2.6/22-8

Table A-16. Programmable Interrupt Timer Modules Memory Map

Address	Register	Width (bits)	Access ¹	Reset Value	Section/Page
PIT 0 PIT 1					
Supervisor Access Only Registers ²					
0xFC08_0000 0xFC08_4000	PIT Control and Status Register (PCSR n)	16	R/W	0x0000	21.2.1/21-3
0xFC08_0002 0xFC08_4002	PIT Modulus Register (PMR n)	16	R/W	0xFFFF	21.2.2/21-4
User/Supervisor Access Registers					
0xFC08_0004 0xFC08_4004	PIT Count Register (PCNTR n)	16	R	0xFFFF	21.2.3/21-5

¹ Accesses to reserved address locations have no effect and result in a cycle termination transfer error.

² User mode accesses to supervisor only addresses have no effect and result in a cycle termination transfer error.

Table A-17. Edge Port Module Memory Map

Address	Register	Width (bits)	Access	Reset Value	Section/Page
Supervisor Access Only Registers¹					
0xFC08_8000	EPORT Pin Assignment Register (EPPAR)	16	R/W	0x0000	15.4.1/15-3
0xFC08_8002	EPORT Data Direction Register (EPDDR)	8	R/W	0x00	15.4.2/15-4
0xFC08_8003	EPORT Interrupt Enable Register (EPIER)	8	R/W	0x00	15.4.3/15-5
Supervisor/User Access Registers					
0xFC08_8004	EPORT Data Register (EPDR)	8	R/W	0xFF	15.4.4/15-5
0xFC08_8005	EPORT Pin Data Register (EPPDR)	8	R	See Section	15.4.5/15-5
0xFC08_8006	EPORT Flag Register (EPFR)	8	R/W	0x00	15.4.6/15-6

¹ User access to supervisor-only address locations have no effect and result in a bus error.

Table A-18. Watchdog Timer Module Memory Map

Address ¹	Register	Width (bits)	Access	Reset Value	Section/Page
Supervisor Only Access					
0xFC08_C000	Watchdog Control Register (WCR)	16	R/W	0x000F	20.2.1/20-3
0xFC08_C002	Watchdog Modulus Register (WMR)	16	R/W	0xFFFF	20.2.2/20-4
Supervisor/User Access					
0xFC08_C004	Watchdog Count Register (WCNTR)	16	R	0xFFFF	20.2.3/20-4
0xFC08_C006	Watchdog Service Register (WSR)	16	R/W	0x0000	20.2.4/20-5

¹ Addresses not assigned to a register and undefined register bits are reserved for expansion. Write accesses to these reserved address spaces and reserved register bits have no effect.

Table A-19. PLL Memory Map

Address	Register	Width (bits)	Access	Reset Value	Section/Page
0xFC09_0000	PLL Output Divider Register (PODR)	8	R/W	0x36 ¹	7.2.1/7-5
0xFC09_0002	PLL Control Register (PCR)	8	R/W	0x00	7.2.2/7-6
0xFC09_0004	PLL Modulation Divider Register (PMDR)	8	R/W	0x00	7.2.3/7-7
0xFC09_0006	PLL Feedback Divider Register (PFDR)	8	R/W	0x42 ¹	7.2.4/7-8

¹ With default reset configuration (RCON is negated).

Table A-20. CCM Memory Map

Address	Register	Width (bits)	Access	Reset Value	Section/Page
Supervisor Access Only Registers¹					
0xFC0A_0004	Chip Configuration Register (CCR)	16	R	See Section	9.3.1/9-3
0xFC0A_0008	Reset Configuration Register (RCON)	16	R	0x0201	9.3.2/9-4
0xFC0A_000A	Chip Identification Register (CIR)	16	R	See Section	9.3.3/9-4

¹ User access to supervisor only address locations have no effect and result in a bus error.

Table A-21. Reset Controller Memory Map

Address	Register	Width (bits)	Access	Reset Value	Section/Page
0xFC0A_0000	Reset Control Register (RCR)	8	R/W	0x00	10.3.1/10-2
0xFC0A_0001	Reset Status Register (RSR)	8	R	See Section	10.3.2/10-3

Table A-22. Power Management Memory Map

Address	Register	Width (bits)	Access	Reset Value	Section/Page
Supervisor Access Only Registers¹					
0xFC04_0013	Wakeup Control Register (WCR)	8	R/W	0x00	8.2.1/8-2
0xFC04_002C	Peripheral Power Management Set Register 0 (PPMSR0)	8	W	0x00	8.2.2/8-3
0xFC04_002D	Peripheral Power Management Clear Register 0 (PPMCR0)	8	W	0x00	8.2.3/8-4
0xFC04_0030	Peripheral Power Management High Register 0 (PPMHR0)	32	R/W	0x0000_0000	8.2.4/8-4
0xFC04_0034	Peripheral Power Management Low Register 0 (PPMLR0)	32	R/W	0x0000_0000	8.2.4/8-4
0xFC0A_0007	Low-Power Control Register (LPCR)	8	R/W	0x00	8.2.5/8-6
0xFC0A_0010	Miscellaneous Control Register (MISCCR)	16	R/W	See Section	8.2.6/8-7

¹ User access to supervisor only address locations have no effect and result in a bus error

Table A-23. GPIO Module Memory Map

Address	Register	Width (bits)	Access	Reset Value	Section/Page
Port Output Data Registers					
0xFC0A_4000	PODR_BUSCTL	8	R/W	0x0F	13.3.1/13-11
0xFC0A_4001	PODR_BE	8	R/W	0x0F	13.3.1/13-11
0xFC0A_4002	PODR_CS	8	R/W	0x0E	13.3.1/13-11
0xFC0A_4003	PODR_FEC12C	8	R/W	0x0F	13.3.1/13-11

Table A-23. GPIO Module Memory Map (continued)

Address	Register	Width (bits)	Access	Reset Value	Section/Page
0xFC0A_4004	PODR_QSPI	8	R/W	0x0F	13.3.1/13-11
0xFC0A_4005	PODR_TIMER	8	R/W	0x0F	13.3.1/13-11
0xFC0A_4006	PODR_UART	8	R/W	0xFF	13.3.1/13-11
0xFC0A_4007	PODR_FECH	8	R/W	0xFF	13.3.1/13-11
0xFC0A_4008	PODR_FECL	8	R/W	0xFF	13.3.1/13-11
Port Data Direction Registers					
0xFC0A_400C	PDDR_BUSCTL	8	R/W	0x00	13.3.2/13-12
0xFC0A_400D	PDDR_BE	8	R/W	0x00	13.3.2/13-12
0xFC0A_400E	PDDR_CS	8	R/W	0x00	13.3.2/13-12
0xFC0A_400F	PDDR_FECI2C	8	R/W	0x00	13.3.2/13-12
0xFC0A_4010	PDDR_QSPI	8	R/W	0x00	13.3.2/13-12
0xFC0A_4011	PDDR_TIMER	8	R/W	0x00	13.3.2/13-12
0xFC0A_4012	PDDR_UART	8	R/W	0x00	13.3.2/13-12
0xFC0A_4013	PDDR_FECH	8	R/W	0x00	13.3.2/13-12
0xFC0A_4014	PDDR_FECL	8	R/W	0x00	13.3.2/13-12
Port Pin Data/Set Data Registers					
0xFC0A_401A	PPDSR_CS	8	R/W	See Section	13.3.3/13-13
0xFC0A_401B	PPDSR_FECI2C	8	R/W	See Section	13.3.3/13-13
0xFC0A_401C	PPDSR_QSPI	8	R/W	See Section	13.3.3/13-13
0xFC0A_401D	PPDSR_TIMER	8	R/W	See Section	13.3.3/13-13
0xFC0A_401E	PPDSR_UART	8	R/W	See Section	13.3.3/13-13
0xFC0A_401F	PPDSR_FECH	8	R/W	See Section	13.3.3/13-13
0xFC0A_4020	PPDSR_FECL	8	R/W	See Section	13.3.3/13-13
Port Clear Output Data Registers					
0xFC0A_4024	PCLRR_BUSCTL	8	W	0x00	13.3.4/13-15
0xFC0A_4025	PCLRR_BE	8	W	0x00	13.3.4/13-15
0xFC0A_4026	PCLRR_CS	8	W	0x00	13.3.4/13-15
0xFC0A_4027	PCLRR_FECI2C	8	W	0x00	13.3.4/13-15
0xFC0A_4028	PCLRR_QSPI	8	W	0x00	13.3.4/13-15
0xFC0A_4029	PCLRR_TIMER	8	W	0x00	13.3.4/13-15
0xFC0A_402A	PCLRR_UART	8	W	0x00	13.3.4/13-15

Table A-23. GPIO Module Memory Map (continued)

Address	Register	Width (bits)	Access	Reset Value	Section/Page
0xFC0A_402B	PCLRR_FECH	8	W	0x00	13.3.4/13-15
0xFC0A_402C	PCLRR_FECL	8	W	0x00	13.3.4/13-15
Pin Assignment Registers					
0xFC0A_4030	PAR_BUSCTL	8	R/W	0x1F	13.3.5.1/13-16
0xFC0A_4031	PAR_BE	8	R/W	0x0F	13.3.5.2/13-16
0xFC0A_4032	PAR_CS	8	R/W	0x0F	13.3.5.3/13-17
0xFC0A_4033	PAR_FECI2C	8	R/W	0x00	13.3.5.4/13-18
0xFC0A_4034	PAR_QSPI	8	R/W	0x00	13.3.5.5/13-18
0xFC0A_4035	PAR_TIMER	8	R/W	0x00	13.3.5.6/13-19
0xFC0A_4036	PAR_UART	8	R/W	0x0000	13.3.5.7/13-20
0xFC0A_4038	PAR_FEC	8	R/W	0x00	13.3.5.8/13-21
0xFC0A_4039	PAR_IRQ	8	R/W	0x00	13.3.5.9/13-23
Mode Select Control Registers					
0xFC0A_403A	MSCR_FLEXBUS	8	R/W	0xFF	13.3.6/13-23
0xFC0A_403B	MSCR_SDRAM	8	R/W	0x3F	13.3.7/13-24
Drive Strength Control Registers					
0xFC0A_403C	DSCR_I2C	8	R/W	See Section	13.3.8.1/13-25
0xFC0A_403D	DSCR_MISC	8	R/W	See Section	13.3.8.2/13-25
0xFC0A_403E	DSCR_FEC	8	R/W	See Section	13.3.8.3/13-26
0xFC0A_403F	DSCR_UART	8	R/W	See Section	13.3.8.4/13-27
0xFC0A_4040	DSCR_QSPI	8	R/W	See Section	13.3.8.5/13-27

Table A-24. SDRAMC Memory Map

Address	Register	Width (bits)	Access	Reset Value	Section/Page
0xFC0A_8000	SDRAM Mode/Extended Mode Register (SDMR)	32	R/W	0x0000_0000	18.4.1/18-14
0xFC0A_8004	SDRAM Control Register (SDCR)	32	R/W	0x0000_0000	18.4.2/18-15
0xFC0A_8008	SDRAM Configuration Register 1 (SDCFG1)	32	R/W	0x0000_0000	18.4.3/18-17
0xFC0A_800C	SDRAM Configuration Register 2 (SDCFG2)	32	R/W	0x0000_0000	18.4.4/18-19
0xFC0A_8110	SDRAM Chip Select 0 Configuration (SDCS0)	32	R/W	0x0000_0000	18.4.5/18-20
0xFC0A_8114	SDRAM Chip Select 1 Configuration (SDCS1)	32	R/W	0x0000_0000	18.4.5/18-20

Appendix B

Revision History

This appendix lists major changes between versions of the MCF5208RM document.

B.1 Changes Between Rev. 1 and Rev. 2

Table B-1. MCF5208RM Rev. 1 to Rev. 2 Changes

Chapter	Description
Overview	In Section 1.3.12/Page 1-9, this device only contains two periodic interrupt timers. Therefore, change heading from “Periodic Interrupt Timers (PIT0–PIT3)” to “Periodic Interrupt Timers (PIT0–PIT1)” and change first sentence from “The four periodic interrupt timers (PIT[3:0]) are 16-bit timers...” to “The two periodic interrupt timers (PIT[1:0]) are 16-bit timers...”
Signal Descriptions	In Table 2-1/Page 2-2, change D[31:0] signal direction from output (O) to input/output (I/O).
Core	In Table 3-1/Page 3-3, change PC's Reset Value entry to “Contents of Location 0x0000_0004” and Written with MOVEC entry to “No”. Change OTHER_A7's Reset Value entry to “Contents of Location 0x0000_0000”.
	In Figure 3-5/Page 3-6, change “Access: User read-only” to “Access: read/write”. Change CCR[4:0] to read/write.
	In Table 3-2/Page 3-6, remove last sentence in C bit field description.
	In Figure 3-8/Page 3-7, change SR[4:0] to read/write.
	In Section 3.4/Page 3-9, change last bullet to “Use of separate system stack pointers for user and supervisor modes”
	In Section 3.4/Page 3-9, change last sentence in step #2 to “The IACK cycle is mapped to special locations within the interrupt controller's address space with the interrupt level encoded in the address.”
	In Section 3.11/Page 3-24, add the following note after the table: <div style="text-align: center;"> NOTE The execution times for moving the contents of the Racc, Raccext[01,23], MACSR, or Rmask into a destination location <ea>x shown in this table represent the best-case scenario when the store instruction is executed and there are no load or M{S}AC instructions in the EMAC execution pipeline. In general, these store operations require only a single cycle for execution, but if preceded immediately by a load, MAC, or MSAC instruction, the depth of the EMAC pipeline is exposed and the execution time is four cycles. </div>
	In the figure D0 Hardware Configuration Info , updated information for bit 10

Table B-1. MCF5208RM Rev. 1 to Rev. 2 Changes (continued)

Chapter	Description
EMAC	In Figure 4-4/Page 4-5 change MACSR[3:0] to R/W.
	In Figure 4-5/Page 4-10 change upper 16 bits of the MASK register to read-only, with a read and reset value of 1.
	In Equation 4-3/Page 4-13, add minus sign to the exponent so that it is “ $-(i + 1 - N)$ ”.
	Changed all ‘mov’ instructions to ‘move’.
Cache	In Table 5-3/Page 5-6, change reset value of ACR0, ACR1 to “See Section” since some of the bits are defined after reset.
	In Figure 5-2/Page 5-6, change CACR fields to R/W, since they may be read via the debug module.
	In Table 5-5/Page 5-8, For split instruction/data cache entry, swap text in parantheses in the description field. Instruction cache uses the upper half of the arrays, while data cache uses the lower half.
	In Section 5.2.2/Page 5-9, change note to: <p style="text-align: center;">NOTE</p> Peripheral space (0xE000_0000-0xFFFF_FFFF) should not be cached. The combination of the CACR defaults and the two ACR n registers must define the non-cacheable attribute for this address space.
	In Figure 5-3/Page 5-9, change ACR fields to R/W, since they may be read via the debug module.
	In Initial Fetch Offset vs. CLNF Bits table: Changed heading from ‘Longword Address Bits’ to ‘Longword Address Bits[3:2]’
SRAM	In Table 6-1/Page 6-2, change RAMBAR reset value entry to “See Section”.
	In Section 6.2.1/Page 6-2, change last bullet to: “A reset clears the RAMBAR’s priority, backdoor write-protect, and valid bits, and sets the backdoor enable bit. This enables the backdoor port and invalidates the processor port to the SRAM. (The RAMBAR must be initialized before the core can access the SRAM.) All other bits are unaffected.”
	In Figure 6-1/Page 6-3, change RAMBAR fields to R/W, since they may be read via the debug module. Reset values of RAMBAR[31:12, 8, 5:1] are unaffected by reset.
PLL	Added “0110 Reserved VCO/6” setting row in PODR[BUSDIV] field description table.
Power Management	In Table 8-8/Page 8-7, add the following note to the LPCR[FWKUP] (fast wake-up) bit description: Note: Setting this bit is potentially dangerous and unreliable. The system may behave unpredictably when using an unlocked clock, since the clock frequency could overshoot the maximum frequency of the device.

Table B-1. MCF5208RM Rev. 1 to Rev. 2 Changes (continued)

Chapter	Description					
CCM	In Figure 9-2/Page 9-3, change read value of CCR[8] to 1 and change default value in note from 0x0201 to 0x012B.					
	In Table 9-3/Page 9-3, change bit 8 description to “Reserved, should be set.”					
	In Figure 9-3/Page 9-4, change RCON reset value from 0x0201 to 0x012B.					
	In Table 9-6/Page 9-6, change the following RCON values in the Default Configuration column: RCON[1]=1, RCON[4:3]=01, RCON[5]=1. Change D7 entry to: <table border="1"> <tr> <th>D7</th><th>PLL Multiplier Select¹</th></tr> <tr> <td>0</td><td>120 (default)</td></tr> <tr> <td>1</td><td>125</td></tr> </table>	D7	PLL Multiplier Select ¹	0	120 (default)	1
D7	PLL Multiplier Select ¹					
0	120 (default)					
1	125					
	¹ Valid only if D1 is set.					
Reset Controller	Clarified Loss of Lock Reset section that this reset only occurs when in PLL mode.					
SCM	Added “The SCMISR[CFEI] bit flags fault errors independent of the CFIER[ECFEI] setting. Therefore, if CFEI is set prior to setting ECFEI, an interrupt is requested immediately after ECFEI is set.” to end of SCMISR section.					
	Added “ Note: This bit reports core faults regardless of the setting of CFIER[ECFEI]. Therefore, if the error interrupt is disabled and a core fault occurs, this bit is set. Then, if the error interrupt is subsequently enabled, an interrupt is immediately requested. To prevent an undesired interrupt, clear the captured error by writing one to CFEI before enabling the interrupt.” to end of SCMISR[CFEI] bit description.					
Crossbar Switch	IN Section 12.1/Page 12-1, complete sentence in second paragraph. From: “The four masters are the ColdFire core, eDMA controller, FEC, and a.” to: “The four masters are the ColdFire core, eDMA controller, FEC, and a reserved master for factory test.”					
	Corrected last part of XBS_CRSn[RO] = 1 bit setting from “(attempted writes have no effect and result in a bus error response).” to “(attempted writes have no effect on the registers and result in a bus error response).”					
	Corrected XBS_CRSn[PARK] bit description from “Park. Determines which master port this slave port parks on when...” to “Park. Determines which master port the current slave port parks on when...”					
GPIO	In Table 13-1/Page 13-4, change D[31:0] signal direction from output (O) to input/output (I/O).					
	In Section 13.3.8/Page 13-25, Change note under each register figure throughout DSCR section from: “... is value of D[21] when RCON = 0.” to “... is value of D[5] when RCON = 0.”					
	Corrected reset values of the PDDR_x registers to 0x00.					
	Corrected stem sentence in PAR_UART section.					
Interrupt Controller	In Section 14.1.1/Page 14-2, delete last sentence of first paragraph: “For many peripheral devices...”					
	Reworded Initialization/Application Info section example steps.					
	Added verb “exists” to notes in CLMASK and SLMASK sections.					
	Marked CLMASK values 0x8 – 0xE as reserved in CLMASK Field Descriptions table.					
	In “Interrupt Control Register (ICRn, (n = 00, 01, 02, ..., 63))” section, added ICR000, ICR100, ICR200 to register addresses and section heading.					

Table B-1. MCF5208RM Rev. 1 to Rev. 2 Changes (continued)

Chapter	Description
Edge Port	Added bit 0 for each EPORT register, although this bit may not be used on this particular device.
DMA Controller	Added second paragraph to Modes of Operation, Normal Mode section.
	Added note to TCDn_CSR[BWC] field description.
	Added external signal timing section.
FlexBus	In figure 17-8 through figure 17-33 add 'ADDR[31:0]' label to first cycle of data signals.
	In Section 17.4.4.1/Page 17-12, change last note on page from: "The processor drives the data lines during the first clock cycle of the transfer. However, this should be ignored by the connected device." to: "The processor drives the data lines during the first clock cycle of the transfer with the full 32-bit address. This may be ignored by standard connected devices using non-multiplexed address and data buses. However, some applications may find this feature beneficial."
	In Figure 17-27/Page 17-24, remove internal termination dashed lines for $\overline{\text{FB_CS}}$, $\overline{\text{FB_BE/BWE}}$, and $\overline{\text{FB_OE}}$ signals.
	In Figure 17-31/Page 17-26, remove internal termination dashed lines for $\overline{\text{FB_CS}}$, $\overline{\text{FB_BE/BWE}}$, and $\overline{\text{FB_OE}}$ signals.
	In Figure 17-33/Page 17-27, remove internal termination dashed lines for $\overline{\text{FB_CS}}$, $\overline{\text{FB_BE/BWE}}$, and $\overline{\text{FB_OE}}$ signals.
	Added Connections for External Memory Port Sizes (CSCRn[SBM] = 1) figure
	In the figure Basic Read-Bus Cycle (No Wait States) , updated the bottom signal.
	Removed reset state column from signals description table, since the signals are most likely shared with other functions.
	Added notes in a few sections regarding the number of chip selects depends on the device and its pin configuration

Table B-1. MCF5208RM Rev. 1 to Rev. 2 Changes (continued)

Chapter	Description
FlexBus (cont'd)	Changed last sentence in first paragraph in memory map/register definition section from "Reading unused or reserved locations terminates normally and returns zeros." to "Do not read unused or reserved locations."
	Corrected second sentence in CSMRn[WP] bit description.
	Reworded first entry in results of address comparison table.
	Rearranged FlexBus operating modes table.
	Clarified first sentence in bus cycle states table, S1 Read entry. Moved second sentence into S2 Read entry.
	Added indeterminate cycle at the end of the read cycle for address bus in all timing diagrams.
	Added notes in basic read and basic write sections regarding this indeterminate cycle.
	Added notes regarding FlexBus signals tristating between bus cycles throughout.
	Added footnote to FlexBus Signal Summary table regarding signal directions changing during SDRAM accesses.
	Changed bit description for CSCRn[RDAH,WRAH] fields
	Updated introduction sentence for figure "Longword-Read Burst from 8-Bit Port 3-1-1-1 (Address Setup and Hold)", added note, added footnote to AH, and added dotted line to $\overline{FB_TA}$ for internal termination.
SDRAM Controller	In Table 18-1/Page 18-5, the SD_DQS table entry add the following note: Note: If a read is attempted from a DDR SDRAM chip select when there is no memory to respond with the appropriate SD_DQS pulses, then the bus cycle will hang. Since there is no high level bus monitor on the device, a reset is the only way to exit this error condition.
	In Figure 18-2/Page 18-11, replace figure with Figure 1 from AN2982 "System Design Using the ColdFire MCF5208 Split Bus Architecture" found at http://www.freescale.com/coldfire since it is more thorough.
	In Figure 18-2/Page 18-12, SD_D[31:0], DQ[31:0], SD_DQS[3:0], and DQS[3:0] should be SD_D[31:16], DQ[31:16], SD_DQS[3:2], and DQS[3:2], respectively, as the device does not support a 32-bit DDR bus. Replace figure with Figure 2 from AN2982 "System Design Using the ColdFire MCF5208 Split Bus Architecture" found at http://www.freescale.com/coldfire since it is more thorough.
	In Section 18.3.5/Page 18-13, remove this entire section, as the device does not support a 32-bit wide DDR bus.
	In Table 18-8/Page 18-17, DQS_OE field should match the corresponding register diagram and be only 2 bits wide at locations 11–10. Change third sentence from "The DSQ_OE[3] bit enables SD_DQS3 and the DSQ_OE[2] bit enables SD_DQS2, and so on." to "The DSQ_OE[1] bit enables SD_DQS3 and the DSQ_OE[0] bit enables SD_DQS2." Consequently, the reserved bit field currently at location 7–3 should be extended to bits 9–3.
	In Table 18-9/Page 18-19, correct equations and examples in SDCFG1[ACT2RW, PRE2ACT, REF2ACT] field descriptions. Change ACT2RW to the following and change PRE2ACT and REF2ACT similarly. "Suggested value = $(t_{RCD} \times f_{SD_CLK}) - 1$ (Round up to nearest integer) Example: If $t_{RCD} = 20\text{ns}$ and $f_{SD_CLK} = 99\text{ MHz}$ Suggested value = $(20\text{ns} \times 99\text{ MHz}) - 1 = 0.98$; round to 1."

Table B-1. MCF5208RM Rev. 1 to Rev. 2 Changes (continued)

Chapter	Description
SDRAM Controller (cont'd)	In Section 18.4.5/Page 18-20, add the following note: NOTE The user should not probe memory on a DDR chip select to determine if memory is connected. If a read is attempted from a DDR SDRAM chip select when there is no memory to respond with the appropriate DQS pulses, then the bus cycle will hang. Since there is no high level bus monitor on the device, a reset is the only way to exit the error condition.
	Added note to SDCFG1[RD_LAT] field: Note: The recommended values are just a starting point and may need to be adjusted depending on the trace length for the data and DQS lines."
	Added Read Clock Recovery (RCR) Block section.
	Updated SD_DQS signal descriptions.
	Added note in memory map section pointing to the slew rate control register in the GPIO module.
	Changed SD_VREF signal description.
	Clarified series termination and SD_CLK termination in DDR layout considerations.
	Clarified DDR SDRAM termination circuit example figure.
	Corrected typos in SDCR[DQS_OE] bit description: from DSQ to DQS.
FEC	In Table 19-2/Page 19-6, correct MIB block counters end address to 0xFC03_02FF.
	In Table 19-3/Page 19-6, correct ECR reset value from 0xF000_0002 to 0xF000_0000.
	In Table 19-3/Page 19-7, correct register name typo in FEC memory map at address 0xFC03_0124. This should be the Descriptor Group Lower Address Register (GALR).
	In Table 19-4/Page 19-8, add RMON_R_DROP to the MIB counter memory map at address 0xFC03_0280 with a description of 'Count of frames not counted correctly.'
	In Figure 19-6/Page 19-13, correct ECR reset value from 0xF000_0002 to 0xF000_0000.
	In Section 19.4.6/Page 19-34, add the following subsection entitled "Duplicate Frame Transmission": The FEC fetches transmit buffer descriptors (TxBDs) and the corresponding transmit data continuously until the transmit FIFO is full. It does not determine whether the TxBD to be fetched is already being processed internally (as a result of a wrap). As the FEC nears the end of the transmission of one frame, it begins to DMA the data for the next frame. In order to remain one BD ahead of the DMA, it also fetches the TxBD for the next frame. It is possible that the FEC will fetch from memory a BD that has already been processed but not yet written back (that is, it is read a second time with the R bit still set). In this case, the data is fetched and transmitted again. Using at least three TxBDs fixes this problem for large frames, but not for small frames. To ensure correct operation for either large or small frames, one of the following must be true: <ul style="list-style-type: none"> • The FEC software driver ensures that there is always at least one TxBD with the ready bit cleared. • Every frame uses more than one TxBD and every TxBD but the last is written back immediately after the data is fetched. • The FEC software driver ensures a minimum frame size, n. The minimum number of TxBDs is then $(\text{Tx FIFO Size} \div (n + 4))$ rounded up to the nearest integer (though the result cannot be less than three). The default Tx FIFO size is 192 bytes; this size is programmable.

Table B-1. MCF5208RM Rev. 1 to Rev. 2 Changes (continued)

Chapter	Description
FEC (cont'd)	Corrected TCR[FEDN] bit to TCR[FDEN] in "Transmit Control Registers (TCRX_CNTRL0 & TCR1)" section
	MII management frame registers section: Reworded sentence from "If the MSCRN register is written to a non-zero value in the case of writing to MMFRn when MSCRN equals 0, an MII frame is generated with the data previously written to the MMFRn." to "If MSCR is cleared while MMFR is written and then MSCR is written with a non-zero value, an MII frame is generated with the data previously written to the MMFR. "
	PAURn register figure, TYPE field change to read-only.
	Removed mention of MII_STATUS register in MII Management Frame Register register description section.
	Max buffer size is 2047, not 2032. Changed throughout.
	Reworded EMRBR[R_BUF_SIZE] description.
	In Transmit Buffer Descriptor Field Definitions table, removed the last sentence from the data length field: "Bits [15:5] are used by the DMA engine; bits[4:0] are ignored." to avoid confusion.
Watchdog Timer	In Figure 20-1/Page 20-2, change 8192 divider to 4096.
	In Section 20.2.3/Page 20-4, change 8192 multiplier in equation 20-1 and text below it to 4096. As a result the maximum timeout frequency changes from 6.44 to 3.22 seconds.
Programmable Interrupt Timers	In Figure 21-3/Page 21-5, remove "IPSBAR Offset" from PCNTRn register diagram.
	Corrected PIT timeout period equation.
DMA Timers	In the table DTMRn Field Descriptions , added the sentence "Avoid setting CLK when RST is set..." to the CLK row description
	In the section Features , updated the maximum timeout period information
	Clarified DTMRn[PS] field description.
	Corrected DTRRn reset value in timer memory map from 0x1111_1111 to 0xFFFF_FFFF.

Table B-1. MCF5208RM Rev. 1 to Rev. 2 Changes (continued)

Chapter	Description															
QSPI	Remove mention of QSPI_CS3 as it is not available on this device.															
	Updated the Introduction section's text															
	In the section External Signal Description , updated the final paragraph															
	In the table QDLYR Field Descriptions , updated the 15 SPE row															
	Updated the table QDR Field Descriptions															
	Updated the second paragraph of the section QSPI RAM															
	Updated the first paragraph of the section Receive RAM															
	Reserved QMR[14] bit (previously DOHIE bit).															
	In Section 23.1.3/Page 23-2, correct baud rate range. Should be 163.39Kbps – 20.83Mbps.															
	In Table 23-8/Page 23-14, correct calculated QSPI_CLK values. They should be as follows:															
	<table border="1"> <thead> <tr> <th colspan="2">Internal Bus Clock = 83.33 MHz</th></tr> <tr> <th>QMR [BAUD]</th><th>QSPI_CLK</th></tr> </thead> <tbody> <tr> <td>2</td><td>20.83 MHz</td></tr> <tr> <td>4</td><td>10.425 MHz</td></tr> <tr> <td>8</td><td>5.208 MHz</td></tr> <tr> <td>16</td><td>2.604 MHz</td></tr> <tr> <td>32</td><td>1.302MHz</td></tr> <tr> <td>255</td><td>163.39 kHz</td></tr> </tbody> </table>	Internal Bus Clock = 83.33 MHz		QMR [BAUD]	QSPI_CLK	2	20.83 MHz	4	10.425 MHz	8	5.208 MHz	16	2.604 MHz	32	1.302MHz	255
Internal Bus Clock = 83.33 MHz																
QMR [BAUD]	QSPI_CLK															
2	20.83 MHz															
4	10.425 MHz															
8	5.208 MHz															
16	2.604 MHz															
32	1.302MHz															
255	163.39 kHz															
UART	In Section 24.2 / Page 24-3, changed "An internal interrupt request signal notifies the interrupt controller..." to "A request signal is provided to notify the interrupt controller..."															
	In Table 24-6 / Page 24-9, changed "DTIN" to "DTnIN" (to maintain consistent signal names throughout chapter).															
	In Section 24.4.5.2 / Page 24-26, changed "...complete normally without exception processing..." to "...complete normally without an error termination..."															
	Corrected note in UIPn[CTS] bit description from "...and value as UIPCRn[RTS]." to "...and value as UIPCRn[CTS]."															
	Reworded note below UART block diagram.															
	In Receiver Timing Diagram figure, replaced UnTXD with UnRXD and TXRTS with RXRTS															
	In Remote Loopback figure, changed UnTXD label to output															
	In Multidrop Mode Timing Diagram figure, master station: changed UMR1n[PT]=2 to UMR1n[PT]=1, peripheral station: deleted extraneous second instance of UMR1n[PM]=11															
	In UART Clock Select Registers figure, added note to UCSR[TCS,RCS] reset value															
I ² C	Rearranged and renamed sections to be consistent with rest of the reference manual.															
	Changed application code examples to pseudocode.															

Table B-1. MCF5208RM Rev. 1 to Rev. 2 Changes (continued)

Chapter	Description
Debug Controller	In Table 26-3/Page 26-7, change reset value of PBR1–3 to “See Section” since the lsb of these registers is cleared at reset.
	In Table 26-7/Page 26-12, change AATR[TT] bit setting 11 to Reserved and remove TT=11 column from AATR[TM] bit description.
	In Table 26-9/Page 26-16, add the following note to the PBR0[Address] field description: Note: PBR0[0] should always be loaded with a 0.
	In Figure 26-9/Page 26-16, change address of PBR3 to 0x1B.
	In Table 26-22/Page 26-38, change CSR's initial state to 0x0090_0000.
	In Section 26.6.2/Page 26-42, add the following note to the end of this section: NOTE The debug module requires the use of the internal bus to perform BDM commands. For this processor core, if the processor is executing a tight loop that is contained within a single aligned longword, the processor may never grant the internal bus to the debug module, for example: <pre> align4 label1: nop bra.b label1 or align4 label2: bra.w label2 </pre> The processor grants the internal bus if these loops are forced across two longwords.
	Clarified last sentence of first paragraph in memory map section regarding quiescent DSCLK during WDEBUG.
	Added note to CSR[PCD] bit description.
JTAG	In Figure 27-3/ Page 27-4, updated the IDCOD register figure to indicate that the reset values for both PRN and PIN are device-dependent.

B.2 Changes Between Rev. 0 and Rev. 0.1

Table B-2. MCF5208RM Rev. 0 to Rev. 0.1 Changes

Location	Description
Section 1.3.16/Page 1-10	The DRAMSEL bit settings should be swapped. DRAMSEL = 0 for DDR mode, and DRAMSEL = 1 for SDR mode.
Table 2-1/Page 2-2	Add “Voltage Domain” column indicated the domain for each signal. The FlexBus and SDRAM signals are SD_VDD, while all the rest are EVDD.
Table 2-1/Page 2-2	Add the following footnote to the SD_BA[1:0], SD_A[13:11], SD_A[9:0], and SD_DQM[3:0] signals: The SDRAM functions of these signals are not programmable by the user. They are dynamically switched by the processor when accessing SDRAM memory space and are included here for completeness.
Table 2-1/Page 2-2	BE/BWE[3:0] for 144 LQFP should be “20, 48, 18, 50” instead of “18, 20, 48, 50”

Table B-2. MCF5208RM Rev. 0 to Rev. 0.1 Changes (continued)

Location	Description																																																															
Table 2-1/Page 2-5	Pin 33 for 144 LQFP package should be EVDD instead of SD_VDD.																																																															
Table 2-1/Page 2-5	<p>Add UART0/1 control signals as alternate 2 functions to the FEC pins. Also, add the pin assignments for the MCF5207 devices. The MCF5207 does not contain an FEC module. However, the FEC port in the GPIO module is used to control the UART0/1 control signals.</p> <table><tr><th>Primary</th><th>GPIO</th><th>Alternate 2</th><th>MCF5207 144 LQFP</th><th>MCF5207 144 MAPBGA</th><th>MCF5208 160 QFP</th><th>MCF5208 196 MAPBGA</th></tr><tr><td>—</td><td>PFECH6</td><td>$\overline{U1RTS}$</td><td>142</td><td>A2</td><td>—</td><td>—</td></tr><tr><td>FEC_TXEN</td><td>PFECH6</td><td>$\overline{U1RTS}$</td><td>—</td><td>—</td><td>158</td><td>A2</td></tr><tr><td>—</td><td>PFECL4</td><td>$\overline{U0RTS}$</td><td>141</td><td>D5</td><td>—</td><td>—</td></tr><tr><td>FEC_TXER</td><td>PFECL4</td><td>$\overline{U0RTS}$</td><td>—</td><td>—</td><td>156</td><td>A3</td></tr><tr><td>—</td><td>PFECL1</td><td>$\overline{U1CTS}$</td><td>139</td><td>B4</td><td>—</td><td>—</td></tr><tr><td>FEC_RXD1</td><td>PFECL1</td><td>$\overline{U1CTS}$</td><td>—</td><td>—</td><td>151</td><td>C5</td></tr><tr><td>—</td><td>PFECL0</td><td>$\overline{U0CTS}$</td><td>140</td><td>E4</td><td>—</td><td>—</td></tr><tr><td>FEC_RXER</td><td>PFECL0</td><td>$\overline{U0CTS}$</td><td>—</td><td>—</td><td>155</td><td>C4</td></tr></table>	Primary	GPIO	Alternate 2	MCF5207 144 LQFP	MCF5207 144 MAPBGA	MCF5208 160 QFP	MCF5208 196 MAPBGA	—	PFECH6	$\overline{U1RTS}$	142	A2	—	—	FEC_TXEN	PFECH6	$\overline{U1RTS}$	—	—	158	A2	—	PFECL4	$\overline{U0RTS}$	141	D5	—	—	FEC_TXER	PFECL4	$\overline{U0RTS}$	—	—	156	A3	—	PFECL1	$\overline{U1CTS}$	139	B4	—	—	FEC_RXD1	PFECL1	$\overline{U1CTS}$	—	—	151	C5	—	PFECL0	$\overline{U0CTS}$	140	E4	—	—	FEC_RXER	PFECL0	$\overline{U0CTS}$	—	—	155	C4
Primary	GPIO	Alternate 2	MCF5207 144 LQFP	MCF5207 144 MAPBGA	MCF5208 160 QFP	MCF5208 196 MAPBGA																																																										
—	PFECH6	$\overline{U1RTS}$	142	A2	—	—																																																										
FEC_TXEN	PFECH6	$\overline{U1RTS}$	—	—	158	A2																																																										
—	PFECL4	$\overline{U0RTS}$	141	D5	—	—																																																										
FEC_TXER	PFECL4	$\overline{U0RTS}$	—	—	156	A3																																																										
—	PFECL1	$\overline{U1CTS}$	139	B4	—	—																																																										
FEC_RXD1	PFECL1	$\overline{U1CTS}$	—	—	151	C5																																																										
—	PFECL0	$\overline{U0CTS}$	140	E4	—	—																																																										
FEC_RXER	PFECL0	$\overline{U0CTS}$	—	—	155	C4																																																										
Table 2-1/Page 2-6	Remove the UART0 and UART1 primary function control signals for the MCF5207. To use these functions on the MCF5207 devices, see the above errata that adds the UART control functions to the FEC pins. The MCF5207 devices do not contain an FEC module; however, the various GPIO FEC registers are used to control these signals.																																																															
Table 2-6/Page 2-10	Correct description of the $\overline{BE/BWEn}$ signals: Remove “SRAM and” from second sentence of first paragraph, Remove SDRAM paragraph and add reference to Table 2-7.																																																															
Table 2-7/Page 2-11	<p>Add the following to the SD_DQM[3:0] entry description:</p> <p>“These pins are multiplexed with the $\overline{BE/BWEn}$ pins.</p> <p>The SD_DQMn should be connected to individual SDRAM DQM signals. Note that most SDRAMs associate DQM3 with the MSB, in which case SD_DQM3 should be connected to the SDRAM's DQM3 input.”</p>																																																															
Table 6-1/Page 6-2	Remove ‘1’ from RAMBAR register name and mnemonic.																																																															
Section 6.2.1/Page 6-2	<p>Add the following two notes:</p> <p>Note: By default the RAMBAR is invalid, but the back door is enabled. In this state, any core accesses to the SRAM will be routed through the backdoor. Therefore the SRAM is accessible by the core, but it will not have a single-cycle access time. In order to insure that the core will have single-cycle access to the SRAM, the RAMBAR[V] bit should be set.</p> <p>Note: Any access within the memory range allocated for the on-chip SRAM (0x8000_0000-0x8FFF_FFFF) will "hit" in the SRAM even if the address is beyond the defined size for the SRAM. This creates a ghosting effect for the on-chip SRAM memory. For example, writes to addresses 0x8000_0000 and 0x8000_84000 will actually modify the exact same memory location. System software should ensure that SRAM address pointers do not exceed the size of the SRAM in order to prevent unwanted overwriting of SRAM.</p>																																																															
Figure 6-1/Page 6-2	Change the reset value for the RAMBAR[BDE] bit from 0 to 1.																																																															
Chapter 9	Remove instances of D8 being used for reset configuration within chapter.																																																															

Table B-2. MCF5208RM Rev. 0 to Rev. 0.1 Changes (continued)

Location	Description
Section 9.1.3/Page 9-2	Remove last sentence regarding using the $\overline{BE}/\overline{BWE}$ signals as GPIO. The byte lane assignments were incorrect and also, the byte lanes change when using split bus mode.
Section 9.2.2/Page 9-2	Add the following note to the end of the section: “It is recommended that the logic levels for reset configuration on D[9,7:1] be actively driven when RCON is used. The rest of the data bus should either be allowed to float or be pulled high.”
Table 9-2/Page 9-2	Change reset value of RCON entry to 0x0201.
Figure 9-2/Page 9-3	Change last sentence in note to read “Default reset value (\overline{RCON} is not asserted) is 0x0201.” instead of “Default reset value (\overline{RCON} is not asserted) is 0x0001.”
Table 9-6/Page 9-6	Change default configuration entry for “Chip Select Configuration” row from “RCON9 = 0” to “RCON9 = 1”.
Table 11-1/Page 11-2	Change Master Privilege Register entry’s mnemonic from “MPR1” to “MPR”.
Table 11-1/Page 11-2	Change CFDTR register address from 0xFC04_0078 to 0xFC04_007C.
Section 11.2.3/Page 11-6	Change next to last sentence in second paragraph from “...an interrupt to the interrupt controller is generated if the CFLOC[ECFEI] bit is set.” to “...an interrupt to the interrupt controller is generated if the CFIER[ECFEI] bit is set.”
Figure 11-18/Page 11-11	Change CFDTR register address from 0xFC04_0078 to 0xFC04_007C.
Chapter 12	Add a reserved master used only for factory test purposes at location M7. The XBS_PRSn[M7] field must comply with the restriction that its value must be unique to the other Mn fields.

Table B-2. MCF5208RM Rev. 0 to Rev. 0.1 Changes (continued)

Location	Description																																	
Table 12-1/Page 12-2	<p>For the slave modules add a column for each slave's address range, as well as two footnotes as shown below:</p> <p style="text-align: center;">Table 12-1. Cross-bar Switch Master/Slave Assignments</p> <table><tr><th colspan="3">Master Modules</th></tr><tr><th>Cross-bar Port</th><th colspan="2">Module</th></tr><tr><td>Master 0 (M0)</td><td colspan="2">ColdFire Core</td></tr><tr><td>Master 1 (M1)</td><td colspan="2">eDMA Controller</td></tr><tr><td>Master 2 (M2)</td><td colspan="2">Fast Ethernet Controller</td></tr><tr><td>Master 7 (M7)</td><td colspan="2">Reserved for Factory Test</td></tr><tr><th colspan="3">Slave Modules</th></tr><tr><th>Cross-bar Port</th><th>Module</th><th>Address Range¹</th></tr><tr><td>Slave 1 (S1)</td><td>Flexbus SDRAM Controller</td><td>0x0000_0000–0x3FFF_FFFF & 0xC000_0000–0xDFFF_FFFF 0x4000_0000–0x7FFF_FFFF</td></tr><tr><td>Slave 4 (S4)</td><td>Internal SRAM Backdoor</td><td>0x8000_0000–0x8FFF_FFFF</td></tr><tr><td>Slave 7 (S7)</td><td>Other On-chip Peripherals</td><td>0xF000_0000–0xFFFF_FFFF²</td></tr></table> <p>¹ Unused address spaces are reserved.</p> <p>² See the various peripheral chapters for their memory maps. Any unused space by these peripherals within this memory range is reserved and should not be accessed.</p>	Master Modules			Cross-bar Port	Module		Master 0 (M0)	ColdFire Core		Master 1 (M1)	eDMA Controller		Master 2 (M2)	Fast Ethernet Controller		Master 7 (M7)	Reserved for Factory Test		Slave Modules			Cross-bar Port	Module	Address Range ¹	Slave 1 (S1)	Flexbus SDRAM Controller	0x0000_0000–0x3FFF_FFFF & 0xC000_0000–0xDFFF_FFFF 0x4000_0000–0x7FFF_FFFF	Slave 4 (S4)	Internal SRAM Backdoor	0x8000_0000–0x8FFF_FFFF	Slave 7 (S7)	Other On-chip Peripherals	0xF000_0000–0xFFFF_FFFF ²
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Slave 7 (S7)	Other On-chip Peripherals	0xF000_0000–0xFFFF_FFFF ²																																
Section 12.1/Page 12-2	<p>Add the following note below the above added table.</p> <p style="text-align: center;">NOTE</p> <p>This memory map provides two disjoint regions mapped to the FlexBus controller to support glueless connections to external memories (e.g., flash and SRAM) as well as a second space with one (or more) unique chip-selects that can be used for non-cacheable, non-memory devices (addresses 0xC000_0000–0xDFFF_FFFF). Additionally, this mapping is selected since it easily maps into the ColdFire access control registers, which provide a coarse association between memory addresses and their attributes (e.g., cacheable, non-cacheable). For this device, one possible configuration defines the default memory attribute as non-chacheable, and one ACR is then used to identify cacheable addresses, e.g., ADDR[31]=0 identifies the cacheable space.</p>																																	
Section 12.4.1/Page 12-4	<p>The possible values for the XBS_PRSn fields depend on the number of masters available on the device. Since the device contains four masters (including reserved masters) then valid values are '000' to '011'. Unpredictable results will occur when using the reserved settings of '100' to '111'. Update reset values accordingly to 0x3000_0210.</p>																																	
Table 13-1/Page 13-2	<p>Add "Voltage Domain" column indicated the domain for each signal. The FlexBus and SDRAM signals are SD_VDD, while all the rest are EVDD.</p>																																	

Table B-2. MCF5208RM Rev. 0 to Rev. 0.1 Changes (continued)

Location	Description																																																															
Table 13-1/Page 13-2	Add the following footnote to the SD_BA[1:0], SD_A[13:11], SD_A[9:0], and SD_DQM[3:0] signals: The SDRAM functions of these signals are not programmable by the user. They are dynamically switched by the processor when accessing SDRAM memory space and are included here for completeness.																																																															
Table 13-1/Page 13-5	<div>Add UART0/1 control signals as alternate 2 functions to the FEC pins. Also, add the pin assignments for the MCF5207 devices. The MCF5207 does not contain an FEC module. However, the FEC port in the GPIO module is used to control the UART0/1 control signals.</div> <table><thead><tr><th>Primary</th><th>GPIO</th><th>Alternate 2</th><th>MCF5207 144 LQFP</th><th>MCF5207 144 MAPBGA</th><th>MCF5208 160 QFP</th><th>MCF5208 196 MAPBGA</th></tr></thead><tbody><tr><td>—</td><td>PFECH6</td><td>U1RTS</td><td>142</td><td>A2</td><td>—</td><td>—</td></tr><tr><td>FEC_TXEN</td><td>PFECH6</td><td>U1RTS</td><td>—</td><td>—</td><td>158</td><td>A2</td></tr><tr><td>—</td><td>PFECL4</td><td>U0RTS</td><td>141</td><td>D5</td><td>—</td><td>—</td></tr><tr><td>FEC_TXER</td><td>PFECL4</td><td>U0RTS</td><td>—</td><td>—</td><td>156</td><td>A3</td></tr><tr><td>—</td><td>PFECL1</td><td>U1CTS</td><td>139</td><td>B4</td><td>—</td><td>—</td></tr><tr><td>FEC_RXD1</td><td>PFECL1</td><td>U1CTS</td><td>—</td><td>—</td><td>151</td><td>C5</td></tr><tr><td>—</td><td>PFECL0</td><td>U0CTS</td><td>140</td><td>E4</td><td>—</td><td>—</td></tr><tr><td>FEC_RXER</td><td>PFECL0</td><td>U0CTS</td><td>—</td><td>—</td><td>155</td><td>C4</td></tr></tbody></table>	Primary	GPIO	Alternate 2	MCF5207 144 LQFP	MCF5207 144 MAPBGA	MCF5208 160 QFP	MCF5208 196 MAPBGA	—	PFECH6	U1RTS	142	A2	—	—	FEC_TXEN	PFECH6	U1RTS	—	—	158	A2	—	PFECL4	U0RTS	141	D5	—	—	FEC_TXER	PFECL4	U0RTS	—	—	156	A3	—	PFECL1	U1CTS	139	B4	—	—	FEC_RXD1	PFECL1	U1CTS	—	—	151	C5	—	PFECL0	U0CTS	140	E4	—	—	FEC_RXER	PFECL0	U0CTS	—	—	155	C4
Primary	GPIO	Alternate 2	MCF5207 144 LQFP	MCF5207 144 MAPBGA	MCF5208 160 QFP	MCF5208 196 MAPBGA																																																										
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Table 13-1/Page 13-6	Remove the UART0 and UART1 primary function control signals for the MCF5207. To use these functions on the MCF5207 devices, see the above errata that adds the UART control functions to the FEC pins. The MCF5207 devices do not contain an FEC module; however, the various GPIO FEC registers are used to control these signals.																																																															
Table 14-15/Page 14-11	Correct source #25, “Flag clearing mechanism” entry from “Write CWIR[CWIC]=1” to “Write SCMISR[CWIC]=1”.																																																															
Figure 15-3/Page 15-4	<div>Change register diagram from 16-bit to 8-bit as shown below:</div> <div>Address: 0xFC08_8002 (EPDDR)Access: Supervisor read/write</div> <table><tr><td></td><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr><tr><td>R</td><td>EPDD7</td><td>EPDD6</td><td>EPDD5</td><td>EPDD4</td><td>EPDD3</td><td>EPDD2</td><td>EPDD1</td><td>0</td></tr><tr><td>W</td><td></td><td></td><td></td><td></td><td></td><td></td><td></td><td></td></tr><tr><td>Reset</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td></tr></table> <div>Figure 15-3. EPORT Data Direction Register (EPDDR)</div>		7	6	5	4	3	2	1	0	R	EPDD7	EPDD6	EPDD5	EPDD4	EPDD3	EPDD2	EPDD1	0	W									Reset	0	0	0	0	0	0	0	0																											
	7	6	5	4	3	2	1	0																																																								
R	EPDD7	EPDD6	EPDD5	EPDD4	EPDD3	EPDD2	EPDD1	0																																																								
W																																																																
Reset	0	0	0	0	0	0	0	0																																																								
Section 17.3.1.1/Page 17-4	Change next to last sentence in section to “For example, a 16-bit address/16-bit data device would connect its addr[15:0] to A[16:1] and data[15:0] to D[31:16].”																																																															
Table 17-2/Page 17-4	Delete table; it is a duplicate of the one in the CCM chapter.																																																															
Figure 17-3/Page 17-7	Correct CSCRn reset value; bits AA and BEM are set at reset.																																																															

Table B-2. MCF5208RM Rev. 0 to Rev. 0.1 Changes (continued)

Location	Description
Table 17-6/Page 17-8	Clarify CSCRn[PS] = 01, 1x bit settings for when split bus mode is used: 01 8-bit port size. Valid data sampled and driven on D[31:24] if SBM=0 or D[7:0] if SBM = 1. 1x 16-bit port size. Valid data sampled and driven on D[31:16] if SBM=0 or D[15:0] if SBM = 1.
Section 17.4.2/Page 17-9	<p>Correct section for split bus mode, as the byte lanes vary depending on the setting.</p> <p>1) Add the following sentence after the first sentence in the first paragraph: “The byte lane assignment is also dependent on the split bus mode setting in the CSCRn register.”</p> <p>2) Change the third sentence to: “Figure 17-4 shows the byte lanes that external memory should be connected to and the sequential transfers if a longword is transferred for three port sizes when not in split bus mode.”</p> <p>3) Add byte lane mapping figure for when split bus mode is enabled and the text introducing it: “When split bus mode is enabled (CSCRn[SBM] = 1) the lane assignments are slightly different, as shown in the below figure.”</p> <div style="text-align: center;"> <pre> graph TD subgraph Bus [Processor External Data Bus] D15_8[D[15:8]] D7_0[D[7:0]] end subgraph Port16 [16-Bit Port Memory] B0[Byte 0] B1[Byte 1] B2[Byte 2] B3[Byte 3] end subgraph Port8 [8-Bit Port Memory] B0_8[Byte 0] B1_8[Byte 1] B2_8[Byte 2] B3_8[Byte 3] end D15_8 --> B0 D15_8 --> B2 D7_0 --> B1 D7_0 --> B3 D7_0 --> B0_8 D7_0 --> B1_8 D7_0 --> B2_8 D7_0 --> B3_8 </pre> <p>Figure 17-5. Connections for External Memory Port Sizes (CSCRn[SBM] = 1)</p> </div>
Throughout Chapter 17	In all timing diagrams within the FlexBus chapter, the address and data signals stop driving the bus one clock cycle sooner than shown. Because of this, in the diagrams illustrating address hold, the address hold state is swapped with the S3 state.
Figure 17-27/Page 17-23	Insert a single clock cycle for address setup at the beginning of each data transfer, between S0 and S1 states.
Figure 17-28/Page 17-24	Insert a single clock cycle for address setup at the beginning of each data transfer, between S0 and S1 states.
Section 18.5.2/Page 18-23	Remove “Perform a single read/write to any of the SDRAM chip select address spaces to issue the command.” sentence from steps 5 and 9 of Section 18.6, “Initialization/Application Information.” This is not recommended or necessary.
Table 19-2/Page 19-5	Change reset value of ECR register from 0x0000_0000 to 0xF000_0002.
Section 19.2.3/Page 19-6	Change second sentence in first paragraph from “These fall in the 0xFC03_0200-0xFC03_03FF address offset range.” to “These fall in the 0xFC03_0200-0xFC03_02FF address range.”
Figure 19-6/Page 19-12	Change reset value of ECR register from 0x0000_0000 to 0xF000_0002.
Figure 19-24/Page 19-23	Correct EMRBR register address from 0xFC03_01B8 to 0xFC03_0188

Table B-2. MCF5208RM Rev. 0 to Rev. 0.1 Changes (continued)

Location	Description
Section 24.4.1.1/Page 24-17	Change first bullet from “An external clock signal on the DTnIN pin. When divided by the 16-bit divider, DTnIN provides an asynchronous clock, which can be further divided by a 1 or 16 prescaler.” to “An external clock signal on the DTnIN pin. When not divided, DTnIN provides a synchronous clock; when divided by 16, it is asynchronous.”
Figure 24-19/Page 24-17	Remove 16-bit divider blocks from both timer inputs, as it is not available when using an external clock source.
Section 24.4.1.2.2/Page 24-18	Change equation to: Baudrate = $f_{extc}/(16 \text{ or } 1)$, since the 16-bit divider is not available when using an external clock source.
Table 26-5/Page 26-8	Clarify in CSR field descriptions that the read-only bits can only be accessed via the BDM port and not read via the processor. The CSR is supervisor write-only from the processor.
Table 26-21/Page 26-35	Remove '1' from RAMBAR register name and mnemonic.

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